UART Protocol Design and Simulation

Lab Report

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Introduction

This report presents the design and simulation of the Universal Asynchronous Receiver Transmitter (UART) protocol implemented using System Verilog. The goal of this project is to effectively demonstrate the asynchronous serial communication facilitated by the UART protocol, highlighting both the transmitter and receiver components.

Tools

- Xilinx Vivado
- ModelSim
- Tera Term

UART System Design

Description

The UART system is designed to facilitate serial communication between devices. The system consists of three main components: a transmitter, receiver, and baud rate generator.

System Components

- Transmitter: Converts parallel data into a serial stream adding start and stop bits.
- Receiver: Accepts serial data and converts it back into parallel format.
- Baud Rate Generator: Provides timing to the transmitter and receiver to ensure synchronous data transfer at a set baud rate.

Simulation Results

Figure 1: Transmitter Module Simulation

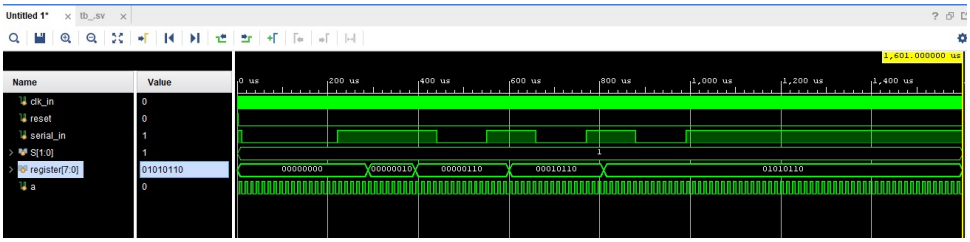

Figure 2: Receiver Module Simulation

Testing and Verification

Description

Testing involved simulating the UART system using ModelSim, and verifying the transmission and reception of data using Tera Term to monitor output.

Hardware Testing Results

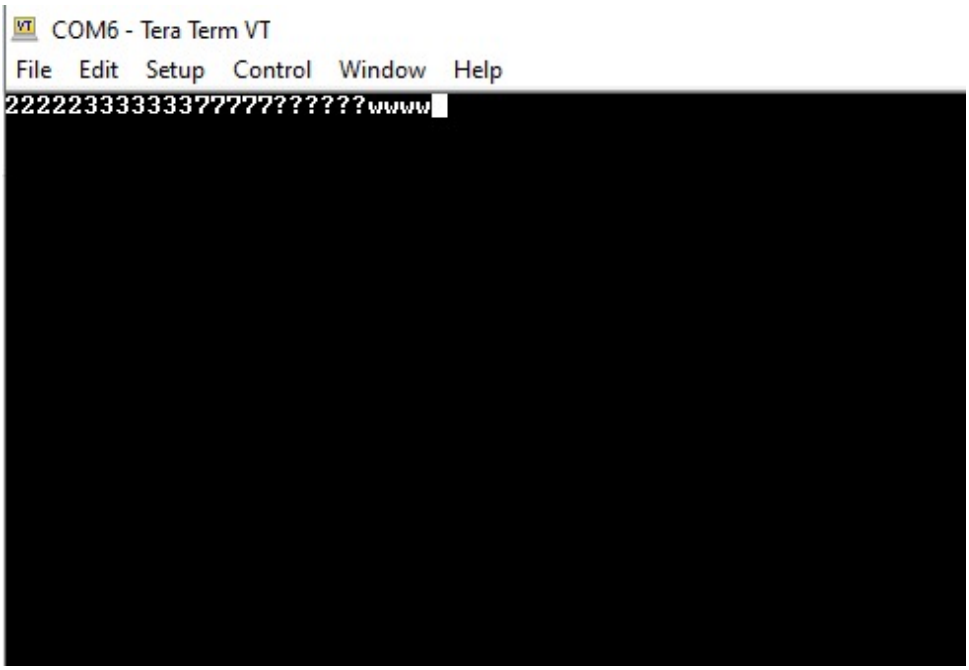

Figure 3: send ASCII values of characters

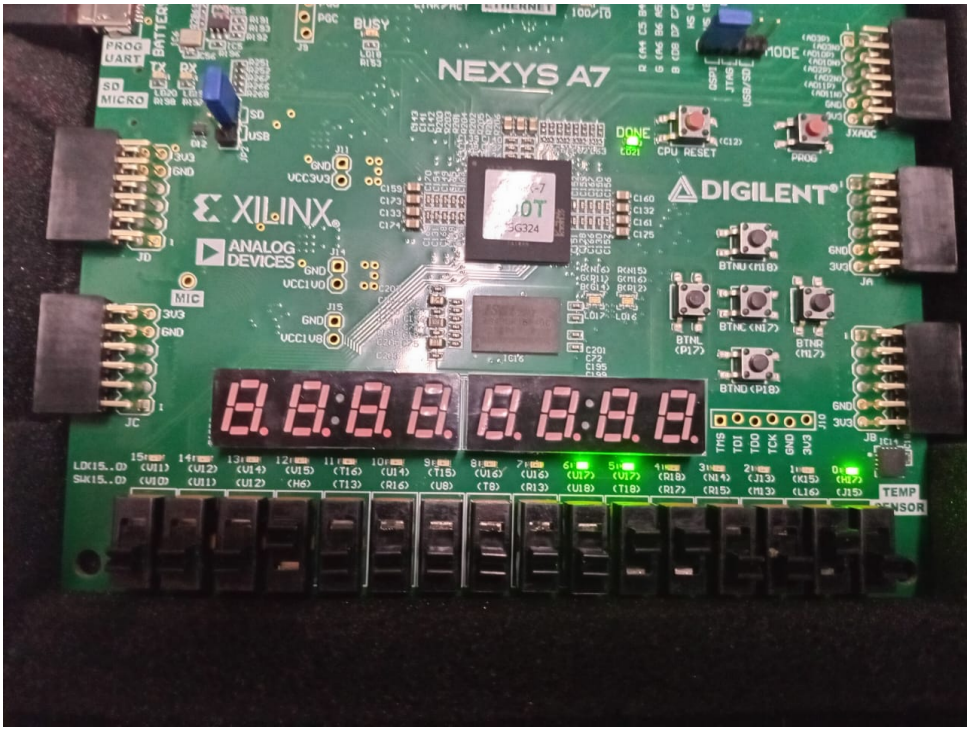

Figure 4: Received ASCII for character 'a'

Conclusion

The UART project successfully demonstrated the asynchronous serial communication between a transmitter and receiver. The UART protocol's independence from a synchronized clock signal makes it versatile for various communication needs in embedded systems. This project underscored the importance of detailed design and simulation in the field of digital communications.