

UVM Verification Project Report

SPI Core Wishbone Compatible



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1. TASK:1 Verification Plan

The following table outlines the comprehensive verification plan for the SPI Core design, covering all critical features and corresponding test cases:

Verification Plan Overview

This plan ensures a structured approach to validating SPI Core which Wishbone Compatible functionalities, with test cases designed for edge scenarios and regular operations.

Test Case ID	Test Name	Objective	Features to Verify	Stimulus	Expected Result
TC1	Reset Test	Verify control register reset values after asynchronous reset.	Directed (reset-only focus).	Upon reset, empty control registers is reset, and data pointers reset to initial states.	
TC2	Complete Read-/Write Test between Protocols	Verify correct read/write operations between Wishbone and SPI protocols.	Directed (cross-protocol verification).	DUT correctly reads and writes data between protocols. Wishbone master writes, SPI master reads and vice versa.	
TC3	Write Buffer Full Test	Verify system behavior when write buffer is full.	Directed (buffer overflow test).	System stops accepting writes when buffer is full, flags indicate full condition.	
TC4	Write Buffer Collision Test	Verify system's behavior during a buffer overflow/collision in write buffer.	Directed (overflow and collision handling).	System detects buffer overflow or collision and handles it correctly without data corruption.	
TC5	Read Buffer Full Test	Verify FIFO asserts full flag when buffer is full.	Directed (continuous writes).	full flag asserts when buffer is full, no further data can be written, write pointer stops incrementing.	

Table 1.1: Verification Plan for WB SPI

2. Usage and Verification Instructions

The following table provides clear, concise instructions on how to configure and execute the verification process for the WB SPI design:

Usage Instructions		
Follow these steps to configure, run, and verify the FIFO design using the provided testbench.		

Step	Action	Example
1. Set Parameters	Configure FIFO depth, data width, and test case number in <code>random.test</code> .	<code>depth = 16;</code> <code>width = 32;</code> <code>test = 4;</code>
2. Select Test Case	Choose the desired test case (1-7): 1: Reset Test 2: Synchronous Reset Test 3: Depth Check Test 4: Full Flag Test 5: Empty Flag Test 6: Write After Read Test 7: Exhaustive Random Test	<code>test = 1</code> for Reset Test.
3. Run Simulation	Execute the testbench using your simulator (e.g., Cadence Xcelium).	<code>xrun -f file.f ...</code>
4. Check Results	Analyze logs and scoreboard outputs for Pass/Fail.	Expected Data = 15, Actual Data = 15
5. Verify Coverage	Review the coverage report to ensure 100% coverage of states and transitions in the test number 7.	Coverage metrics logged in the simulation tool.

Table 2.1: Usage and Verification Instructions for FIFO Design

2.1 DUT Register Model

2.1.1 DUT Register Model

```
Nov 28 21:41
cc@ncdc-0057:~$ uvmreg

File Edit View Search Terminal Help
UVM INFO /quicktest.sv(30) @ 105: H10.drv [DRV] sending item
data:"(kind:UVM_READ, addr:'h1, data:'h0, n_bits:8, byte_en:'hff, status:UVM_IS_OK)"
UVM INFO /quicktest.sv(35) @ 115: H10.drv [DRV] sending item complete

-----
Name                                     Type                                     Size Value
-----
model                                   WB_SPI_regs_vendor_Cadence_Design_Systems_library_WB_SPI_Registers_version_1_0 - @3652
WB_SPI_memory_WB_SPI_registers          WB_SPI_regs_c                             - @3676
SPCR                                    uvm_reg_field                             ... RW SPCR[1:0]=2'h0
SPR                                     uvm_reg_field                             ... RW SPCR[2:2]=1'h0
CPHA                                    uvm_reg_field                             ... RW SPCR[3:3]=1'h0
CPOL                                    uvm_reg_field                             ... RW SPCR[4:4]=1'h1
HSTR                                    uvm_reg_field                             ... RW SPCR[6:6]=1'h0
SPE                                     uvm_reg_field                             ... RW SPCR[7:7]=1'h0
SPDR                                    uvm_reg_field                             ... @3721
SPDR_c                                 uvm_reg_field                             ... RW SPDR[7:0]=8'h00
SPER                                    uvm_reg_field                             ... @3752
ESPR                                    uvm_reg_field                             ... RW SPER[1:0]=2'h0
ICNT                                    uvm_reg_field                             ... RW SPER[7:6]=2'h0
SPSR                                    uvm_reg_field                             ... @3769
RFEEMPTY                               uvm_reg_field                             ... RW SPSR[0:0]=1'h1
RFFULL                                 uvm_reg_field                             ... RW SPSR[1:1]=1'h0
WFEEMPTY                               uvm_reg_field                             ... RW SPSR[2:2]=1'h1
WFFULL                                 uvm_reg_field                             ... RW SPSR[3:3]=1'h0
WCOL                                    uvm_reg_field                             ... RW SPSR[6:6]=1'h0
SPIF                                    uvm_reg_field                             ... RW SPSR[7:7]=1'h0
WB_SPI_memory                          uvm_reg_map                               0 id=@3665 seqr=H10.sqr offset=0x0 size=0x3 baseaddr=0x0
WB_SPI_memory_WB_SPI_registers          uvm_reg_map                               0 id=@3701 seqr=H10.sqr offset=0x0 size=0x2 baseaddr=0x0
-----
Name                                     Type                                     Size Value
-----
WB_SPI_memory                          uvm_reg_map                               - @3665
endian                                  uvm_little_endian                         ... UVM_LITTLE_ENDIAN
effective_sequencer                     uvm_sequencer                             ... H10.sqr
WB_SPI_memory_WB_SPI_registers          uvm_reg_map                               - @3701
endian                                  uvm_little_endian                         ... UVM_LITTLE_ENDIAN
effective_sequencer                     uvm_sequencer                             ... H10.sqr
SPCR                                    uvm_reg_field                             ... @84 + 'h0
SPDR                                    uvm_reg_field                             ... @3721 + 'h2
SPER                                    uvm_reg_field                             ... @3752 + 'h3
SPSR                                    uvm_reg_field                             ... @3769 + 'h1

UVM INFO /home/cc/mnt/XCELIN2389/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 115: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
--- UVM Report catcher Summary ---

Number of demoted UVM_FATAL reports : 0
Number of demoted UVM_ERROR reports : 0
Number of demoted UVM_WARNING reports : 0
Number of caught UVM_FATAL reports : 0
Number of caught UVM_ERROR reports : 0
Number of caught UVM_WARNING reports : 0
```

Figure 2.1: reseter model of the dut *wb_spi*.

3. Test Results

3.1 Test Results

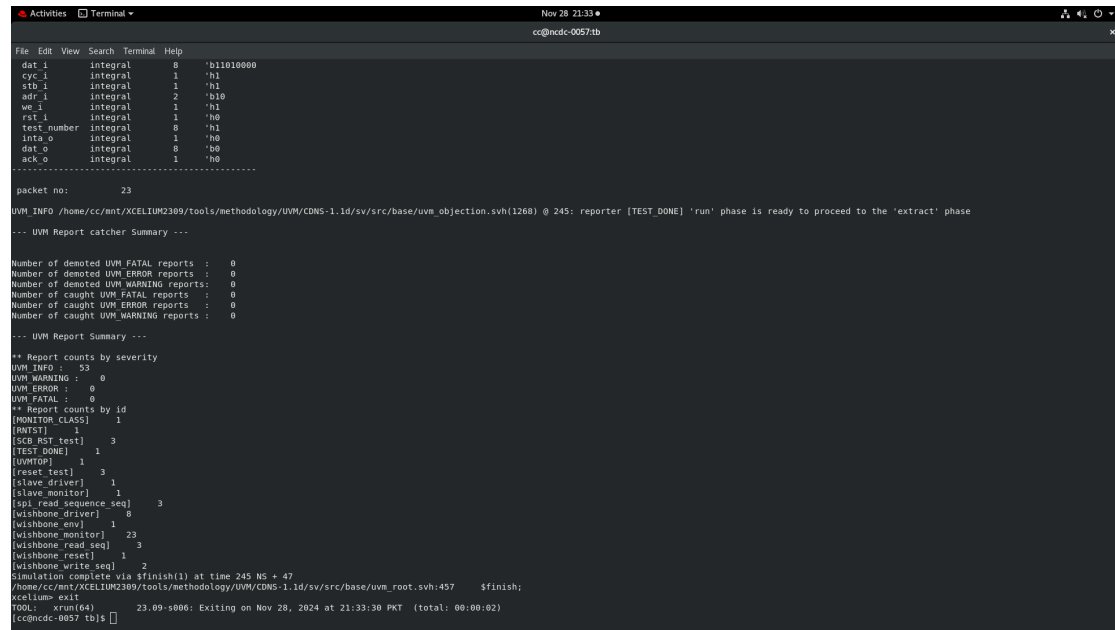
3.1.1 Test Case 1: Reset Test

```
Activities Terminal Nov 28 21:35 cc@ncdc-0057:tb
File Edit View Search Terminal Help
parent sequence (name) string 7 myseq_3
parent sequence (full name) string 62 uvm_test_top.tb.wishbone.my_agent.sequencer.reset_test.myseq_3
sequencer string 43 uvm_test_top.tb.wishbone.my_agent.sequencer

-----
UVM INFO ../Wishbone Master UVC/sv/wishbone_monitor.sv(47) @ 50: uvm_test_top.tb.wishbone.my_agent.monitor [wishbone_monitor] Sending Packet :
-----
Name Type Size Value
-----
item wishbone trans 0 054601
dat_i integral 0 'b10
cyc_i integral 1 'h1
stb_i integral 1 'h1
adr_i integral 2 'h11
we_i integral 1 'h0
rst_i integral 1 'h0
test_number integral 8 'h1
inta_o integral 1 'h0
dat_o integral 8 'h0
ack_o integral 1 'h1
-----
packet no: 4
Read data is
00000000
Read counter is 3
UVM INFO ../sv/SPI_scoreboard.sv(88) @ 50: uvm_test_top.tb.scoreboard [SCB_RST_test] Control register Matched
UVM INFO ../sv/SPI_scoreboard.sv(86) @ 50: uvm_test_top.tb.scoreboard [SCB_RST_test] Status register Matched
UVM INFO ../sv/SPI_scoreboard.sv(92) @ 50: uvm_test_top.tb.scoreboard [SCB_RST_test] Extension register Matched
UVM INFO ../Wishbone Master UVC/sv/wishbone_seqs.sv(60) @ 50: uvm_test_top.tb.wishbone.my_agent.sequencer@reset_test.myseq_3 [wishbone_write_seq] Executing wishbone_write_seq sequence
UVM INFO ../Wishbone Master UVC/sv/wishbone_driver.sv(36) @ 50: uvm_test_top.tb.wishbone.my_agent.driver [wishbone_driver] Packet is
-----
Name Type Size Value
-----
req wishbone trans 0 05463
dat_i integral 0 'b11010000
cyc_i integral 1 'h1
stb_i integral 1 'h1
adr_i integral 2 'h10
we_i integral 1 'h1
rst_i integral 1 'h0
test_number integral 8 'h1
inta_o integral 1 'h0
dat_o integral 8 'h0
ack_o integral 1 'h0
begin time time 64 50
depth int 32 'd3
parent sequence (name) string 7 myseq_3
parent sequence (full name) string 62 uvm_test_top.tb.wishbone.my_agent.sequencer.reset_test.myseq_3
sequencer string 43 uvm_test_top.tb.wishbone.my_agent.sequencer
-----
UVM INFO ../Wishbone Master UVC/sv/wishbone_monitor.sv(47) @ 60: uvm_test_top.tb.wishbone.my_agent.monitor [wishbone_monitor] Sending Packet :
```

Figure 3.1: Simulation result for Reset Test.

3.1.2 Test Case 1: Reset Test error



```
File Edit View Search Terminal Help
Nov 28 21:33
cc@ncdc-0057.tb

dat_i      integral      8      'b11010000
cyc_i      integral      1      'h1
stb_i      integral      1      'h1
adr_i      integral      2      'b10
we_i       integral      1      'h1
rst_i      integral      1      'h0
test_number integral      8      'h1
inta_o     integral      1      'h0
dat_o      integral      8      'b0
ack_o      integral      1      'h0

-----
packet no:      23

UVM_INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/DNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 245: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
--- UVM Report catcher Summary ---

Number of demoted UVM FATAL reports : 0
Number of demoted UVM ERROR reports : 0
Number of demoted UVM WARNING reports: 0
Number of caught UVM FATAL reports : 0
Number of caught UVM ERROR reports : 0
Number of caught UVM WARNING reports: 0
--- UVM Report Summary ---

** Report counts by severity
UVM INFO : 53
UVM WARNING : 0
UVM ERROR : 0
UVM FATAL : 0
** Report counts by id
[MONITOR_CLASS] 1
[RNTEST] 1
[SCB_RST_test] 3
[TEST_DONE] 1
[UWANTOP] 1
[reset test] 3
[slave driver] 1
[slave monitor] 1
[spl_read_sequence_seq] 3
[wishbone_driver] 8
[wishbone_env] 1
[wishbone_monitor] 23
[wishbone_read_seq] 3
[wishbone_reset] 1
[wishbone_write_seq] 2
Simulation complete via sfinish() at time 245 NS + 47
/home/cc/mnt/XCELIUM2309/tools/methodology/UVM/DNS-1.1d/sv/src/base/uvm_root.svh:457 $finish;
xcelium> exit
TOOL: Xrun(64) 23.09-5000: Exiting on Nov 28, 2024 at 21:33:30 PKT (total: 00:00:02)
cc@ncdc-0057.tb$
```

Figure 3.2: Simulation result for Reset Test.

3.1.3 Test Case 2: Complete read write between the protocols

```

File Edit View Search Terminal Help
Nov 28 21:35
cc@ncdc-0057.tb

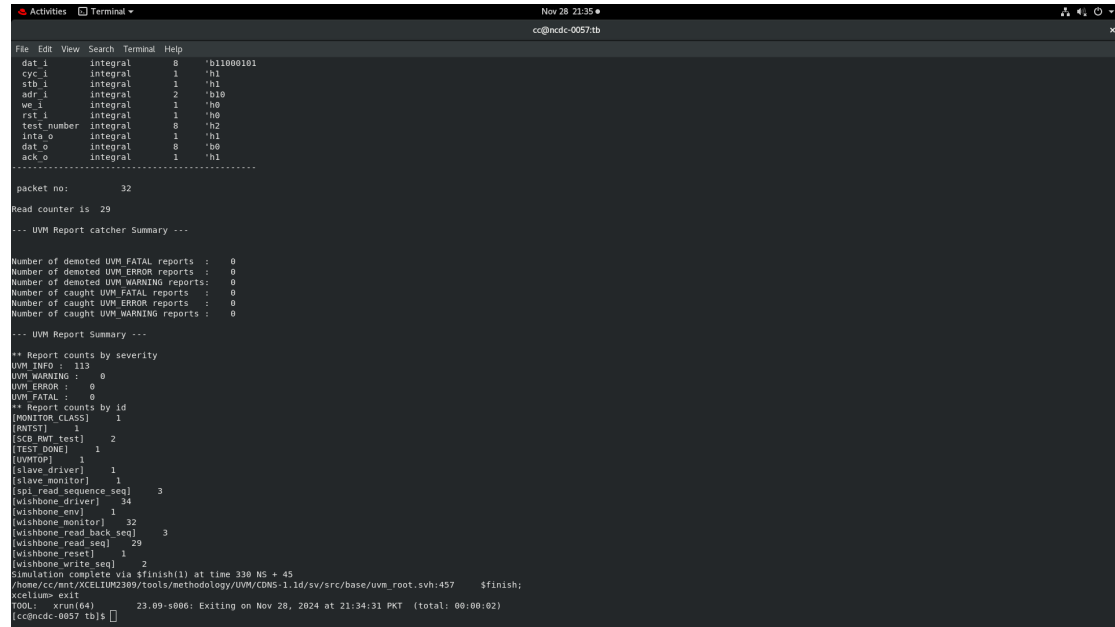
dat_i integral 8 'b11101001
cyc_i integral 1 'h1
stb_i integral 1 'h1
adr_i integral 2 'b10
we_i integral 1 'h0
rst_i integral 1 'h0
test_number integral 8 'h2
inta_o integral 1 'h0
dat_o integral 8 'b0
ack_o integral 1 'h0
begin_time time 64 280
depth int 32 'd3
parent sequence (name) string 7 myseq_2
parent sequence (full name) string 74 uvm_test_top.tb.wishbone.my_agent.sequencer.wishbone_read_back_seq.myseq_2
sequencer string 43 uvm_test_top.tb.wishbone.my_agent.sequencer

-----
UVM INFO ../Wishbone_Master:UVC/sv/wishbone_monitor.sv(47) @ 290: uvm_test_top.tb.wishbone.my_agent.monitor [wishbone_monitor] Sending Packet :
-----
Name Type Size Value
-----
Item wishbone trans - @5888
dat_i integral 8 'b1001
cyc_i integral 1 'h1
stb_i integral 1 'h1
adr_i integral 2 'b10
we_i integral 1 'h0
rst_i integral 1 'h0
test_number integral 8 'h2
inta_o integral 1 'h1
dat_o integral 8 'b1110110
ack_o integral 1 'h1
-----
packet no: 28
Read counter is 20
UVM INFO ../sv/SPI_scoreboard.sv(185) @ 290: uvm_test_top.tb.scoreboard [SCB_RMT_test] In value Matched
UVM INFO ../sv/SPI_scoreboard.sv(113) @ 290: uvm_test_top.tb.scoreboard [SCB_RMT_test] Out value Matched
UVM INFO ../Wishbone_Master:UVC/sv/wishbone_seqs.sv(89) @ 290: uvm_test_top.tb.wishbone.my_agent.sequencer@wishbone_read_back_seq.myseq_2 [wishbone_read_seq] Executing wishbone_read_seq sequence
UVM INFO ../Wishbone_Master:UVC/sv/wishbone_driver.sv(36) @ 290: uvm_test_top.tb.wishbone.my_agent.driver [wishbone_driver] Packet is
-----
Name Type Size Value
-----
req wishbone trans - @5710
dat_i integral 8 'b1111101
cyc_i integral 1 'h1
stb_i integral 1 'h1
adr_i integral 2 'b10
we_i integral 1 'h0
rst_i integral 1 'h0
test_number integral 8 'h2
inta_o integral 1 'h0
dat_o integral 8 'b0
ack_o integral 1 'h0

```

Figure 3.3: test₂.

3.1.4 Test Case 2: Complete read write between the protocols error



```
File Edit View Search Terminal Help
Nov 28 21:35
cc@ncdc-0057.tb

dat_i      integral 8 'b11000101
cyc_i      integral 1 'h1
stb_i      integral 1 'h1
adr_i      integral 2 'd10
we_i       integral 1 'h0
rst_i      integral 1 'h0
test number integral 0 'h2
inta_o     integral 1 'h1
dat_o      integral 8 'b0
ack_o      integral 1 'h1

-----
packet no:      32
Read counter is 29

--- UVM Report catcher Summary ---

Number of demoted UVM FATAL reports : 0
Number of demoted UVM ERROR reports : 0
Number of demoted UVM WARNING reports: 0
Number of caught UVM FATAL reports : 0
Number of caught UVM ERROR reports : 0
Number of caught UVM WARNING reports : 0

--- UVM Report Summary ---

** Report counts by severity
UVM INFO : 113
UVM WARNING : 0
UVM ERROR : 0
UVM FATAL : 0
** Report counts by id
[MONITOR_CLASS] 1
[RMST] 1
[SCB_RMT_test] 2
[TEST_DONE] 1
[UWNTOP] 1
[slave_driver] 1
[slave_monitor] 1
[spi_read_sequence_seq] 3
[wishbone_driver] 34
[wishbone_env] 1
[wishbone_monitor] 32
[wishbone_read_back_seq] 3
[wishbone_read_seq] 29
[wishbone_reset] 1
[wishbone_write_seq] 2
Simulation complete via $finish() at time 338 NS + 45
/home/cc/mnt/XCELLUM2309/tools/methodology/UVM/CDNS-1.1d/src/base/uvm_root.svh:457 $finish;
xcellium> exit
TOOL: xrun(64) 23.09-s080: Exiting on Nov 28, 2024 at 21:34:31 PKT (total: 00:00:02)
cc@ncdc-0057.tb$
```

Figure 3.4: test₂.

3.1.5 test₂

```

Nov 28 21:37
cc@ncdc-0057.tb

File Edit View Search Terminal Help
-----
cyc_i    integral 1 'h1
stb_i    integral 1 'h1
adr_i    integral 2 'b10
we_i     integral 1 'h1
rst_i    integral 1 'h0
test_number integral 8 'h3
inta_o   integral 1 'h0
dat_o    integral 8 'h0
ack_o    integral 1 'h1

-----
packet no: 12

UVM INFO ../sv/Wishbone Master UVC/sv/wishbone_segs.sv(35) @ 138: uvm_test_top.tb.wishbone.my_agent.sequencer@test 3 [test 3] drop objection
UVM INFO ../sv/Wishbone Master UVC/sv/wishbone_monitor.sv(47) @ 140: uvm_test_top.tb.wishbone.my_agent.monitor [wishbone_monitor] Sending Packet :
-----
Name      Type      Size Value
-----
item      wishbone.trans - 85436
dat_i     integral 8 'b1111011
cyc_i     integral 1 'h1
stb_i     integral 1 'h1
adr_i     integral 2 'b1
we_i      integral 1 'h0
rst_i     integral 1 'h0
test_number integral 8 'h3
inta_o    integral 1 'h0
dat_o     integral 8 'b1001
ack_o     integral 1 'h0

-----
packet no: 13

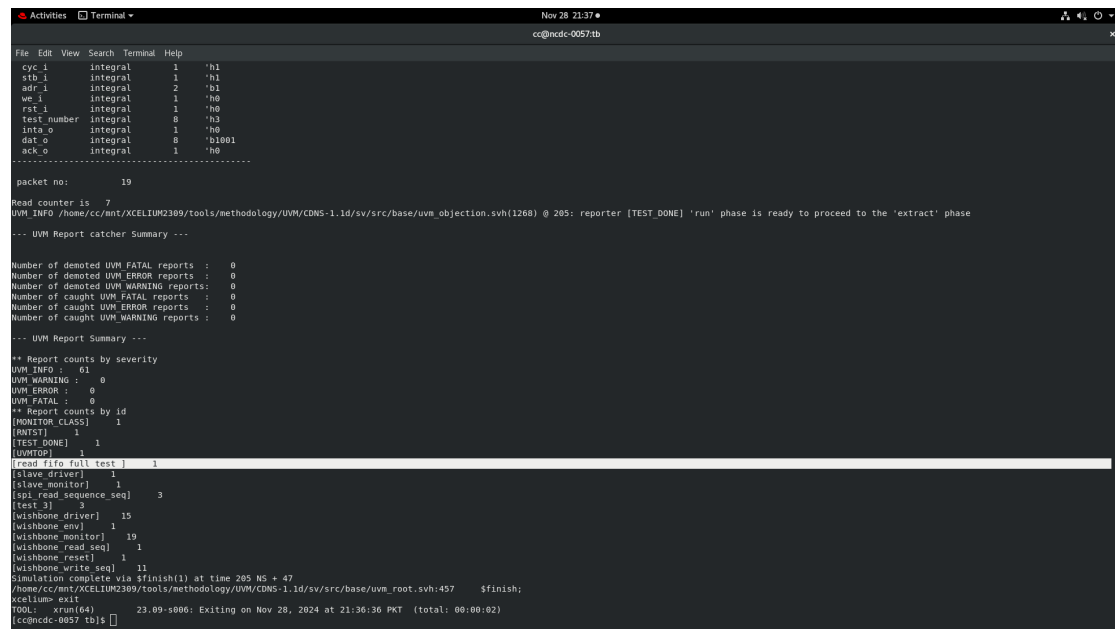
Read data is
00001001
Read counter is 1
UVM INFO ../sv/SPI scoreboard.sv(125) @ 140: uvm_test_top.tb.scoreboard [read fifo full test ] the fifo buffer full matched
UVM INFO ../sv/Wishbone Master UVC/sv/wishbone_monitor.sv(47) @ 150: uvm_test_top.tb.wishbone.my_agent.monitor [wishbone_monitor] Sending Packet :
-----
Name      Type      Size Value
-----
item      wishbone.trans - 85482
dat_i     integral 8 'b1111011
cyc_i     integral 1 'h1
stb_i     integral 1 'h1
adr_i     integral 2 'b1
we_i      integral 1 'h0
rst_i     integral 1 'h0
test_number integral 8 'h3
inta_o    integral 1 'h0
dat_o     integral 8 'b1001
ack_o     integral 1 'h1

-----
packet no: 14

```

Figure 3.5: Simulation result for Depth Check Test.

3.1.6 test₃



```
File Edit View Search Terminal Help
Nov 28 21:37
cc@ncdc-0057.tb

cyc_i      integral 1 'h1
srb_i      integral 1 'h1
adr_i      integral 2 'b1
we_i       integral 1 'h0
rst_i      integral 1 'h0
test_number integral 8 'h3
inta_o     integral 1 'h0
dat_o      integral 8 'b1001
ack_o      integral 1 'h0
-----
packet no: 19
Read counter is 7
UVM_INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CNDS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 205: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
--- UVM Report catcher Summary ---
Number of demoted UVM FATAL reports : 0
Number of demoted UVM ERROR reports : 0
Number of demoted UVM WARNING reports: 0
Number of caught UVM FATAL reports : 0
Number of caught UVM ERROR reports : 0
Number of caught UVM WARNING reports: 0
--- UVM Report Summary ---
** Report counts by severity
UVM INFO : 61
UVM WARNING : 0
UVM ERROR : 0
UVM FATAL : 0
** Report counts by id
[MONITOR_CLASS] 1
[RNTEST] 1
[TEST_DONE] 1
[UVMTOP] 1
[read_fifo_full_test] 1
[slave_driver] 1
[slave_monitor] 1
[spl_read_sequence_seq] 3
[test_3] 3
[wishbone_driver] 15
[wishbone_env] 1
[wishbone_monitor] 19
[wishbone_read_seq] 1
[wishbone_reset] 1
[wishbone_write_seq] 11
Simulation complete via $finish() at time 205 NS + 47
/home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CNDS-1.1d/sv/src/base/uvm_root.svh:457 $finish;
xcelium> exit
TOOL: Xrun(64) 23.09-5000: Exiting on Nov 28, 2024 at 21:36:36 PKT (total: 00:00:02)
cc@ncdc-0057.tb$
```

Figure 3.6: test₃.

3.1.7 Test Case 4: Write buffer Collision

```
Nov 28 21:38
cc@ncdc-0057.tb

UVM INFO ../Wishbone Master UVC/sv/wishbone_seqs.sv(35) @ 238: uvm_test_top.tb.wishbone.my_agent.sequencer@test_4 [test_4] drop objection
UVM INFO /home/cc/mnt/XCELIUR2389/tools/methodology/UVM/CWMS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 240: reporter [TEST DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM INFO ../Wishbone Master UVC/sv/wishbone_monitor.sv(47) @ 248: uvm_test_top.tb.wishbone.my_agent.monitor [wishbone_monitor] Sending Packet :
-----
Name      Type      Size  Value
-----
item      wishbone_trans  -  @5657
dat_i     integral      8  'b1001111
cyc_i     integral      1  'h1
stb_i     integral      1  'h1
adr_i     integral      2  'b1
we_i      integral      1  'h0
rst_i     integral      1  'h0
test_number integral      0  'h4
inta_o    integral      1  'h1
dat_o     integral      8  'b11000100
ack_o     integral      1  'h0
-----
packet no:      23
Read data is
11000100
Read counter is 1
UVM INFO ../sv/SPI_scoreboard.sv(135) @ 248: uvm_test_top.tb.scoreboard [write fifo WC0L test ] the fifo buffer WC0L matched
--- UVM Report catcher Summary ---
Number of demoted UVM FATAL reports : 0
Number of demoted UVM ERROR reports : 0
Number of demoted UVM WARNING reports: 0
Number of caught UVM FATAL reports : 0
Number of caught UVM ERROR reports : 0
Number of caught UVM WARNING reports : 0
--- UVM Report Summary ---
** Report counts by severity
UVM INFO : 85
UVM WARNING : 0
UVM ERROR : 0
UVM FATAL : 0
** Report counts by id
[MONITOR_CLASS] 1
[PUTTEST] 1
[TEST_DONE] 1
[UNTOP] 1
[slave driver] 1
[slave monitor] 1
[spl_read_sequence_seq] 3
[test_4] 5
[wishbone driver] 25
[wishbone env] 1
```

Figure 3.7: test₄.

3.1.8 Test Case 5: Read buffer Full

```

Nov 28 21:39
cc@ncdc-0057.tb

File Edit View Search Terminal Help

cyc_i      integral 1 'h1
stb_i      integral 1 'h1
adr_i      integral 2 'b1
we_i       integral 1 'h0
rst_i      integral 1 'h0
test_number integral 8 'h5
inta_o     integral 1 'h0
dat_o      integral 8 'h0
ack_o      integral 1 'h0
begin_time time      64 840
depth      int       32 'd3
parent sequence (name) string 7 myseq_2
parent sequence (full name) string 50 uvm_test_top.tb.wishbone.my_agent.sequencer.test_5.myseq_2
sequencer  string 43 uvm_test_top.tb.wishbone.my_agent.sequencer

UVM INFO ../sv/Wishbone Master UVC/sv/wishbone_monitor.sv(47) @ 850: uvm_test_top.tb.wishbone.my_agent.monitor [wishbone_monitor] Sending Packet :

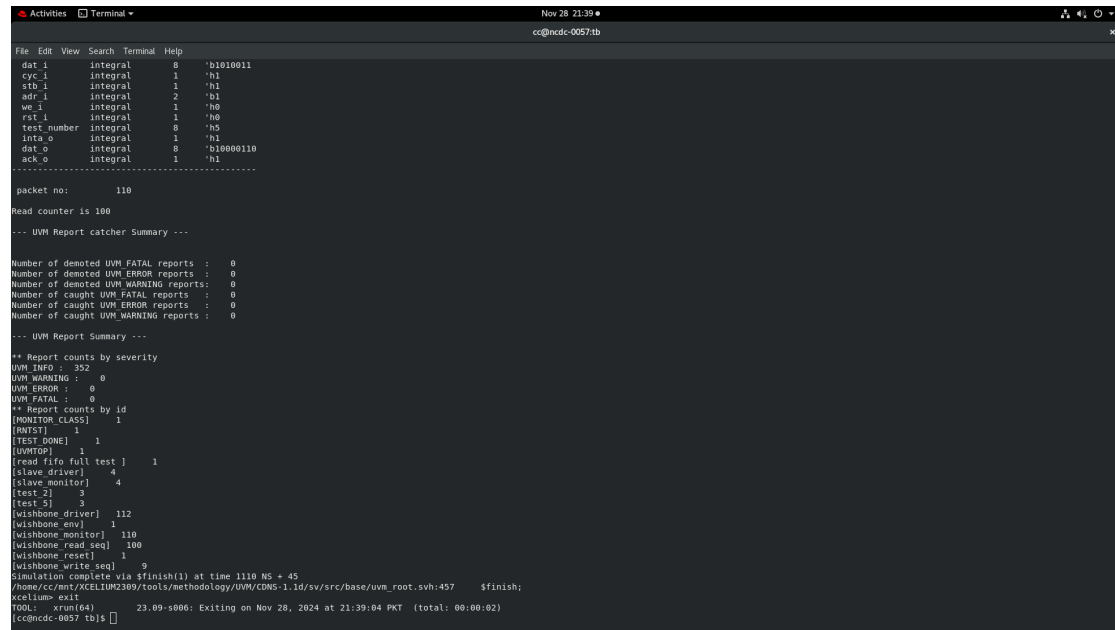
-----
Name      Type      Size Value
-----
item      wishbone_trans - @0209
dat_i     integral 8 'b11100010
cyc_i     integral 1 'h1
stb_i     integral 1 'h1
adr_i     integral 2 'b1
we_i      integral 1 'h0
rst_i     integral 1 'h0
test_number integral 8 'h5
inta_o    integral 1 'h1
dat_o     integral 8 'b10000110
ack_o     integral 1 'h1
-----
packet no: 84

Read counter is 74
UVM INFO ../sv/SPI_scoreboard.sv(143) @ 850: uvm_test_top.tb.scoreboard [read fifo full test ] the fifo read buffer full matched
UVM INFO ../sv/Wishbone Master UVC/sv/wishbone_seqs.sv(89) @ 850: uvm_test_top.tb.wishbone.my_agent.sequencer@test_5.myseq_2 [wishbone_read_seq] Executing wishbone_read_seq sequence
UVM INFO ../sv/Wishbone Master UVC/sv/wishbone_driver.sv(50) @ 850: uvm_test_top.tb.wishbone.my_agent.driver [wishbone_driver] Packet is

-----
Name      Type      Size Value
-----
req       wishbone_trans - @0083
dat_i     integral 8 'b10110011
cyc_i     integral 1 'h1
stb_i     integral 1 'h1
adr_i     integral 2 'b1
we_i      integral 1 'h0
rst_i     integral 1 'h0
test_number integral 8 'h5
inta_o    integral 1 'h0
dat_o     integral 8 'b0
ack_o     integral 1 'h0
begin_time time      64 850
depth      int       32 'd3
  
```

Figure 3.8: test 5.

3.1.9 Test Case 5: Read buffer Full



```
File Edit View Search Terminal Help
Nov 28 21:39
cc@ncdc-0057.tb

dat_i      integral      8      'b1010011
cyc_i      integral      1      'h1
stb_i      integral      1      'h1
adr_i      integral      2      'd1
we_i       integral      1      'h0
rst_i      integral      1      'h0
test_number integral      8      'h0
inta_o     integral      1      'h1
dat_o      integral      8      'b10000110
ack_o      integral      1      'h1
-----
packet no:      110
Read counter is 100
--- UVM Report catcher Summary ---
Number of demoted UVM FATAL reports : 0
Number of demoted UVM ERROR reports : 0
Number of demoted UVM WARNING reports: 0
Number of caught UVM FATAL reports  : 0
Number of caught UVM ERROR reports  : 0
Number of caught UVM WARNING reports: 0
--- UVM Report Summary ---
** Report counts by severity
UVM INFO : 352
UVM WARNING : 0
UVM ERROR : 0
UVM FATAL : 0
** Report counts by id
[MONITOR_CLASS] 1
[RNTEST] 1
[TEST_DONE] 1
[UVMTOP] 1
[read fifo full test] 1
[slave_driver] 4
[slave_monitor] 4
[test_2] 3
[test_5] 3
[wishbone_driver] 112
[wishbone_env] 1
[wishbone_monitor] 110
[wishbone_read_seq] 100
[wishbone_reset] 1
[wishbone_write_seq] 0
Simulation complete via sfinish() at time 1110 NS + 45
/home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDMS-1.1d/sv/src/base/uvm_root.svh:457 sfinish;
xcellium> exit
TOOL: Xrun(64) 23.09-1000: Exiting on Nov 28, 2024 at 21:39:04 PKT (total: 00:00:02)
cc@ncdc-0057.tb$
```

Figure 3.9: test₅.