

RISC-V Processor Verification Report

Test Results and Analysis



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Contents

1	Introduction	2
2	Test 1: Basic Instruction Verification	3
2.1	Data Memory Waveform	3
2.2	Register File Waveform	3
3	Test 2	4
3.1	Data Memory Trace	4
3.2	Register File Trace	4
4	Test 3: Full Execution Trace	5
4.1	Tracer Core Snapshot	5
4.2	Simulation Output Log	5
5	Conclusion	7

Chapter 1

Introduction

This report presents the results of RISC-V single-cycle processor verification through three distinct tests. Each test assesses the processor's performance with different sets of instructions, validating the core's functionality and identifying mismatches. The verification uses Cadence Xcelium simulation and includes Tracer IP integration to compare results with reference outputs.

Chapter 2

Test 1: Basic Instruction Verification

The first test focused on validating basic RISC-V instructions, including arithmetic and memory operations.

2.1 Data Memory Waveform

The following figure shows the data memory waveforms captured during Test 1.

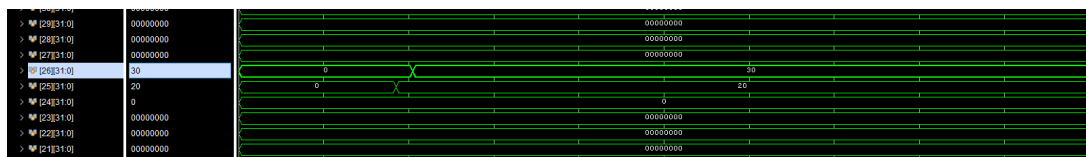


Figure 2.1: Test 1: Data Memory Waveform

2.2 Register File Waveform

The register file contents during the execution of Test 1 are shown below. This verifies the correct write-back behavior of the processor.

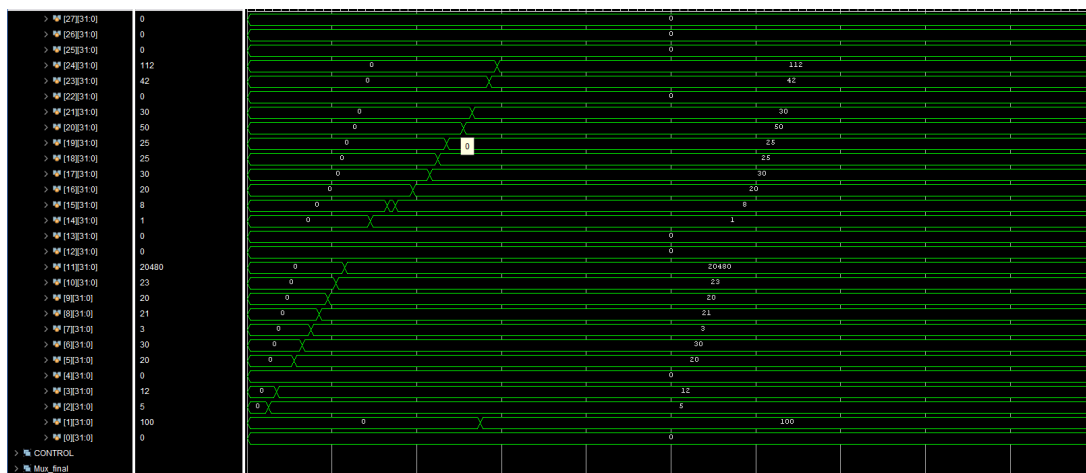


Figure 2.2: Test 1: Register File Waveform

Chapter 3

Test 2

Test 2 focused on verifying memory operations such as loads and stores, along with branching instructions.

3.1 Data Memory Trace

The trace of data memory operations is shown below, highlighting memory writes and reads.

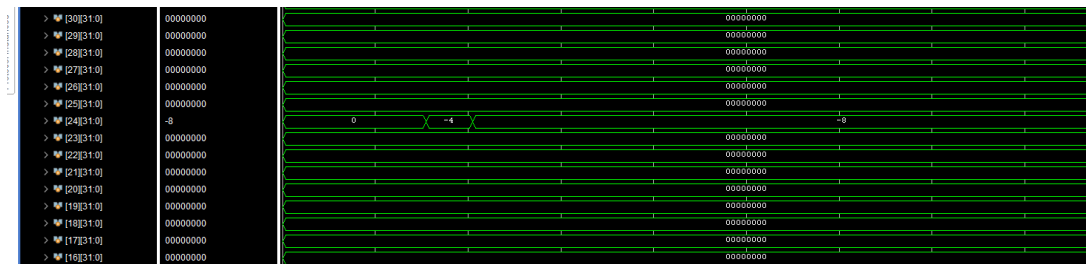


Figure 3.1: Test 2: Data Memory Trace

3.2 Register File Trace

The following figure shows the register file state during Test 2. This helps verify whether the branching instructions update the registers correctly.

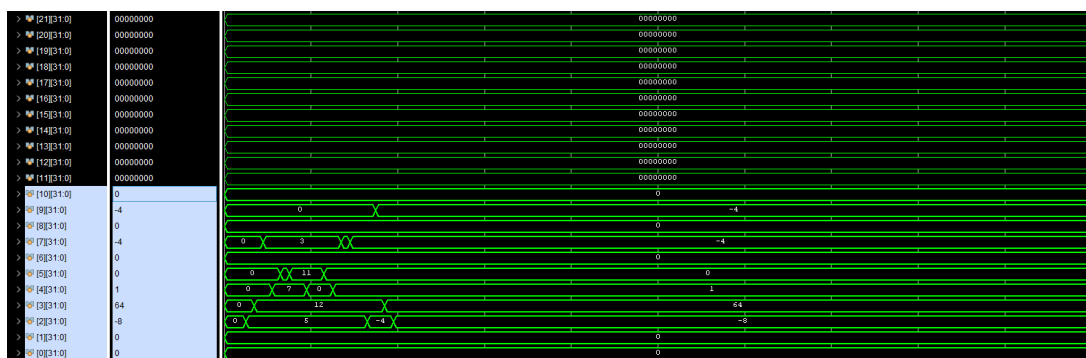
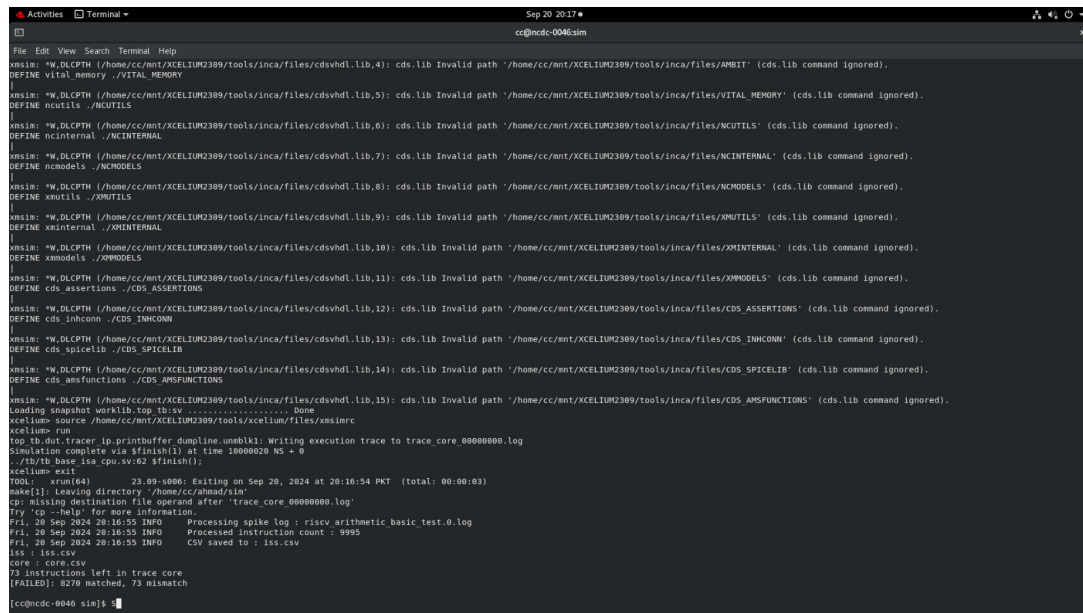


Figure 3.2: Test 2: Register File Trace



```

File Edit View Search Terminal Help
cc@ncdc-0046:~$
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,4): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/AMBIT' (cds.lib command ignored).
DEFINE vital_memory ./VITAL_MEMORY
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,5): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/VITAL_MEMORY' (cds.lib command ignored).
DEFINE ncutils ./NCUTILS
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,6): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/NCUTILS' (cds.lib command ignored).
DEFINE ncinternal ./NCINTERNAL
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,7): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/NCINTERNAL' (cds.lib command ignored).
DEFINE ncmmodels ./NCMODELS
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,8): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/NCMODELS' (cds.lib command ignored).
DEFINE xutils ./XUTILS
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,9): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/XUTILS' (cds.lib command ignored).
DEFINE xinternal ./XMINTERNAL
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,10): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/XMINTERNAL' (cds.lib command ignored).
DEFINE xmodels ./XMODELS
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,11): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/XMODELS' (cds.lib command ignored).
DEFINE cds_assertions ./CDS_ASSERTIONS
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,12): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/CDS_ASSERTIONS' (cds.lib command ignored).
DEFINE cds_inhconn ./CDS_INHCONN
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,13): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/CDS_INHCONN' (cds.lib command ignored).
DEFINE cds_spicelib ./CDS_SPICELIB
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,14): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/CDS_SPICELIB' (cds.lib command ignored).
DEFINE cds_amsfunctions ./CDS_AMSFUNCTIONS
|
msim: "W,DLCPH (/home/cc/mnt/XCELIUM2389/tools/inca/files/cdsvhdl.lib,15): cds.lib Invalid path '/home/cc/mnt/XCELIUM2389/tools/inca/files/CDS_AMSFUNCTIONS' (cds.lib command ignored).
Loading snapshot worklib_top.tb sv: ..... Done
xcelium> source /home/cc/mnt/XCELIUM2389/tools/xcelium/files/xmsimrc
xcelium> run
top.tb.dut.tracer ip.printbuffer.dumpline.unabkl: Writing execution trace to trace_core_00000000.log
Simulation complete via $finish() at time 10000000 NS + 0
../tb/tb_base isa.cpu.sv:62 $finish():
xcelium> exit
23.09-s086: Exiting on Sep 20, 2024 at 20:16:54 PKT (total: 00:00:03)
make[1]: Leaving directory '/home/cc/ahmad/sim'
cp: missing destination file operand after 'trace_core_00000000.log':
Try 'cp --help' for more information.
Fri, 20 Sep 2024 20:16:55 INFO Processing spike log : riscv_arithmetic_basic_test.0.log
Fri, 20 Sep 2024 20:16:55 INFO Processed instruction count : 9995
Fri, 20 Sep 2024 20:16:55 INFO CSV saved to : iss.csv
iss : iss.csv
core : core.csv
73 instructions left in trace core
[FAILED]: 9270 matched, 73 mismatch
cc@ncdc-0046:~$

```

Figure 4.2: Test 3: Tracer Simulation Output Log

Chapter 5

Conclusion

The verification of the RISC-V single-cycle processor was conducted through three tests. Test 1 validated basic instructions, Test 2 focused on memory and branching, and Test 3 provided a complete execution trace. While a few mismatches were detected, the majority of the instructions executed correctly, demonstrating the overall functionality of the processor.