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Chapter 1

Introduction

This report presents the results of RISC-V single-cycle processor verification through three distinct tests. Each test assesses the processor's performance with different sets of instructions, validating the core's functionality and identifying mismatches. The verification uses Cadence Xcelium simulation and includes Tracer IP integration to compare results with reference outputs.

Chapter 2

Test 1: Basic Instruction Verification

The first test focused on validating basic RISC-V instructions, including arithmetic and memory operations.

2.1 Data Memory Waveform

The following figure shows the data memory waveforms captured during Test 1.

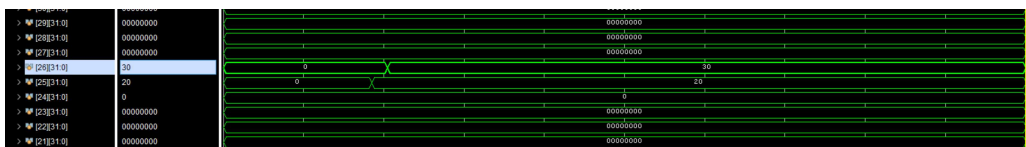


Figure 2.1: Test 1: Data Memory Waveform

2.2 Register File Waveform

The register file contents during the execution of Test 1 are shown below. This verifies the correct write-back behavior of the processor.

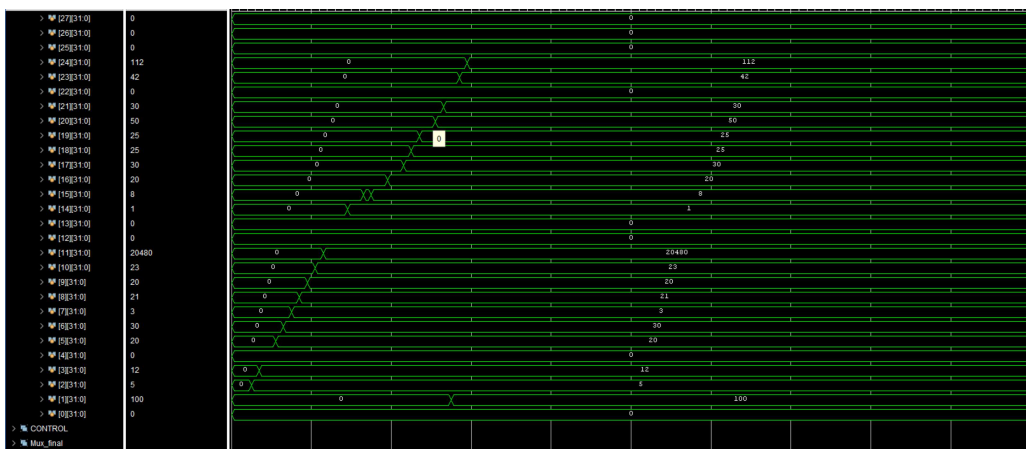


Figure 2.2: Test 1: Register File Waveform

Chapter 3

Test 2

Test 2 focused on verifying memory operations such as loads and stores, along with branching instructions.

3.1 Data Memory Trace

The trace of data memory operations is shown below, highlighting memory writes and reads.

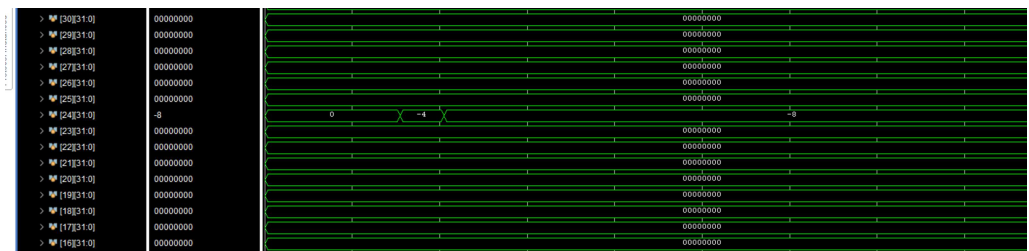


Figure 3.1: Test 2: Data Memory Trace

3.2 Register File Trace

The following figure shows the register file state during Test 2. This helps verify whether the branching instructions update the registers correctly.

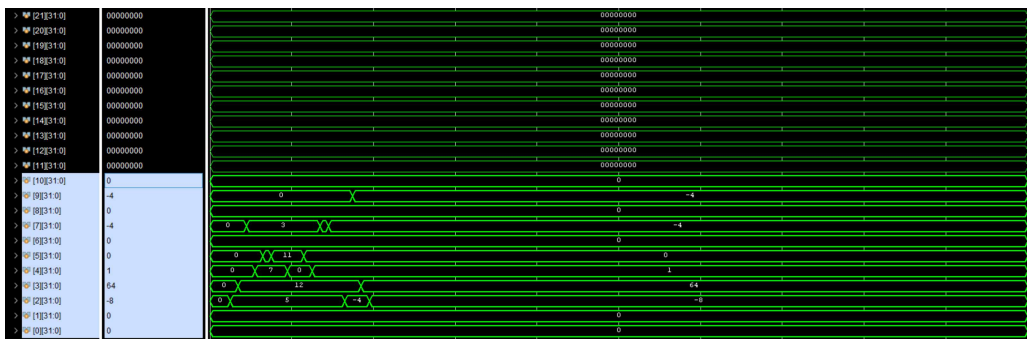


Figure 3.2: Test 2: Register File Trace

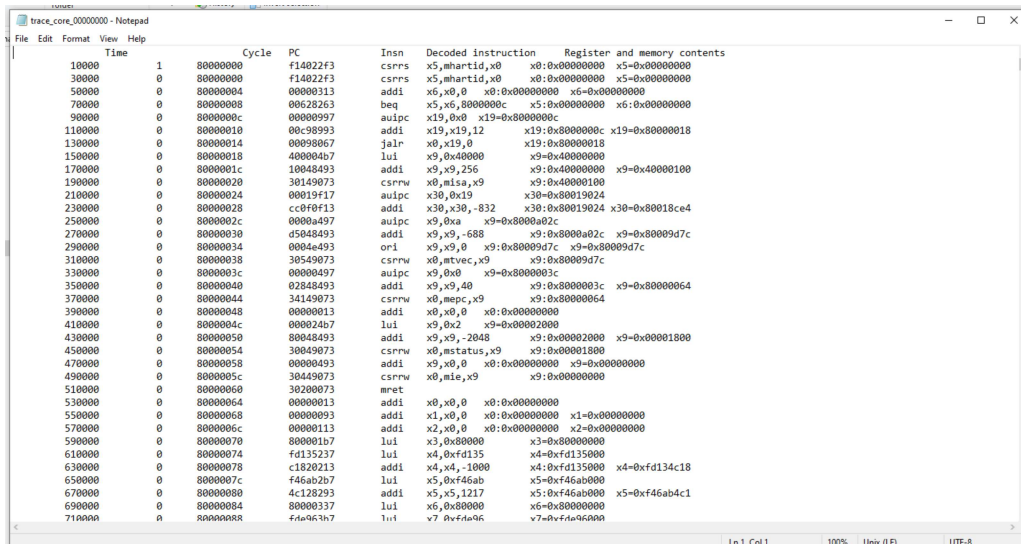
Chapter 4

Test 3: Full Execution Trace

Test 3 included a full execution trace captured by the Tracer IP to verify the correctness of control flow and data operations in the processor.

4.1 Tracer Core Snapshot

The following snapshot from the Tracer core shows the instruction execution and comparison with reference values.



Time	Cycle	PC	Insn	Decoded instruction	Register and memory contents
10000	1	80000000	f14022f3	csrrs	x5, mhartid, x0 x0:0x00000000 x5=0x00000000
30000	0	80000000	f14022f3	csrrs	x5, mhartid, x0 x0:0x00000000 x5=0x00000000
50000	0	80000004	00003113	addi	x6, x0, 0 x0:0x00000000 x6=0x00000000
70000	0	80000008	00028263	beq	x5, x6, 8000000c x5:0x00000000 x6:0x00000000
90000	0	8000000c	00009997	auipc	x19, 0x0 x19=0x8000000c
110000	0	80000010	00c98993	addi	x19, x19, 12 x19:0x8000000c x19=0x80000018
130000	0	80000014	00090867	jalr	x0, x19, 0 x19:0x80000018
150000	0	80000018	400004b7	lui	x9, 0x40000000 x9=0x40000000
170000	0	8000001c	10048493	addi	x9, x9, 256 x9:0x40000000 x9=0x40000100
190000	0	80000020	30149073	csrrw	x0, misa, x9 x9:0x40000100
210000	0	80000024	00019f17	auipc	x30, 0x19 x30=0x80019024
230000	0	80000028	cc0f0f13	addi	x30, x30, -832 x30:0x80019024 x30=0x80018ce4
250000	0	8000002c	0000a497	auipc	x9, 0xa x9=0x8000a02c
270000	0	80000030	d5048493	addi	x9, x9, -688 x9:0x8000a02c x9=0x80009d7c
290000	0	80000034	0004e493	orl	x9, x9, 0 x9:0x80009d7c x9=0x80009d7c
310000	0	80000038	30549073	csrrw	x0, mtvec, x9 x9:0x80009d7c
330000	0	8000003c	00000497	auipc	x9, 0x0 x9=0x8000003c
350000	0	80000040	02348493	addi	x9, x9, 40 x9:0x8000003c x9=0x80000064
370000	0	80000044	34149073	csrrw	x0, mepc, x9 x9:0x80000064
390000	0	80000048	00000013	addi	x0, x0, 0 x0:0x00000000
410000	0	8000004c	000024b7	lui	x9, 0x2 x9=0x00002000
430000	0	80000050	80048493	addi	x9, x9, -2048 x9:0x00002000 x9=0x00001800
450000	0	80000054	30049073	csrrw	x0, mstatus, x9 x9:0x00001800
470000	0	80000058	00000493	addi	x9, x0, 0 x0:0x00000000 x9=0x00000000
490000	0	8000005c	30449073	csrrw	x0, mie, x9 x9:0x00000000
510000	0	80000060	30200073	mret	
530000	0	80000064	00000013	addi	x0, x0, 0 x0:0x00000000
550000	0	80000068	00000093	addi	x1, x0, 0 x0:0x00000000 x1=0x00000000
570000	0	8000006c	00000113	addi	x2, x0, 0 x0:0x00000000 x2=0x00000000
590000	0	80000070	800001b7	lui	x3, 0x800000 x3=0x80000000
610000	0	80000074	fd135237	lui	x4, 0xfd135 x4=0xfd135000
630000	0	80000078	c1820213	addi	x4, x4, -1000 x4:0xfd135000 x4=0xfd134c18
650000	0	8000007c	f46ab2b7	lui	x5, 0xf46ab x5=0xf46ab000
670000	0	80000080	4c128293	addi	x5, x5, 1217 x5:0xf46ab000 x5=0xf46ab4c1
690000	0	80000084	80000337	lui	x6, 0x800000 x6=0x80000000
710000	0	80000088	f46ab3b7	lui	x7, 0xf46ab x7=0xf46ab000

Figure 4.1: Test 3: Tracer Core Snapshot

4.2 Simulation Output Log

The Tracer IP log from Test 3 provides detailed feedback on instruction execution, identifying mismatches and confirming correct operations for most of the instructions.

```

File Edit View Search Terminal Help
Sep 20 2024
cc@ncdc-0046sim

mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,4): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/AMBIT' (cds.lib command ignored).
DEFINE vital_memory ./VITAL_MEMORY
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,5): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/VITAL_MEMORY' (cds.lib command ignored).
DEFINE ncutils ./NCUTILS
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,6): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/NCUTILS' (cds.lib command ignored).
DEFINE ncinternal ./NCINTERNAL
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,7): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/NCINTERNAL' (cds.lib command ignored).
DEFINE ncmmodels ./NCMODELS
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,8): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/NCMODELS' (cds.lib command ignored).
DEFINE xmutils ./XMUTILS
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,9): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/XMUTILS' (cds.lib command ignored).
DEFINE xminternal ./XMINTERNAL
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,10): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/XMINTERNAL' (cds.lib command ignored).
DEFINE xmmmodels ./XMMODELS
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,11): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/XMMODELS' (cds.lib command ignored).
DEFINE cds_assertions ./CDS_ASSERTIONS
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,12): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/CDS_ASSERTIONS' (cds.lib command ignored).
DEFINE cds_inhconn ./CDS_INHCONN
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,13): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/CDS_INHCONN' (cds.lib command ignored).
DEFINE cds_spicelib ./CDS_SPICELIB
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,14): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/CDS_SPICELIB' (cds.lib command ignored).
DEFINE cds_amsfunctons ./CDS_AMSFUNCTONS
|
mshin: "W.DLCPTH (/home/cc/mnt/XCELIUM2309/tools/inca/files/cdsvhdl.lib,15): cds.lib Invalid path '/home/cc/mnt/XCELIUM2309/tools/inca/files/CDS_AMSFUNCTONS' (cds.lib command ignored).
xcelium run
Loading snapshot worklib top 1b:sv ..... Done
xcelium> source /home/cc/mnt/XCELIUM2309/tools/xcelium/files/xmsinc
xcelium> run
top 1b-dut-tracer ip-printbuffer dumpline.unsblkl: Writing execution trace to trace_core_000000000.log
Simulation complete via $finish() at time 100000020 ns + 0
./Z01b base iss_cpu.vv:62 $finish();
xcelium> exit
TOOL: xrun(64) 23.09-s886: Exiting on Sep 20, 2024 at 20:16:34 PKT (total: 00:00:03)
mshin[1]: Leaving directory /home/cc/amsim
cp: missing destination file operand after 'trace_core_000000000.log'
Try 'cp --help' for more information.
Fri, 20 Sep 2024 20:16:55 INFO Processing spike log : riscv_arithmetic_basic_test.0.log
Fri, 20 Sep 2024 20:16:55 INFO Processed instruction count : 9995
Fri, 20 Sep 2024 20:16:55 INFO CSV saved to : iss.csv
iss : iss.csv
core : core.csv
73 instructions left in trace core
[FAILED]: 8270 matched, 73 mismatch
cc@ncdc-0046 sim$

```

Figure 4.2: Test 3: Tracer Simulation Output Log

Chapter 5

Conclusion

The verification of the RISC-V single-cycle processor was conducted through three tests. Test 1 validated basic instructions, Test 2 focused on memory and branching, and Test 3 provided a complete execution trace. While a few mismatches were detected, the majority of the instructions executed correctly, demonstrating the overall functionality of the processor.