Contents

Chapter 1

Introduction

This report presents the results of RISC-V single-cycle processor verification through three distinct tests. Each test assesses the processor's performance with different sets of instructions, validating the core's functionality and identifying mismatches. The verification uses Cadence Xcelium simulation and includes Tracer IP integration to compare results with reference outputs.

Chapter 2

Test 1: Basic Instruction Verification

The first test focused on validating basic RISC-V instructions, including arithmetic and memory operations.

2.1 Data Memory Waveform

The following figure shows the data memory waveforms captured during Test 1.

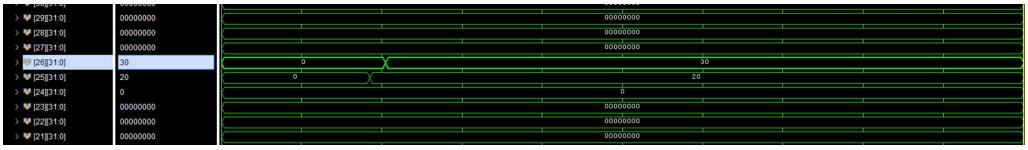

Figure 2.1: Test 1: Data Memory Waveform

2.2 Register File Waveform

The register file contents during the execution of Test 1 are shown below. This verifies the correct write-back behavior of the processor.

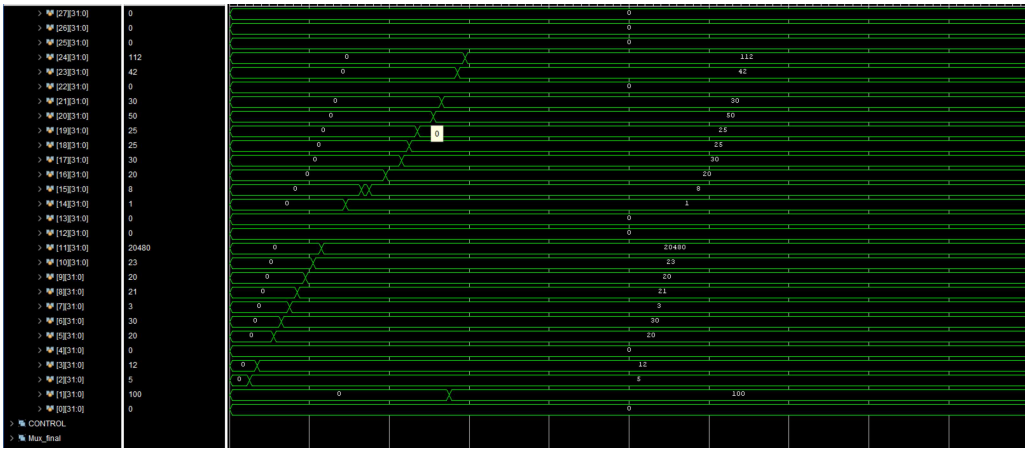

Figure 2.2: Test 1: Register File Waveform

Chapter 3

Test 2

Test 2 focused on verifying memory operations such as loads and stores, along with branching instructions.

3.1 Data Memory Trace

The trace of data memory operations is shown below, highlighting memory writes and reads.

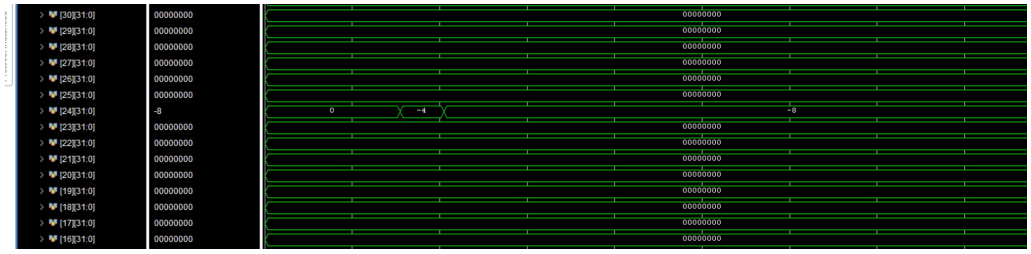

Figure 3.1: Test 2: Data Memory Trace

3.2 Register File Trace

The following figure shows the register file state during Test 2. This helps verify whether the branching instructions update the registers correctly.

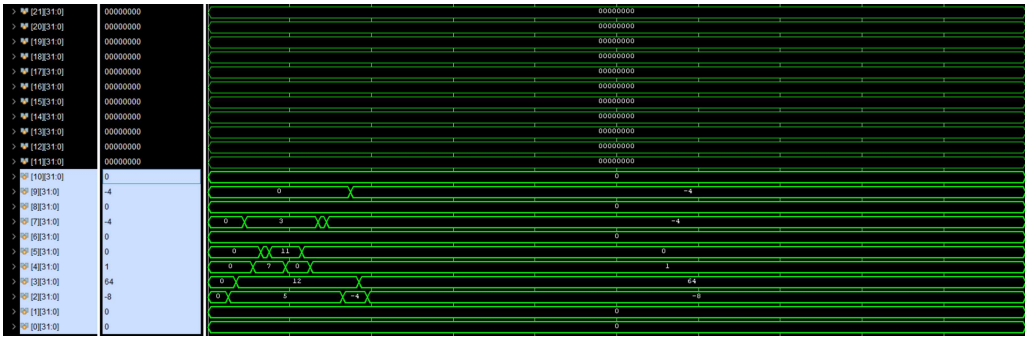

Figure 3.2: Test 2: Register File Trace

Chapter 4

Test 3: Full Execution Trace

Test 3 included a full execution trace captured by the Tracer IP to verify the correctness of control flow and data operations in the processor.

4.1 Tracer Core Snapshot

The following snapshot from the Tracer core shows the instruction execution and comparison with reference values.

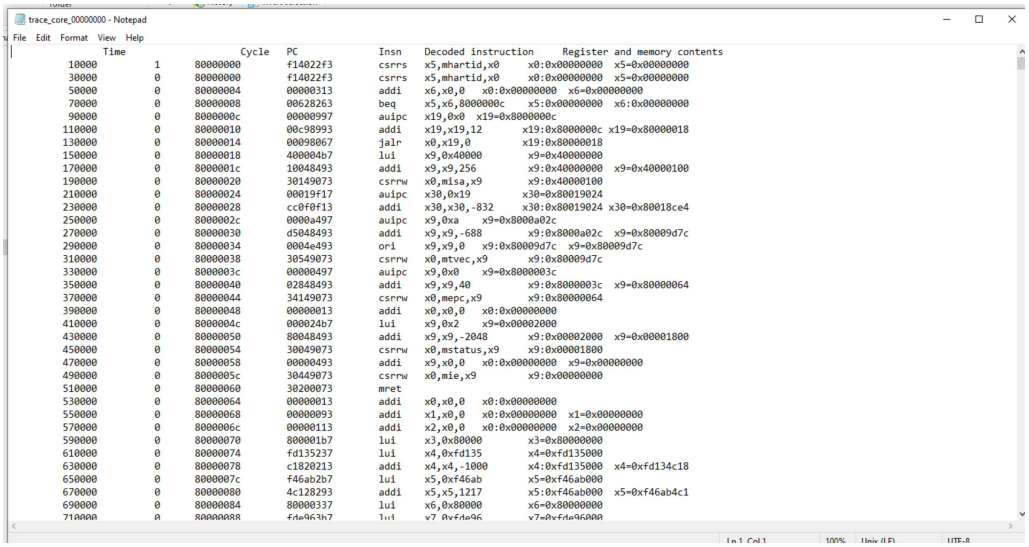

Figure 4.1: Test 3: Tracer Core Snapshot

4.2 Simulation Output Log

The Tracer IP log from Test 3 provides detailed feedback on instruction execution, identifying mismatches and confirming correct operations for most of the instructions.

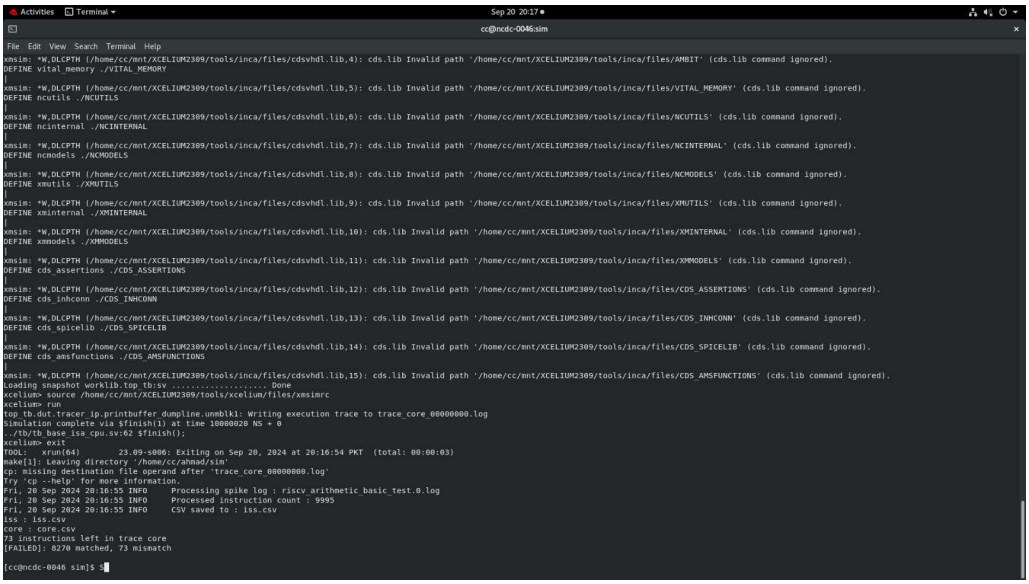

Figure 4.2: Test 3: Tracer Simulation Output Log

Chapter 5

Conclusion

The verification of the RISC-V single-cycle processor was conducted through three tests. Test 1 validated basic instructions, Test 2 focused on memory and branching, and Test 3 provided a complete execution trace. While a few mismatches were detected, the majority of the instructions executed correctly, demonstrating the overall functionality of the processor.