# Experiment 3

# Combinational Circuits: Structural Modeling using Vivado

1.(a) Truth Table:

| a | b | c | x | y |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

1.(b) Maximum combinational delay:

Maximum combinational delay from c to x is 9.018.

Maximum combinational delay from b to y is 8.224

1.(c) Resource Utilization:

LUTs: 1

I/Os: 5

2. code:

```verilog
module task2(input a,b,c,
        output x,y
        );
    assign y = ((~(a&b))^(a|b))&(a|b);
    assign x =  (a|b)^(~c);

endmodule
```