1 Introduction (Informative)

The word *Architecture* is an overloaded term much favored by marketing organizations.   In the TimeCard context, there are two important complementary technical definitions.

At the *system* level (a level above both hardware and software implementation details), the *Architectural Principles* are a set of black-box qualities or properties et al that the system in question must exhibit or possess.

At the *hardware* and *software* level, the *Architectural Constraints* are a set of often interacting constraints and driving requirements that will be analyzed in context to find the best way to implement the Architectural Principles using what's available in practice.

2 What is an Architecture? (Informative)

An *architecture* is a set of principles and objectives that do not directly or indirectly require any specific design or set of design choices.

An architecture defines a set of black-box properties of a TimeCard that are verifiable without looking within, so one can think of the design being such that the TimeCard behaves *as if* the actual design were that implied by the specific architecture used as an example.

3 Architectural Constraints (Normative)

Timestamps **shall** support a mathematical *distance metric*, so algebraic differences in timestamp values will yield precise durations, despite, for example, efforts to smooth over (smear) step discontinuities of time such as leap seconds.

Where PTP is used as an incoming time reference, TimeCard **shall** work correctly with PTPv2.1 (1588-2019) Mixed Multicast Unicast Operations "Hybrid" mode. Hybrid mode may work with PTPv2 (1588-2008) as well, but this is not required.

The TimeCard standard **shall** itself be structured such that widely used legacy TimeCard units automatically conform, allowing direct replacement of old by improved new TimeCards without requiring hardware changes in the host system being provided with time reference signals. Application and operating system software changes are acceptable, being an expected part of the upgrade project. << Needs a better description of acceptable changes. >>

A TimeCard **shall** have at least one time-reference input connector (perhaps fed from a local primary reference source such as a Cesium-Beam Primary Reference Standard or a non-standard Radio Clock of some kind.

A TimeCard **shall** have at least one time-reference output, which can be physical (like a coaxial cable or a twisted pair or an optical fiber carrying a 1PPS pulse train or a sinewave or an IRIG signal, et al), and/or logical (like a register map accessed via the PCIe hardware bus interface).

Practical TimeCards require pre-conditioning and warmup time before the first usable signal is generated and when full performance is achieved. Both the maximum time to first usable signal and the maximum time to full performance **shall** be specified, measured from application of power.

38 The maximum time required to achieve specified performance after resynch due to an abrupt
39 change of a pre-specified kind, including step discontinuities in incoming time references such as
40 during a fail-over event, **shall** be specified.

41 Bridging step discontinuities implies the ability to command a time step before re-closing the
42 PLL control loops, so we don't have to wait for hours while the PLL slowly slews, or just gives
43 up because the needed jump is too large. The capability to change the PLL loop time constant
44 without resetting the loop-filter integrator **shall** be provided. << Modeled on the Datum model
45 1050 Disciplined Oscillator, which switches the feedback resistor value to change the time
46 constant, leaving the charge in the capacitor unchanged. >>

47 Required stability and graceful autonomous handling of overloads and subsequent recovery
48 when overloads subside and cease **shall** be provided.   << Needs more precise wording. >>

49 Support for traceability verification analysis [G8260] of systems utilizing one or more TimeCard
50 units **shall** be provided. This implies that all data needed to perform traceability analysis is
51 publicly available.   << Traceability is more loosely defined in IEEE 1588v2.1 and so in P3335
52 we will update this generic definition. >>

53 Above are universal constraints, while what follows varies by specific use case. Requirements
54 must be phrased as Optional Shalls: If <statement or condition is true> then <shall is imposed>.

55 Typical constraints also include: The requirement to adhere to specified, often legacy IDDs.
56 Required use of a specific computer platform. Lack of memory space or processing capacity in
57 the specified computer platform. Inadequate scalability.

58 4   TimeCard Architecture (Normative)

59 A TimeCard is a set of functions, interface definitions[1], and TimeCard behaviors, not necessarily
60 implemented as a tangible physical object. For instance, a TimeCard may be implemented as a
61 function of some kind within an FPGA, ASIC, or SoC in a system that requires a time reference
62 but is not itself a time reference or clock.

63 4.1   Architectural Principles (Normative)

64 Qualities sought include *adequately* high stability (quantified using ADEV or TDEV or MTIE as
65 appropriate), low phase noise, high accuracy, high precision, fine granularity, high resolution,
66 ability to synchronize TimeCard instances over a specified large physical extent while meeting
67 some pre-specified performance requirements, ability to create Ensemble clocks from multiple
68 time reference inputs, et al. The definition of *adequately* depends on the relevant use cases.

69 A TimeCard generates a single unified timescale and may publish this simultaneously in multiple
70 forms. There is exactly one timescale, not one per reference signal output.

71 All outputs **shall** publish the single *unified* timescale, approximating the timescale's ideal to fit
72 the capabilities of the output media. A major implication is that the boundaries between seconds
73 seen on the various output media from the same TimeCard instance always align exactly.

74 In addition to stability requirements, there are often maximum Phase Noise (PN) requirements.
75 PN is very weak amplitude (AM) and/or phase modulation (PM) of a periodic carrier whose

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[1] If not defined within the present standard, interface definitions are usually incorporated by normatively citing a set
of formally approved IDDs standards. This is needed for interoperability spanning various TimeCard makes and
models.

76 frequency exceeds about one megahertz. While PN is not defined for slow pulse trains like
77 1PPS, time jitter is defined. PN is specified as a pair of power spectra of some kind (covering
78 AM and PM, if both are important) versus offset frequency. Each reference signal output will
79 likely have its own PN spectrum.

80 Low SWaP and cost (either absolute or relative to the host system being served, as appropriate
81 for specific use cases).

82 Manufacturers will be required to measure and publish their guaranteed maximum holdover
83 errors as a function of holdover time, along with required minimum warmup conditions and
84 times, et al. Holdover requirements apply only to 1PPS outputs and assume that the chosen
85 incoming reference is perfect. MTIE is widely used

86 The ITU G810 Appendix II.5 definition [G8260] of MTIE **shall** be the holdover metric for
87 TimeCards.

88 Alternately, multiple independent incoming time-reference signals may be combined into a
89 single unified *ensemble* time-reference signal that may be chosen as an incoming time reference.

90 TimeCard implementations **shall** be capable of combining multiple incoming reference signals
91 into a single unified *Ensemble* reference signal that may be used in the same manner as an
92 individual reference signal.

4.2   What's Common to all Implementations (Informative)
94 The architecture, constraints, and interfaces are common to all TimeCard implementations; all
95 else can vary. TimeCard implementations need not support all architecture objectives and/or
96 constraints. Manufacturers will specify exactly what they do and do not offer, and customers
97 will choose those offerings that best suit their specific application use case or cases.

98 In some use cases, the sole purpose of the TimeCard is to provide a standard interface to provide
99 a time reference to bespoke hardware, often with minimal to no technical requirements.

100 Cost sensitivity varies by orders of magnitude. One size does not fit all. So, numerical
101 performance requirements are explicitly defined as *unspecified* in the standard, meaning that the
102 WG deliberated and decided to leave this issue to the market to segment and settle[2].

103 Although we usually think of an oscillator as being a physical object perhaps containing a very
104 good resonator of some kind, this is not necessarily true in a TimeCard. For some use cases, a
105 DDS implemented in FPGA firmware controlled by a low-end commodity digital logic clock or
106 a wristwatch crystal oscillator or the like suffices.

107 TimeCards are a kind of PTP "Ordinary Clock".

4.3   Time-Flow Narrative (Informative)
109 The following is an informative traversal narrative, proceeding from the time-inputs to the time-
110 outputs in the direction of reference-time flow:

111   There is at least one input time reference signal available, and there may be multiple
112 simultaneously connected and available time references. If more than one signal is available,
113 there will be a pre-configured scheme to select which signal to use, what to do if and when the

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[2] *Unspecified* will be formally defined in the Nomenclature section of the P3335 standard. Also, officially define "out of scope", and update the definition of Traceable and Optional (conditional) Shall.

114 chosen reference signal degrades or ceases, and just how fussy and impatient to be in this
115 decision.

116 A TimeCard may have its own integral or dedicated Primary Reference Clock oscillator and
117 have no need of any incoming time reference, so the earlier rule would change to zero or more
118 incoming time reference signals. More commonly, there could be an ensemble clock
119 implemented where the local Primary Reference provides phase and frequency, plus external
120 incoming reference signals that define the boundaries between adjacent SI Seconds and label
121 those seconds according to TAI or UTC or some other time scale.

122 The TimeCard's internal Hardware Clock is steered into synchronism with the chosen incoming
123 time reference signal using a PLL of some kind; details vary, as does how tightly the PLL
124 synchronizes to the chosen incoming time reference, and the specific PLL type and loop
125 bandwidth. Knowledge of the specific PLL Type and Loop Bandwidth is necessary for the
126 design of the embedding system. Loop bandwidths range from millihertz (very loose
127 synchronization) to tens of kilohertz (very tight synchronization).

5 Documentation Requirements (Normative)

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129 Many Architectural Principles and Constraints are optional, which ones to support being left to
130 the market on the theory that customers will choose what's best for them. This implies that the
131 necessary data for publicly available products must be freely available to the public.

132 Manufacturers **shall** specify in publicly available datasheets exactly which of the listed
133 Architectural Principles and Constraints they do and do not meet or implement.

134 Manufacturers **shall** specify in publicly available datasheets the PLL Type and Loop Bandwidth.

135 Manufacturers **shall** provide in publicly available documents all data needed to perform
136 traceability analysis, or state that traceability is not supported.

137 All exercised optional (conditional) requirements **shall** be documented.

6 References (Normative)

138
139 [G8620] ITU-T G.8260 "Definitions and terminology for synchronization in packet networks"
140 and especially "Definitions and terminology for synchronization in packet networks –
141 Amendment 2", both 2015 issue or later. Available gratis.
142 <https://www.itu.int/en/Pages/default.aspx>.

143 [IEEE 1139] "IEEE Standard Definitions of Physical Quantities for Fundamental Frequency and
144 Time Metrology" – defines ADEV and TDEV.

145 [MTIE] "Measurement of Maximum Time Interval Error for Telecommunications Clock
146 Stability Characterization", Stefano Bregni, IEEE Transactions on Instrumentation and
147 Measurement, Vol. 45, No. 5, October 1996, pages 900-906. Cites ITU G810 "Definitions and
148 terminology for synchronization networks", Appendix II.5 "Maximum Time Interval Error
149 (MTIE)".

150 [PTPv2.1] IEEE 1588-2019 "Precision Time Protocol"

7 Bibliography (Informative)

151
152 < https://en.wikipedia.org/wiki/Precision_Time_Protocol>

153   ComSoc article on PTP? << Need precise cite. >>

154   [IRS_DID] DI-IPSC-81434A, "Interface Requirements Specification – Data Item Description",
155   approved 1999-12-15, 20 pages. This defines the kinds of data that are required, but leaves their
156   detailed format to design. DIDs may be obtained gratis from the US Defense Acquisition
157   University website <https://www.dau.edu/> by searching for "DI-IPSC" (without quotes).

158   [IDD_DID] DI-IPSC-81436A, "Interface Design Description – Data Item Description",
159   approved 1999-12-15, 6 pages. This defines the exact format – what every bit means and
160   exactly where it is located. This is essential for interoperability between various TimeCard
161   makes and models.

162   [SSDD] DI-IPSC-81432A, "System/Subsystem Design Description", approved 10 August 1999,
163   9 pages. The SSDD describes the system- or subsystem-wide design and the architectural design
164   of a system or subsystem.

165   [SSS] DI-IPSC-81431A, "System/Subsystem Specification", approved 1 October 2000,
166   11 pages. The SSS specifies the requirements for a system or subsystem and the methods to be
167   used to ensure that each requirement has been met.

168   8   Notes
169   The present P3335 standard formal text document was started on 25 April 2025, largely based on
170   "TimeCard Architecture (Section 5) Draft (20250424).docx".

171   9   Acronyms
172   **1PPS** = One Pulse Per Second, **ADEV** = Allen Deviation, **AM** = Amplitude Modulation, **ASIC**
173   = Application Specific Integrated Circuit, **DDS** = Direct Digital Synthesis, **FPGA** = Field
174   Programmable Gate Array, **GHz** = Gigahertz (10^9 Hz), **IDD** = Interface Definition Document
175   [IDD_DID], **IRIG** = Inter-Range Instrumentation Group, **IRS** = Interface Requirements
176   Specification [IRS_IDD], **ITU** = International Telecommunications Union, **MTIE** = Maximum
177   time interval error, **PCIe** = Peripheral Component Interconnect - Express, **PLL** = Phase Locked
178   Loop, **PM** = Phase Modulation, **PN** = Phase Noise, **PTP** = Precision Time Protocol [PTPv2.1],
179   **RT** = Radar Time, **SI** = International Metric System (French abbreviation), **SoC** = System on a
180   Chip, **SSDD** = System/Subsystem Design Document (DI-IPSC-81432A), **SWaP** = Size, Weight
181   and Power, **TAI** = International Atomic Time (French abbreviation), **TC** = PTP Transparent
182   Clock, **TDEV** = Time Deviation, **UTC** = Coordinated Universal Time (French abbreviation),
183   **WG** = Working Group