TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7W14F, TC7W14FU

SCHMITT INVERTER

The TC7W14 is high speed C²MOS SCHMITT INVERTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.

Pin configuration and function are the same as the TC7WU04 but the inputs have 25% V_{CC} hysteresis and with its schmitt trigger function, the TC7W14 can be used as a line receivers which will receive slow input signals.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

•	High Speed	 	 $t_{pd} = 11ns$	(Typ.)	at
			V _{CC} = 5V		

• Low Power Dissipation $I_{CC} = 1\mu A$ (Max.) at

• High Noise Immunity $V_H = 1.1V$ at

 $V_{CC} = 5V$

Output Drive Capability 10 LSTTL Loads

Symmetrical Output Impedance ... |IOH| = IOL = 4mA

• Balanced Propagation Delays $t_{pLH} = t_{pHL}$

• Wide Operating Voltage Range ... $V_{CC(opr)} = 2\sim 6V$

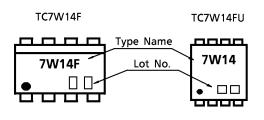
SSOP8-P-0.65

Weight SOP8-P-1.27 : 0.05g (Typ.) SSOP8-P-0.65 : 0.02g (Typ.)

MAXIMUM RATINGS (Ta = 25°C)

	,		
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	Vcc	-0.5~7	٧
DC Input Voltage	VIN	-0.5~V _{CC} +0.5	٧
DC Output Voltage	VOUT	-0.5~V _{CC} + 0.5	V
Input Diode Current	ΙΚ	± 20	mA
Output Diode Current	^I ок	± 20	mΑ
DC Output Current	IOUT	± 25	mΑ
DC V _{CC} /Ground Current	lcc	± 25	mΑ
Power Dissipation	PD	300	mW
Storage Temperature	T _{stg}	- 65∼150	°C
Lead Temperature (10s)	TL	260	°C

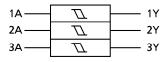
MARKING



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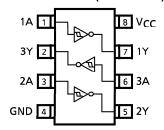
LOGIC DIAGRAM



TRUTH TABLE

Α	Υ
L	Н
Н	L

PIN ASSIGNMENT (TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	Vcc	2~6	V
Input Voltage	VIN	0~V _{CC}	V
Output Voltage	VOUT	0~V _{CC}	V
Operating Temperature	T _{opr}	- 40∼85	°C

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL TEST CONDITION				Т	a = 25°	C	Ta = -40~85°C		UNIT
CHARACTERISTIC	STIVIBUL	1531	CONDITION	Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Positive Threshold					1.0	1.25	1.5	1.0	1.5	,,
Voltage	V _P		_	4.5 6.0	2.3 3.0	2.7 3.5	3.15 4.2	2.3 3.0	3.15 4.2	\
	1			2.0	0.3	0.65	0.9	0.3	0.9	
Negative	$ v_N $		_	4.5	1.13	1.6	2.0	1.13	2.0	V
Threshold Voltage	'-			6.0	1.5	2.3	2.6	1.5	2.6	
				2.0	0.3	0.6	1.0	0.3	1.0	
Hysteresis Voltage	∣ ∨ _H		_	4.5	0.6	1.1	1.4	0.6	1.4	V
	''			6.0	0.8	1.2	1.7	0.8	1.7	
		4 VIN=VIL		2.0	1.9	2.0	_	1.9	_	
High Loyal			$I_{OH} = -20\mu A$	4.5	4.4	4.5	—	4.4	—	
High-Level Output Voltage	VOH			6.0	5.9	6.0	_	5.9	_	v
Output Voltage			$I_{OH} = -4mA$	4.5	4.18	4.31	—	4.13	—	
			$I_{OH} = -5.2$ mA	6.0	5.68	5.80	_	5.63	_	
				2.0	_	0.0	0.1	<u> </u>	0.1	
Low-Level			$I_{OL} = 20 \mu A$	4.5	—	0.0	0.1	_	0.1	
Output Voltage	VOL	$V_{IN} = V_{IH}$		6.0	_	0.0	0.1		0.1	V
Catput Voltage			$I_{OL} = 4mA$	4.5	—	0.17	0.26	_	0.33	
			I _{OL} = 5.2mA	6.0	_	0.18	0.26	_	0.33	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} o	or GND	6.0			± 0.1	1	± 1.0	
Quiescent Supply Current	lcc	V _{IN} = V _{CC} o	or GND	6.0	_	_	1.0	_	10.0	μ Α

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AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
CHARACTERISTIC	STIVIBUL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition	tTLH			1	۰	nc
Time	tTHL	_		4	°	ns
Propagation Delay	t _{pLH}			11	21	200
Time	t _{pHL}	_	_	11	21	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

CHARACTERISTIC	SYMBOL	TEST CONDITION VCC		Т	a = 25°C		Ta = −40~85°C		UNIT
CHARACTERISTIC	3 I WIBOL			MIN.	TYP.	MAX.	MIN.	MAX.	OIVII
Output Transition	t		2.0	_	30	75	_	95	
Time	t _{TLH}	_	4.5	<u> </u>	8	15	_	19	ns
Time	^t THL		6.0	—	7	13	_	16	
Brangation Dalay	4		2.0	_	42	125	_	155	
Propagation Delay	t _{pLH}	_	4.5	l —	14	25	—	31	ns
Time	грн <u>г</u>	трнг	6.0	—	12	21	—	26	
Input Capacitance	CIN	_		_	5	10	_	10	
Power Dissipation Capacitance	C _{PD}	(Note 1)		_	28	_	_	_	pF

Note 1 : CpD is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder. $ICC(opr) = CPD \cdot VCC \cdot fIN + ICC / 2$ (per gate)