Flash ChipSet
Product Manual

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- *Revisions before Rev. 5—initial release and general changes.*
- *Revision 5—general editorial changes, new model numbers to reflect HDII controller and ChipSet on tape reels, new caution label, new inner and outer packaging drawings, two MB ChipSet removed.*

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1.0 Introduction

The SanDisk Flash ChipSet (FCS) consists of two chips: a highly integrated flash controller chip and a flash memory chip in a TSOP (thin small outline package). The FCS complies with the Personal Computer Memory Card International Association ATA (PC Card ATA) standard. (In Japan, the applicable standard group is JEIDA.) The FCS also supports the ANSI ATA (True IDE) drive interface.

This SanDisk Flash ChipSet controller is designed specifically for use as a Flash mass storage controller for the SanDisk Flash Memory devices. This interface allows a host computer to issue commands to read or write blocks of memory in the Flash memory array. The intelligence to manage the interface protocols, data storage and retrieval as well as ECC, Defect handling and diagnostics are controlled by this device. Automatic power management and clock control is handled by this controller as well.

The user designing a system with the Flash ChipSet will have the same functionality and capabilities of an intelligent ATA (IDE) disk drive. An advantage of this controller and its ATA command set is the ease of software development by the user. Once the device has been configured by the user (if in PCMCIA mode) it appears to the host as a standard ATA disk drive. Additional ATA commands have been provided to enhance system performance.

The Flash ChipSet controller is a highly integrated solution that is packaged in a 100 pin TQFP plastic package. This ASIC controller is designed to handle all intelligent operations, even the rare cases when new defects arise and need to be mapped out or replaced by a spare. The hardware performs the complicated task of ECC detection and correction and will return good data to the host. The controller manages all defects and errors and makes the Flash memory appear as perfect memory to the host.

1.1 Scope

This specification describes the key features and specifications of the SanDisk Flash ChipSet as well as the information required by an engineer to interface this product to a host system.

1.2 System Features

- PC Card ATA compatible—memory mapped or I/O operation
- Supports True IDE Mode
- Very low CMOS power
- +5 V± 10% or 3.3 V± 5% operation
- Very High Performance
- Supports Pre-Erase and Write without Erase Commands to effectively double write performance
- Supports programmable power
- Small controller package, 100 pin TQFP (14x14)
- 68000 processor built into the controller
- Two 512 Byte ping-pong data buffers
- Powerful Risc controller built in for real time control
- 50 bit Reed Solomon ECC
- Built in power-on reset circuit
- Automatic error correction and retry
- Automatic Sleep Mode
- Non-volatile storage

1.3 Industry Standards

The Flash ChipSet is fully compatible with the industry standards listed below. These standards can be obtained from the addresses listed below.

1. **American National Standard for Information Systems—AT Attachment Interface for Disk Drives, ANSI X3.221-1994.**
   Published by:
   American National Standards Institute,
   11 West 42nd Street,
   New York NY 10036.

2. **PC Card Standard - May 1996.**
   Published by:
   PCMCIA (Personal Computer Memory Card International Association)
   2635 North First Street
   San Jose CA 95134 USA
   Phone: +1-408-433-2273
   Fax: +1-408-433-9558
   E-Mail: office@pcmcia.org

   The PC Card Standard is also published by:
   JEIDA (Japan Electronic Industry Development Association)
   Kikai Shinko Kaikan, 3-5-8, Shibakoen
   Minato-ku, Tokyo 105, Japan
   Phone: +81-3-3433-1923
   Fax: +81-3-3433-6350

1.4 System Block Diagram

In the following block diagram you can see that the SanDisk controller chip is the heart of this design. This controller chip interfaces with the host system and the SanDisk flash memory chip.

This block diagram also shows an external switch used to isolate the flash memory's supply line from the host's supply. This reduces the sleep mode current drain to the absolute minimum when the memory is not being accessed.

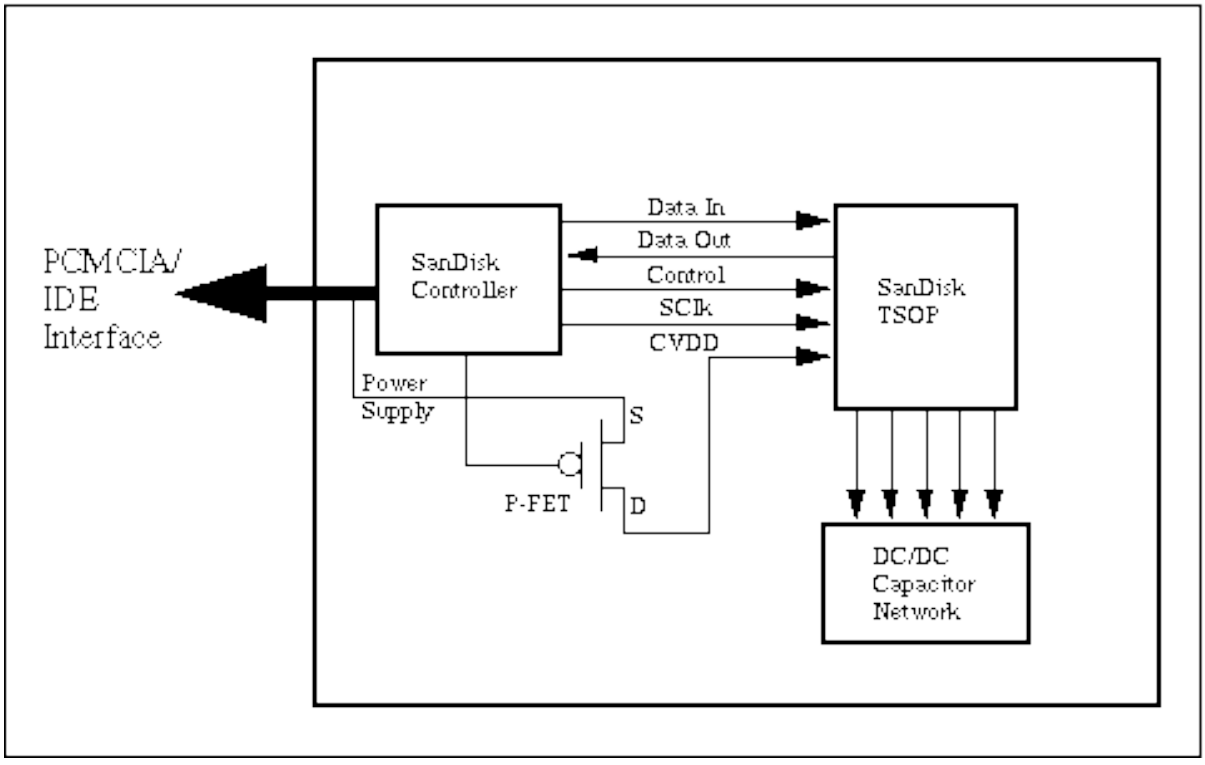


Figure 1-1 Flash ChipSet System Block Diagram

1.5 Flash ChipSet Controller Block Diagram

The following block diagram shows the major sections within the SanDisk 100 pin Flash ChipSet Controller.

The Clock and Reset block are responsible for the initial power-on reset and main clock control functions within the device. The clock generator interfaces with an external R-C circuit.

The PCMCIA/ATA block provides all the functionality required to interface to a PCMCIA host in either memory or I/O mode. It also provides the host with a path to the 192 byte CIS RAM array used to store the Card Information Structures. If configured to be in True IDE Mode, this block will be compatible with the standard ATA/IDE protocol.

The 68000 Core CPU block is a completely static microcomputer used to initialize and control the entire system.

The ROM block is a 22K by 16 bit mask ROM used for all 68000 CPU program instruction fetches.

The Buffer Memory and DMA blocks are used for all real time data transfers between the Host Interface and the buffer memory and the Flash Interface and the buffer memory.

The Sequencer block is a dedicated RISC state machine used for all real time command and control of the SanDisk Flash Memory.

The ECC and Defect Handling blocks contain the hardware required to guarantee data integrity/reliability for all real time data transfer to and from the SanDisk Flash Memory.

The Flash Control block contains all the hardware drivers and receivers along with the random logic required to interface with the SanDisk Flash memory.

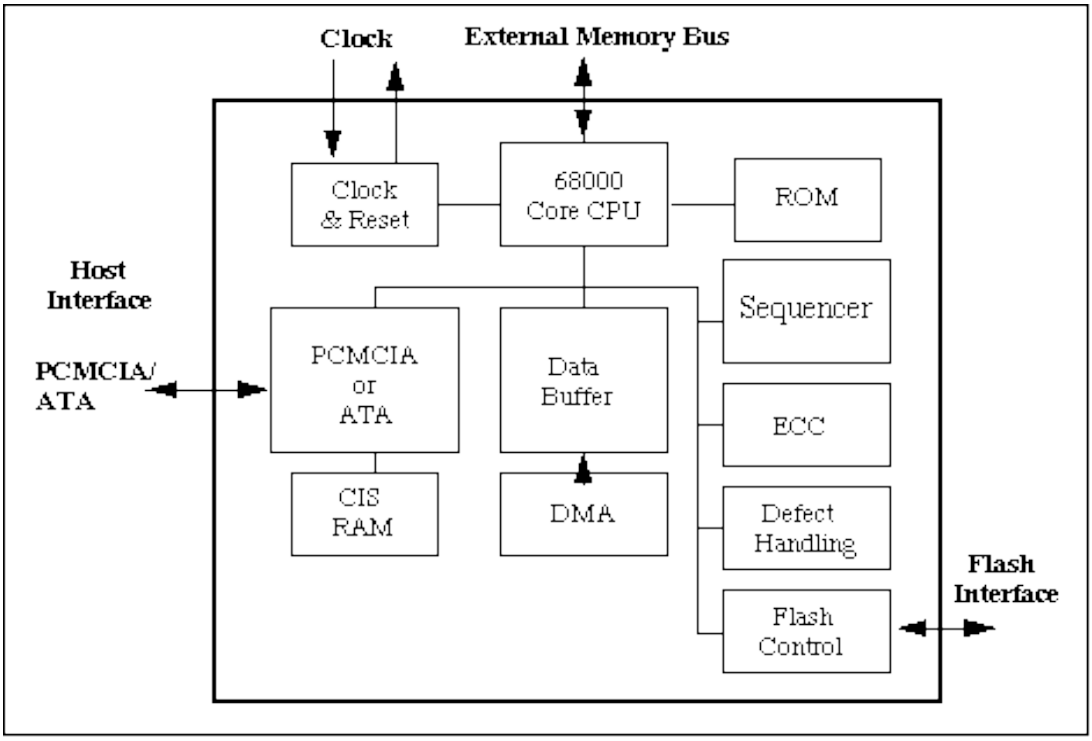


Figure 1-2 Flash ChipSet Controller Block Diagram

1.6 True IDE Mode

The SanDisk Flash ChipSet operates in both the True IDE Mode (68-pin ATA mode) and PC Card ATA mode. The True IDE Mode allows PCMCIA storage devices to be booted from a standard IDE BIOS software driver, identical to a standard IDE hard drive. This eliminates the need for special PCMCIA software and controllers.

Note: The 68-pin ATA mode (True IDE Mode) is defined by the Small Form Factor (SFF) Committee and is not part of the PCMCIA Standard. The SFF Committee can be contacted at 408-867-6630. The 68-pin ATA document can be acquired from Global Engineering at 800-854-7179.

In this manual, 68-pin ATA mode will be referred to as “True IDE Mode.”

1.6.1 Enabling True IDE Mode

True IDE Mode is enabled by the host grounding pin 40 (-OE) of the controller during the power-off to power-on cycle.

Refer to Table 4-1 for pin assignments and type. Refer to Table 4-2 for signal descriptions for both PC Card ATA mode and True IDE Mode.

Note: When designing products using the Flash ChipSet in True IDE Mode and removable applications, it is recommended that power be applied to the socket after the removable device with FCS is inserted and that power be removed from the socket when the removable device with FCS is removed. This can be accomplished by monitoring the card detect pins (-CD1 and -CD2) and controlling an FET (Field Effect Transistor) that switches Vcc on or off depending on the state of the card detect pins.

2.0 Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltages unless otherwise stated.

2.1 Flash ChipSet System Environmental Specifications

		Standard Product	Industrial Product (5V only)
Temperature	Operating: Non-Operating:	0° C to 70° C -25° C to 85° C	-40° C to 85° C -50° C to 100° C
Humidity	Operating: Non-Operating:	8% to 95%, non-condensing 8% to 95%, non-condensing	8% to 95%, non-condensing 8% to 95%, non-condensing
Acoustic Noise:		0 dB	0 dB
Altitude (relative to sea level)	Operating: Non-Operating:	80,000 feet maximum	80,000 feet maximum

2.2 Flash ChipSet System Power Requirements

		5 Volt	3.3 Volt
DC Input Voltage (VCC) 100 mV max. ripple (p-p)	**Standard Product**	5V ±10%	3.3V ±5%
	Industrial Product	5V ±5%	3.3V ±5%
+5 V Currents (maximum Average value) See Notes 1 to 3.	Sleep: Reading: Writing:	< 0.5 mA (Slow - Fast) 46 mA - 75 mA 46 mA - 90 mA	< 0.2 mA (Slow - Fast) 32 mA - 45 mA 32 mA - 60 mA

Note 1. Sleep mode current is specified under the condition that all Flash ChipSet inputs are at static CMOS levels and in a “Not Busy” operating state.

Note 2. The currents specified show the complete range of programmability in Flash ChipSet. A tradeoff between performance and maximum current used can be done using the Set Features command. The Flash ChipSet defaults to the fastest speed and highest current. See the Set Features command for more details.

Note 3. At maximum performance, typical average Read current is 30 mA at 3.3 volts and typical average write current is 50 mA at 3.3 volts.

2.3 Flash ChipSet System Performance

All performance timings assume the Flash ChipSet controller is in the default (i.e., fastest) mode.

Start Up Times	Sleep to write: Sleep to read: Reset to ready:	2.5 msec maximum 2.0 msec maximum 50 msec typical 400 msec maximum
Active to Sleep Delay		Programmable
Data Transfer Rate To/From Flash		4.0 MBytes/sec burst
Data Transfer Rate To/From Host		6.0 Mbytes/sec burst
Controller Overhead	Command to DRQ	1.25 msec maximum

Note: The Sleep to Write and Sleep to Read times are the times it takes Flash ChipSet to exit sleep mode when any command is issued by the host to when the card is reading or writing. Flash ChipSets do not require a reset to exit sleep mode.

2.4 Flash ChipSet System Reliability and Maintenance

MTBF (@ 25°C)	>1,000,000 hours
Preventive Maintenance	None
Data Reliability	<1 non-recoverable error in 10^{14} bits read
Endurance SDFCSTB (Standard Product)	300,000 erase / program cycles per logical sector guaranteed
Endurance SDFCSTBI (Industrial Product)	100,000 erase / program cycles per logical sector guaranteed

2.5 Flash ChipSet Physical Specifications

Controller Package	100 pin TQFP	Weight: 0.5 gram ± 5%
TSOP Package	56 pin TSOP	Weight: 0.7 gram ± 10%

2.6 Capacity Specifications

The table below shows the specific capacity for the Flash ChipSet models and the default number of heads, sectors/track and cylinders.

Model Numbers	Capacity (formatted)	Sectors/Card (Max LBA+1)	No. of Heads	No. of Sectors/ Track	No. of Cylinders
SDFCSTB-32	4,030,464 bytes	7,872	2	32	123
SDFCSTB-64	8,028,160 bytes	15,680	2	32	245
SDFCSTB-128	16,056,320 bytes	31,360	2	32	490

3.0 Design Options and Considerations

3.1 Host Interface Options

As stated in the introduction, the SanDisk Flash ChipSet controller can be configured to interface to the host in one of several modes. A complete and robust PCMCIA protocol using PC Card ATA memory mode or I/O mode is one option. This option uses 43 signals to interface to the host computer. Another method of interfacing to the host is the True IDE Mode. In this mode the OE pin on the controller is grounded. At power on, the controller automatically configures itself in the True IDE Mode. This mode requires 26 signals to complete the interface. See the schematics in the appendices at the end of this manual for further reference.

In its simplest form, the FCS consists of one controller and one 56 pin TSOP (thin small outline package). At this time, SanDisk is providing the TSOP in a capacity of 4, 8 or 16 megabytes. Schematics in Appendix 2 and 3 show the TSOP configuration. In the future, as memory technology provides for greater densities, memory capacities will increase, but this will have no effect on the host interface design, since the host interface is controlled by industry standards.

It is possible to achieve other memory sizes by using more than one memory device. If this is required, please contact SanDisk Applications Engineering at 408-542-0400 for additional information.

3.2 Choosing the Host Interface

If the application requires dynamic insertion and removal (hot swapping), the obvious choice is PC Card ATA. An example would be a multifunction PC Card including Flash storage plus another function such as a modem. This choice does require a hardware controller and a software driver, plus a certain amount of memory.

Note: When designing for a PC Card ATA host interface with hot swap support, the use of an FET switch to control the socket voltage is recommended. The card detect pins should be monitored and power applied to the socket only upon detecting the card detect signals. Power should be removed from the socket when the card is removed.

In this section, we will concentrate on the IDE interface, since the FCS is most often used in embedded applications, where the components are either soldered onto the main board, or on a daughter board which is plugged into the main board, and removability is not an issue. The IDE interface is very simple, requiring an absolute minimum of hardware and software. In many cases the hardware is built into the host system, and where it is not, it is quite straightforward to implement.

3.3 Hardware Interface

3.3.1 I/O Connector

The schematics at the end of this manual show a 44 pin connector. This is a 2 mm connector used with 2.5 inch and smaller disk drives, as defined by the ATA Small Form Factor Committee. The definitions of the first 40 pins are the same as the standard 40 pin IDE connector. Of course, the user may choose a different connector, or no connector at all.

3.3.2 Signal Definitions

The following signal names are defined in the ATA specification. The names in parentheses are the net names used in the schematics at the end of this manual.

CS1FX- (CE1-) Chip Select 0—This is the chip select signal which selects the Command Register Block.

CS3FX- (CE2-) Chip Select 1—This is the chip select signal which selects the Control Register Block.

DA0-2 (HA0-2) Host Address Bus—This is the 3 bit binary address issued by the host to select one of the registers in the Command or Control Register Block.

DASP- Drive Active/Slave Present—This is a time multiplexed signal which indicates that a drive is active, or a slave is present. See the ANSI ATA specification for details.

DD0-DD15 (HD0-HD15) Host Data Bus—This is the 8- or 16-bit bidirectional bus between the host and the controller.

DIOR- (IORD-) I/O Read—This is the Read Strobe. The falling edge of DIOR- enables 8- or 16-bit data from a register of the controller onto the host data bus. The rising edge of DIOR- latches data into the host.

DIOW- (IOWR-) I/O Write—This is the Write Strobe. The rising edge of DIOW- clocks 8- or 16-bit data from the host data bus into a register on the controller.

DMACK- DMA Acknowledge—Not used. The FCS does not support DMA mode.

DMARQ DMA Request—Not used. The FCS does not support DMA mode.

INTRQ (IRQ) Interrupt request—This signal is used to interrupt the host system. See ANSI ATA specification for details.

IOCS16- 16 bit I/O—When this signal is asserted by the controller, transfers are 16-bit using DD0-15, otherwise transfers are 8-bit using DD0-7.

IORDY I/O Channel Ready—This signal is not used. The FCS meets the timing requirements of PIO modes 0 and 1 without issuing this signal.

PDIAG- Passed diagnostics—This signal is asserted by Drive 1 to indicate to Drive 0 that it has completed diagnostics.

RESET- Drive Reset—This signal from the host is asserted for at least 25 µS after voltage levels have stabilized during power on and negated thereafter unless some event requires that the drive(s) be reset following power on.

CSEL Cable Select—This signal may be used to let the host select the drive address through special cabling which grounds the CSEL signal for drive 0 (master), and leaves CSEL open for drive 1 (slave). If host selection is not used, the CSEL signal should not be connected to the host bus. Instead, ground the CSEL signal at the controller (U1 pin 23) for drive 0 (master) and leave it open for drive 1 (slave). See JP1 in the schematics.

3.4 Design Notes

3.4.1 Commonly Asked Questions

Q. How is IDE mode selected?
A. Connect U1 pin 40 (OE-) to ground.

Q. How is the unit set to be master or slave?
A. Connect jumper JP1 for a master, leave open for a slave.

Q. What are PIO modes?
A. PIO stands for programmed input/output. Each mode has a different set of timing parameters. The FCS supports modes 0 and 1 only, with minimum cycle times of 600 and 383 nS respectively.

Q. Does the FCS support DMA?
A. No.

Q. Why is IORDY not connected to anything?
A. Please refer to the ANSI specification, page 10. This is an optional signal which is negated when the drive is not ready to respond to a data transfer request. For the FCS, this signal is not used. As long as the host obeys PIO mode 0 or 1 timing, the FCS is guaranteed to respond properly.

Q. Is it necessary to use the FET switch?
A. No. See section 3.4.3 for a discussion of this option.

3.4.2 Oscillator Component Selection

Please refer to the schematic in Appendix 2 for the locations of the components in the following discussion. Resistor R1 and capacitors C11, 12 and 13 are the frequency determining components for the oscillator. The actual values for these components are a function of the layout, which affects the stray capacitance in the circuit. The value of R1 must be between 1.0 and 1.5K. C13 is not used in the current version of the controller, but it is recommended that pads for this capacitor be included in the layout for future use. If the application requires dual voltage operation, C11 is the capacitor used to set the frequency for 5 volt operation, and C12 is automatically switched across C11 for 3.3 volt operation. If the application does not require dual voltage operation, C12 may be omitted, and C11 selected to give the correct frequency at the desired supply voltage. Again, it is recommended that pads for C11 be provided even if it is not used, for future applications. The nominal frequency is 16 MHz at 5 volts, and 10 MHz at 3.3 volts.

See section 3.5.2 for the procedure to determine component values.

3.4.3 Discussion of the Use of the FET Switch Q1 and Associated Capacitors

The purpose of the FET switch is to minimize the current drawn by the FCS during sleep mode by turning off power to the flash memory.

If the FET is used, sleep current to the FCS will be less than 10µA. Otherwise, the maximum sleep current will be less than 500 µA at 5 volts, 200 µA at 3.3 volts, as specified in the product manual. The actual current will depend on the number of memory units used, and is typically 100 µA for a 4 MB memory chip.

If power consumption is not important, the FET switch can be eliminated. See schematic in Appendix 3 for this option. Note that Q1 and C3 have been eliminated and C10 has been changed from a tantalum 1µF to a ceramic .22 µF capacitor.

3.4.4 General PC Board Layout Suggestions

SanDisk recommends that the following PC Board Layout suggestions be followed when designing with the Flash ChipSet:

1. It is recommended, but not mandatory, that a four layer board be used, with all of the components surface mounted on the top layer. The next two layers are ground and power planes respectively, and the bottom layer is used for traces.
2. Keep all traces between the controller and the memory as short as possible.
3. Mount bypass capacitors as close as possible to the power pins that are being bypassed. Please refer to Figure 3-1 for a recommended layout method for bypass capacitors. Where more than one pin is to be bypassed by a single capacitor, isolate the power plane around those pins, and connect the isolated section to the main power plane at one point.

Table 3-1 Relationship Between Capacitors and Device Pins to be Bypassed

Schematic	Capacitor	Pins to be Bypassed
2 and 3	C1	U1 pins 56, 65 and 88
2 and 3	C2	U1 pins 5, 15 and 38
2	C3	Q1 source
2 and 3	C4	TSOP_1 pin 1
2 and 3	C16	TSOP_1 pin 56
2 and 3	C10	J1 pins 41 and 42

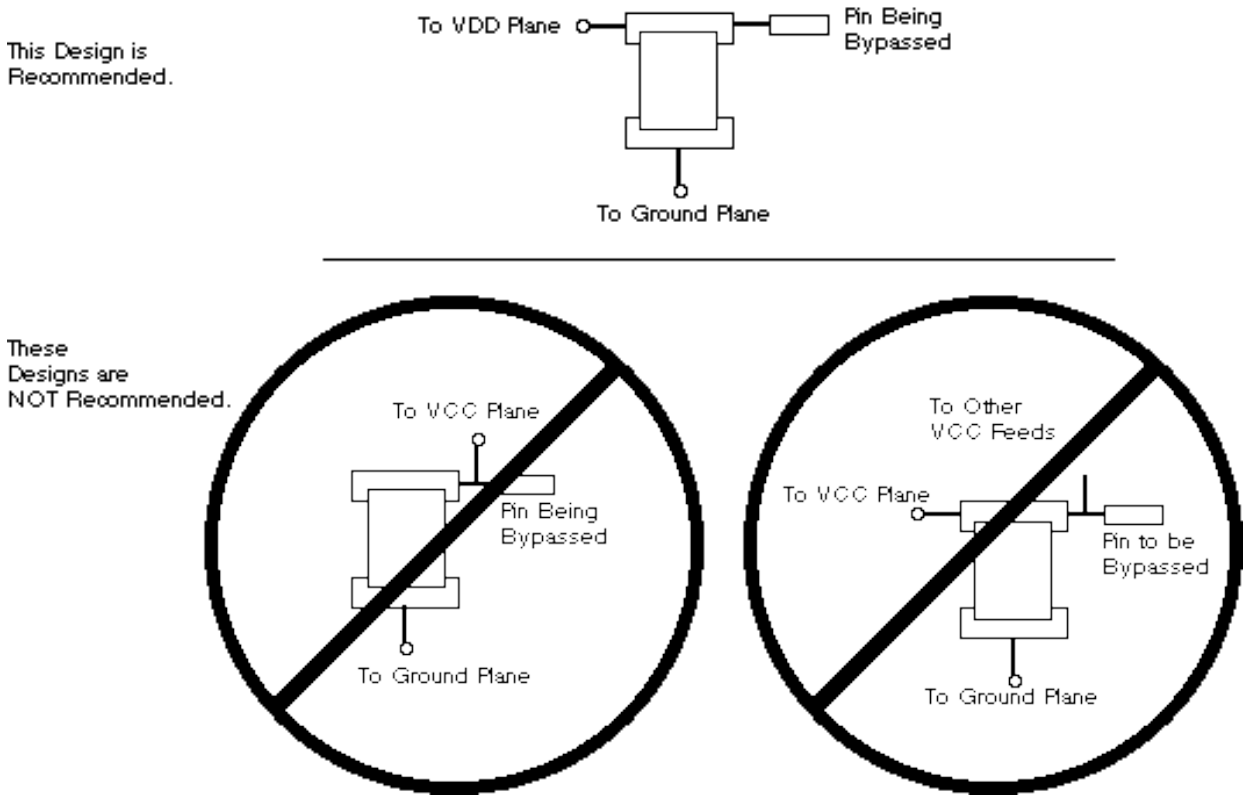


Figure 3-1 FCS Design

4. Mount R1 and C11-13 as close as possible to U1-12 and 13. Keep the lines from U1-67 and 68 to C13 and C12 away from other signal lines, and keep them as short as possible, and surround them with ground.

3.4.5 Recommendations for Creating a PC Board Layout

Follow the steps below when creating a PC board layout with the Flash ChipSet.

1. Draw the schematic for your application based on the schematics in the appendices. These schematics and corresponding netlists are available in file form from SanDisk. Call SanDisk Applications Engineering at 408-542-0405 to request a copy.
2. Fax a copy of the schematic to SanDisk Applications Engineering for review.The fax number is 408-542-0403.
3. Make changes as needed and begin PCB layout. Use only SanDisk recommended components or equivalent. See the Flash ChipSet Product Manual.
4. When layout is completed, fax a copy of the layout and schematic to SanDisk Applications Engineering for review.
5. Make changes as needed and fabricate prototype boards.
6. Carefully inspect a finished board and compare it to the schematic before mounting components.

3.5 Bringing up and Debugging the Prototype

3.5.1 Development Environment

It is highly recommended that initial development be done in a PC-AT environment using MS-DOS. This will greatly simplify debugging because of the wealth of hardware and software tools available in this environment. For example, SanDisk provides the Flash ChipSet

Evaluation Kit (see the Ordering Information Chapter in this manual), which includes adapters and software utilities to assist the FCS user. Even without such a kit, simply connecting to the IDE connector and using DOS DEBUG to communicate with the SanDisk controller in the prototype will go far toward bringing up the prototype.

3.5.2 Setting the Oscillator Frequency

It is crucial to set the oscillator frequency before proceeding with further testing, since proper memory operation requires that the serial clock be within certain limits.

The frequency should be set at room temperature (approximately 22° C). It should not be measured at either end of R1, since the measuring instrument will load the tank circuit and change the frequency. Instead, connect a frequency counter to the SCLK1 line at either pin 53 of the controller. The frequency at this point is 1/8 of the oscillator frequency, or 2 MHz at 5 volts and 1.25 MHz at 3.3 volts.

It is assumed in the following steps that the test environment is a standard PC and the Flash ChipSet is the master IDE drive. It is important that the BIOS not access the ChipSet until the frequency is set, since errors can occur which could damage the memory. Therefore, before testing the ChipSet, install the BIOS hard drive setting to "no drive installed."

In order to measure the frequency, the controller must be active, and not in the sleep mode. This can be done with the DOS DEBUG utility as follows:

1. Make sure that the FCS is set as drive 0 (master) on the primary IDE channel.
2. Load DEBUG and read the controller's status register by entering **I 1F7** at the prompt. This should return a value of 50H, which indicates that the device is ready. If not, nothing further can be done, since the controller will not respond to commands. Check to make sure that power is applied to the FCS, that the traces on the board match the schematic, and that there are no obvious shorts or bad solder joints. Probe all the pins on the IDE connector with an oscilloscope to see if any lines are obviously shorted or open.
3. Once the controller responds that it is ready, disable automatic power saving mode by entering **O 1F2 0.**
4. Now set idle by entering **O 1F7 E3.**
5. Measure the SCLK1 frequency.

If dual voltage operation is required, first set the supply to 5.00 volts, apply power, and adjust the value of R1 and C11 until the frequency is 2.0 MHz $\pm$ 63 KHz, making sure that the value of R1 is between 1.0K and 1.5K ohms. Turn off power, adjust the power supply to 3.30 volts, apply power, and adjust the value of C12 until the frequency is 1.25 MHz ± 39 KHz. Note that there is a second order interaction between these two settings, since C12 will slightly load C11 even when it is not actually switched in, so repeat the adjustment steps for a final tweaking of values.

If dual voltage operation is not required, omit C12 and adjust the values of R1 and C11 until the proper frequency is achieved. (2.0 MHz ± 63 KHz at 5.00 volts, or 1.25 MHz ± 39 KHz at 3.30 volts)

To confirm that the component values are correct, test the frequency on five to ten prototypes and make final adjustments if necessary. In production use a ± 0.5% resistor for R1, and ± 5% capacitors for C11 and C12. It is not necessary to check the frequency of each production unit, as there is enough extra margin built into the FCS to accommodate the recommended component tolerances.

3.5.3 Testing for Proper Operation

Follow the steps below to test for proper operation:

1. Using DOS DEBUG again, write data to registers as follows:

   O 1F2 AA

   O 1F3 55

   O 1F4 CC

   O 1F5 33

2. Now read each register in turn to see if the data matches what was written. This will test for stuck, shorted or open bits.

   I 1F2

   I 1F3

   I 1F4

   I 1F5

3. Next send the EXECUTE DRIVE DIAGNOSTICS command.

   O 1F7 90

4. Now read the task file registers.

   I 1F1— Should contain 01. Otherwise there is an error. See table 9-2 of this manual for error definitions.

   I 1F2—Should contain 01.

   I 1F3—Should contain 01.

   I 1F4—Should contain 00.

   I 1F5—Should contain 00.

   I 1F6—Should contain 00.

   I 1F7—Should contain 50.

At this point the board is probably working properly. It would be useful now to use the SDDEMO utility to read and write to the card. This program can run script files to issue commands to the board in different orders and using different data patterns to thoroughly test the board.

3.6 Design Tools and Software Utilities

3.6.1 Hardware

The SanDisk Flash ChipSet Evaluation Kit provides a development board with sockets for a controller and a TSOP. This module has a 68 pin PCMCIA connector. In addition, the kit includes an adapter board which plugs into a standard 16-bit ISA board which plugs into any 386 / 486 / Pentium PC, and an adapter board which allows connection to a standard 40 pin IDE connector.

3.6.2 Software

The SanDisk Host Developer's Tool Kit provides C source code for all necessary routines to develop an MS-DOS compatible FAT file system for any hardware platform which does not provide this function. This kit is available for purchase, and provides an invaluable resource which can save many man-months of software development.

The SDP Sample Source Code and SDDEMO Utility disk is available free of charge. It is also included with the Flash ChipSet Evaluation Kit. A diskette containing Orcad design files and netlists is also available free of charge. Contact SanDisk Applications Engineering at 408-542-0400 for more information.

4.0 Flash ChipSet Controller Interface Description

4.1 FCS Controller Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 4-1. Low active signals have a "-" prefix. Pin type is Input, Output or Input/Output. The table following this Pin Assignment defines the DC characteristics for all Input and Output type structures.

4.2 FCS Controller Electrical Description

Table 4-2 describes the I/O signals. Signals whose source is the host are designated as inputs while signals which the Flash ChipSet sources are outputs. All Host Interface logic levels conform to those specified in the PCMCIA Release 2.1 specification. Refer to section 4.3 for definitions of Input and Output type.

Table 4-1 FCS Controller Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode			True IDE Mode		
Pin Num	Signal Name	Pin Type	In, Out[4] Type	Signal Name	Pin Type	In, Out[4] Type	Signal Name	Pin Type	In, Out[4] Type
1	HD15[1]	I/O	I1Z,OZ3	HD15[1]	I/O	I1Z,OZ3	HD15[1]	I/O	I1Z,OZ3
2	HD14[1]	I/O	I1Z,OZ3	HD14[1]	I/O	I1Z,OZ3	HD14[1]	I/O	I1Z,OZ3
3	HD13[1]	I/O	I1Z,OZ3	HD13[1]	I/O	I1Z,OZ3	HD13[1]	I/O	I1Z,OZ3
4	HD12[1]	I/O	I1Z,OZ3	HD12[1]	I/O	I1Z,OZ3	HD12[1]	I/O	I1Z,OZ3
5	VDD 1 & 2		POWER	VDD 1 & 2		POWER	VDD 1 & 2		POWER
6	HD11[1]	I/O	I1Z,OZ3	HD11[1]	I/O	I1Z,OZ3	HD11[1]	I/O	I1Z,OZ3
7	HD10[1]	I/O	I1Z,OZ3	HD10[1]	I/O	I1Z,OZ3	HD10[1]	I/O	I1Z,OZ3
8	HD9[1]	I/O	I1Z,OZ3	HD9[1]	I/O	I1Z,OZ3	HD9[1]	I/O	I1Z,OZ3
9	HD8[1]	I/O	I1Z,OZ3	HD8[1]	I/O	I1Z,OZ3	HD8[1]	I/O	I1Z,OZ3
10	GND 1 & 2		GROUND	GND 1 & 2		GROUND	GND 1 & 2		GROUND
11	RC_IN	I	I3Z	RC_IN	I	I3Z	RC_IN	I	I3Z
12	C_EXT	O	OT3	C_EXT	O	OT3	C_EXT	O	OT3
13	HD7	I/O	I1Z,OZ3	HD7	I/O	I1Z,OZ3	HD7	I/O	I1Z,OZ3
14	HD6	I/O	I1Z,OZ3	HD6	I/O	I1Z,OZ3	HD6	I/O	I1Z,OZ3
15	VDD 3 & 4		POWER	VDD 3 & 4		POWER	VDD 3 & 4		POWER
16	HD5	I/O	I1Z,OZ3	HD5	I/O	I1Z,OZ3	HD5	I/O	I1Z,OZ3
17	HD4	I/O	I1Z,OZ3	HD4	I/O	I1Z,OZ3	HD4	I/O	I1Z,OZ3
18	HD3	I/O	I1Z,OZ3	HD3	I/O	I1Z,OZ3	HD3	I/O	I1Z,OZ3
19	HD2	I/O	I1Z,OZ3	HD2	I/O	I1Z,OZ3	HD2	I/O	I1Z,OZ3
20	GND 3 & 4		GROUND	GND 3 & 4		GROUND	GND 3 & 4		GROUND
21	HD1	I/O	I1Z,OZ3	HD1	I/O	I1Z,OZ3	HD1	I/O	I1Z,OZ3
22	HD0	I/O	I1Z,OZ3	HD0	I/O	I1Z,OZ3	HD0	I/O	I1Z,OZ3
23	-CSEL	I	I2Z	-CSEL	I	I2Z	-CSEL	I	I2U
24	HA10	I	I1Z	HA10	I	I1Z	HA10[2]	I	I1Z
25	HA9	I	I1Z	HA9	I	I1Z	HA9[2]	I	I1Z
26	HA8	I	I1Z	HA8	I	I1Z	HA8[2]	I	I1Z
27	HA7	I	I1Z	HA7	I	I1Z	HA7[2]	I	I1Z

Table 4-1 FCS Controller Pin Assignments and Pin Type (con't)

PC Card Memory Mode				PC Card I/O Mode			True IDE Mode		
Pin Num	Signal Name	Pin Type	In, Out[4] Type	Signal Name	Pin Type	In, Out[4] Type	Signal Name	Pin Type	In, Out[4] Type
28	HA6	I	I1Z	HA6	I	I1Z	HA6[2]	I	I1Z
29	HA5	I	I1Z	HA5	I	I1Z	HA5[2]	I	I1Z
30	HA4	I	I1Z	HA4	I	I1Z	HA4[2]	I	I1Z
31	HA3	I	I1Z	HA3	I	I1Z	HA3[2]	I	I1Z
32	GND 5 & 6		GROUND	GND 5 & 6		GROUND	GND 5 & 6		GROUND
33	HA2	I	I1Z	HA2	I	I1Z	HA2	I	I1Z
34	HA1	I	I1Z	HA1	I	I1Z	HA1	I	I1Z
35	HA0	I	I1Z	HA0	I	I1Z	HA0	I	I1Z
36	RESET	I	I2Z	RESET	I	I2Z	-RESET	I	I2Z
37	-CE1	I	I3U	-CE1	I	I3U	-CS0	I	I3Z
38	VDD 5 & 6		POWER	VDD 5 & 6		POWER	VDD 5 & 6		POWER
39	-CE2[1]	I	I3U	-CE2[1]	I	I3U	-CS1[1]	I	I3Z
40	-OE	I	I3U	-OE	I	I3U	-ATA SEL	I	I3U
41	-WE	I	I3U	-WE	I	I3U	-WE[3]	I	I3U
42	-IORD	I	I3U	-IORD	I	I3U	-IORD	I	I3Z
43	-IOWR	I	I3U	-IOWR	I	I3U	-IOWR	I	I3Z
44	GND 7& 8		GROUND	GND 7& 8		GROUND	GND 7& 8		GROUND
45	-REG	I	I3U	-REG	I	I3U	-REG[3]	I	I3U
46	RDY	O	OT1	IREQ	O	OT1	INTRQ	O	OZ1
47	-WAIT	O	OT1	-WAIT	O	OT1	IORDY	O	ON1
48	-INPACK	O	OT1	-INPACK	O	OT1	-INPACK	O	OZ1
49	BVD2	I/O	I1U,OT1	-SPKR	I/O	I1U,OT1	-DASP	I/O	I1U,ON1
50	BVD1	I/O	I1U,OT1	-STSCHG	I/O	I1U,OT1	-PDIAG	I/O	I1U,ON1
51	WPROTCT	I	I1D	WPROTCT	I	I1D	WPROTCT	I	I1D
52	WP	O	OT3	-IO16	O	OT3	-IO16	O	ON3
53	SCLK1	O	OT2	SCLK1	O	OT2	SCLK1	O	OT2
54	SCLK0	O	OT2	SCLK0	O	OT2	SCLK0	O	OT2
55	CS	O		CS	O		CS	O	
56	VDD 7 & 8		POWER	VDD 7 & 8		POWER	VDD 7 & 8		POWER
57	PD	O	OT3	PD	O	OT3	PD	O	OT3
58	SI1	O	OT3	SI1	O	OT3	SI1	O	OT3
59	SI0	O	OT3	SI0	O	OT3	SI0	O	OT3
60	SO1	I/O	I1U,OZ1	SO1	I/O	I1U,OZ1	SO1	I/O	I1U,OZ1
61	GND 9 & 10		GROUND	GND 9 & 10		GROUND	GND 9 & 10		GROUND
62	SO0	I/O	I1U,OZ1	SO0	I/O	I1U,OZ1	SO0	I/O	I1U,OZ1
63	SO3	I	I1D	SO3	I	I1D	SO3	I	I1D
64	TEST	I	I1D	TEST	I	I1D	TEST	I	I1D
65	VDD 9 & 10		POWER	VDD 9 & 10		POWER	VDD 9 & 10		POWER
66	IO0	I/O	I1U,OZ1	IO0	I/O	I1U,OZ1	IO0	I/O	I1U,OZ1
67	IO1	I/O	I1U,OZ1	IO1	I/O	I1U,OZ1	IO1	I/O	I1U,OZ1
68	IO2	I/O	I1U,OZ1	IO2	I/O	I1U,OZ1	IO2	I/O	I1U,OZ1

Table 4-1 FCS Controller Pin Assignments and Pin Type (con't)

PC Card Memory Mode				PC Card I/O Mode			True IDE Mode		
Pin Num	Signal Name	Pin Type	In, Out[4] Type	Signal Name	Pin Type	In, Out[4] Type	Signal Name	Pin Type	In, Out[4] Type
69	SO2	I/O	I1U,OZ1	SO2	I/O	I1U,OZ1	SO2	I/O	I1U,OZ1
70	GND 11 &12		GROUND	GND 11 &12		GROUND	GND 11 &12		GROUND
71	-ROMCEL0	O	OT1	-ROMCEL0	O	OT1	-ROMCEL0	O	OT1
72	-ROMOEL	O	OT1	-ROMOEL	O	OT1	-ROMOEL	O	OT1
73	-ROMWEL	I/O	I1D, OT1	-ROMWEL	I/O	I1D, OT1	-ROMWEL	I/O	I1D, OT1
74	MA0	I/O	I1Z,OT1	MA0	I/O	I1Z,OT1	MA0	I/O	I1Z,OT1
75	MA1	I/O	I1Z,OT1	MA1	I/O	I1Z,OT1	MA1	I/O	I1Z,OT1
76	MA2	I/O	I1Z,OT1	MA2	I/O	I1Z,OT1	MA2	I/O	I1Z,OT1
77	MA3	I/O	I1Z,OT1	MA3	I/O	I1Z,OT1	MA3	I/O	I1Z,OT1
78	MA4	I/O	I1Z,OT1	MA4	I/O	I1Z,OT1	MA4	I/O	I1Z,OT1
79	MA5	I/O	I1Z,OT1	MA5	I/O	I1Z,OT1	MA5	I/O	I1Z,OT1
80	MA6	I/O	I1Z,OT1	MA6	I/O	I1Z,OT1	MA6	I/O	I1Z,OT1
81	MA7	I/O	I1Z,OT1	MA7	I/O	I1Z,OT1	MA7	I/O	I1Z,OT1
82	GND 13&14		GROUND	GND 13&14		GROUND	GND 13&14		GROUND
83	MA8	I/O	I1Z,OT1	MA8	I/O	I1Z,OT1	MA8	I/O	I1Z,OT1
84	MA9	I/O	I1Z,OT1	MA9	I/O	I1Z,OT1	MA9	I/O	I1Z,OT1
85	MA10	I/O	I1Z,OT1	MA10	I/O	I1Z,OT1	MA10	I/O	I1Z,OT1
86	MA11	I/O	I1Z,OT1	MA11	I/O	I1Z,OT1	MA11	I/O	I1Z,OT1
87	MA12	I/O	I1Z,OT1	MA12	I/O	I1Z,OT1	MA12	I/O	I1Z,OT1
88	VDD 11&12		POWER	VDD 11&12		POWER	VDD 11&12		POWER
89	MA13	I/O	I1Z,OT1	MA13	I/O	I1Z,OT1	MA13	I/O	I1Z,OT1
90	MA14	I/O	I1Z,OT1	MA14	I/O	I1Z,OT1	MA14	I/O	I1Z,OT1
91	MA15	I/O	I1Z,OT1	MA15	I/O	I1Z,OT1	MA15	I/O	I1Z,OT1
92	MD0	I/O	I1U,OT1	MD0	I/O	I1U,OT1	MD0	I/O	I1U,OT1
93	MD1	I/O	I1U,OT1	MD1	I/O	I1U,OT1	MD1	I/O	I1U,OT1
94	GND 15&16		GROUND	GND 15&16		GROUND	GND 15&16		GROUND
95	MD2	I/O	I1U,OT1	MD2	I/O	I1U,OT1	MD2	I/O	I1U,OT1
96	MD3	I/O	I1U,OT1	MD3	I/O	I1U,OT1	MD3	I/O	I1U,OT1
97	MD4	I/O	I1U,OT1	MD4	I/O	I1U,OT1	MD4	I/O	I1U,OT1
98	MD5	I/O	I1U,OT1	MD5	I/O	I1U,OT1	MD5	I/O	I1U,OT1
99	MD6	I/O	I1U,OT1	MD6	I/O	I1U,OT1	MD6	I/O	I1U,OT1
100	MD7	I/O	I1U,OT1	MD7	I/O	I1U,OT1	MD7	I/O	I1U,OT1

Note: 1. These signals are required only for 16 bit access and not required when installed in 8-bit systems. For lowest power dissipation, leave these signals open.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.
4. Please refer to section 4.3 for definitions of In, Out type.

Table 4-2 FCS Controller Signal Description (Host Interface)

Signal Name	Dir.	Pin	Description
BVD1 (PC Card Memory Mode)	I/O	50	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	49	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	37, 39	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multi-plexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Tables 9-1, 9-2, 9-5, 9-6 and 9-7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode)	I	23	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
HA10 - HA0 (PC Card Memory Mode)	I	24, 25, 26, 27, 28, 29, 30, 31, 33, 34, 35	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the Flash ChipSet, the memory mapped port address registers within the Flash ChipSet, a byte in the card's information structure and its configuration control and status registers.
HA10 - HA0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
HA10 - HA0 (True IDE Mode)	I		In True IDE Mode only HA[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.

Table 4-2 FCS Controller Signal Description (Host Interface)

Signal Name	Dir.	Pin	Description
HD15 - HD00 (PC Card Memory Mode)	I/O	1, 2, 3, 4, 6, 7, 8, 9, 13, 14, 16, 17, 18, 19, 21, 22	These lines carry the data, commands and status information between the host and the controller. HD00 is the LSB of the even byte of the word. HD08 is the LSB of the odd byte of the word.
HD15 - HD00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
HD15 - HD00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
-INPACK (PC Card Memory Mode)	O	48	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the Flash ChipSet when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the Flash ChipSet and the CPU.
-INPACK (True IDE Mode)			In True IDE Mode this output signal is not used and should not be connected at the host.
-IORD (PC Card Memory Mode)	I	42	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Flash ChipSet when the Flash ChipSet is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode)	I	43	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the Flash ChipSet controller registers when the Flash ChipSet is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode)	I	40	This is an Output Enable strobe generated by the host interface. It is used to read data from the Flash ChipSet in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.

Table 4-2 FCS Controller Signal Description (Host Interface)

Signal Name	Dir.	Pin	Description
RDY (PC Card Memory Mode)	O	46	In Memory Mode this signal is set high when the Flash ChipSet is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the Flash ChipSet has completed its power up or reset function. No access of any type should be made to the Flash ChipSet during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The Flash ChipSet has been powered up with +RESET continuously disconnected or asserted.
IREQ (PC Card I/O Mode)			I/O Operation - After the Flash ChipSet has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select	I	45	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
RESET (PC Card Memory Mode)	I	36	When the pin is high, this signal Resets the Flash ChipSet. The Flash ChipSet is Reset only at power up if this pin is left high or open from power-up. The Flash ChipSet is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
-WAIT (PC Card Memory Mode)	O	47	The -WAIT signal is driven low by the Flash ChipSet to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode)			In True IDE Mode this output signal may be used as IORDY.
-WE (PC Card Memory Mode)	I	41	This is a signal driven by the host and used for strobing memory write data to the registers of the Flash ChipSet when the Flash ChipSet is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect	O	52	Memory Mode - The Flash ChipSet does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IO16 (PC Card I/O Mode)			I/O Operation - When the Flash ChipSet is configured for I/O Operation, Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IO16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

Table 4-2 FCS Controller Signal Description (Flash Memory Interface)

Signal Name	Dir.	Pin	Description
CS	O	55	This is the chip select that runs to all the Flash memory chips and allows the select state to be entered for those devices with the proper IDs loaded.
PD	O	57	This is a control line that goes to the Flash memory and is shared by all in a Daisy-chain manner. This line controls where the data on the serial interface from the controller to the memory is gated internal to the memory. This signal connects to all memories in a Daisy-chained manner.
SCLK0 SCLK1	O	53, 54	These are the clock that drives the Flash memory device.
SI0	O	59	This is a serial in data line to the memory from the controller. This is the even bit of the serial data stream. This signal connects to all memories in a Daisy-chained manner.
SI1	O	58	This is a serial in data line to the memory from the controller. This is the odd bit of the serial data stream. This signal connects to all memories in a Daisy-chained manner.
SO0	I/O	62	This is the even bit data line that is used to send serial information from the Flash memory to the SanDisk controller. This is a Daisy-Chained line between the Flash memory chips.
SO1	I/O	60	This is the odd bit data line that is used to send serial information from the Flash memory to the SanDisk controller. This is a Daisy-Chained line between the Flash memory chips.
SO2	I/O	69	This is the third data line that is used to send serial information from the Flash memory to the SanDisk controller. This is a Daisy-Chained line between the Flash memory chips. This pin is only used with the 64 Mbit Memory and Controller combination.
SO3	I	63	This is the fourth data line that is used to send serial information from the Flash memory to the SanDisk controller. This is a Daisy-Chained line between the Flash memory chips. This pin is only used with the 64 Mbit Memory and Controller combination.

Table 4-2 FCS Controller Signal Description (Control and Configuration)

Signal Name	Dir.	Pin	Description
C_EXT	O	12	This pin is part of the clock circuit. In an RC network, this pin is connected to the capacitor resistor junction.
GND[XX]	--	10, 20, 32, 44, 61, 70, 82, 94	Ground.
IO0	I/O	66	This is programmed as an output pin that is used to drive a power switch to isolate VDD in the memory array. This line goes low for turning ON power and goes High for turning power OFF.
IO1 IO2	I/O	67, 68	These pins are reserved for “Frequency Adjusters” in the RC Network.
RC_IN	I	11	This is the input used to connect an Resistor/Capacitor (RC) network to generate a clock.
TEST	I	64	This internally pulled down input pin when set to a 1, puts this device in a test mode. This pin should not be connected in a user system.
VDD[XX]	--	5, 15, 38, 56, 65, 88	+5 V power or +3.3 volt power.
WPROTCT	I	51	This input signal is to be asserted high if the memory is in the Write Protect Mode. This pin should normally be grounded.

Table 4-2 FCS Controller Signal Description (External ROM Interface)

Signal Name	Dir.	Pin	Description
MA[15-0]	I/O	91, 90, 89, 87 86, 85, 84, 83 81, 80, 79, 78 77, 76, 75, 74	These lines are used by the controller to address the external Eprom or Flash memory. These lines drive the memory for both reading and writing the bus. The address lines are listed from MSB (15) to LSB (0).
MD[7-0]	I/O	100, 99, 98 97, 96, 95 93, 92	These I/O lines carry the data between the external Eprom or Flash device and the internal 68000 processor.
-ROMCEL0	O	71	This output signal is used to select the external EPROM used for control store by the internal 68000 processor. This signal should be connected to the -CE pin of the external memory device.
-ROMOEL	O	72	This signal is used by the controller for enabling external control store into the internal microprocessor. This signal gates the output enable function for the external EPROM, allowing it to drive the bus.
-ROMWEL	I/O	73	This signal gates the write gate to an external Flash memory when used as control store. This signal is driven low active by the 68000 processor allowing it to modify the code for download updates. This pin should not be connected by the system to enable the internal MASK ROM program memory. If this pin is connected to an external pull-up resistor, the external EEPROM is enabled.

4.3 FCS Controller Electrical Specification

The following table defines all D.C. Characteristics for the Flash ChipSet Controller.

Unless otherwise stated, conditions are:

SDFCSTB	SDFCSTBI
Vcc = 5V ±10%	Vcc = 5V ± 5%
Vcc = 3.3V ±5%	Vcc = 3.3V ±5%
Ta = 0°C to 60°C	Ta = -40°C to 85°C

Absolute Maximum conditions are:

Vcc = -0.3V min. to 7.0V max.

V* = -0.5V min. to Vcc + 0.5V max.

* Voltage on any pin except Vcc with respect to GND.

4.3.1 Input Leakage Current

Note: In the table below, x refers to the characteristics described in section 4.3.2. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
IxZ	Input Leakage Current	IL	Vih = Vcc / Vil = Gnd	-1		1	µA
IxU	Pull Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
IxD	Pull Down Resistor	RPD1	Vcc = 5.0V	50k		500k	Ohm

Note: The minimum pullup resistor leakage current meets the PCMCIA specification of 10k ohms but is intentionally higher in the Flash ChipSet to reduce power use.

4.3.2 Input Characteristics

Type	Parameter	Symbol	MIN	TYP	MAX	MIN	TYP	MAX	Units
			VCC = 3.3 V			VCC = 5.0 V			
1	Input Voltage CMOS	Vih Vil	2.4		0.6	3.0		0.8	Volts
2	Input Voltage CMOS	Vih Vil	1.5		0.6	2.0		0.8	Volts
3	Input Voltage CMOS Schmitt Trigger	Vth Vtl		1.8 1.0			2.8 2.0		Volts

4.3.3 Output Drive Type

Note: In the table below, x refers to the characteristics in section 4.3.4. For example, OT3 refers to Totempole output with a type 3 output drive characteristic.

Type	Output Type	Valid Conditions
OTx	Totempole	Ioh & Iol
OZx	Tri-State N-P Channel	Ioh & Iol
OPx	P-Channel Only	Ioh Only
ONx	N-Channel Only	Iol Only

4.3.4 Output Drive Characteristics

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
2	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 Gnd +0.4V	Volts
3	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 Gnd +0.4V	Volts
X	Tri-State Leakage Current	Ioz	Vol = Gnd Voh = Vcc	-10		10	µA

4.4 FCS Controller Pinout Drawing

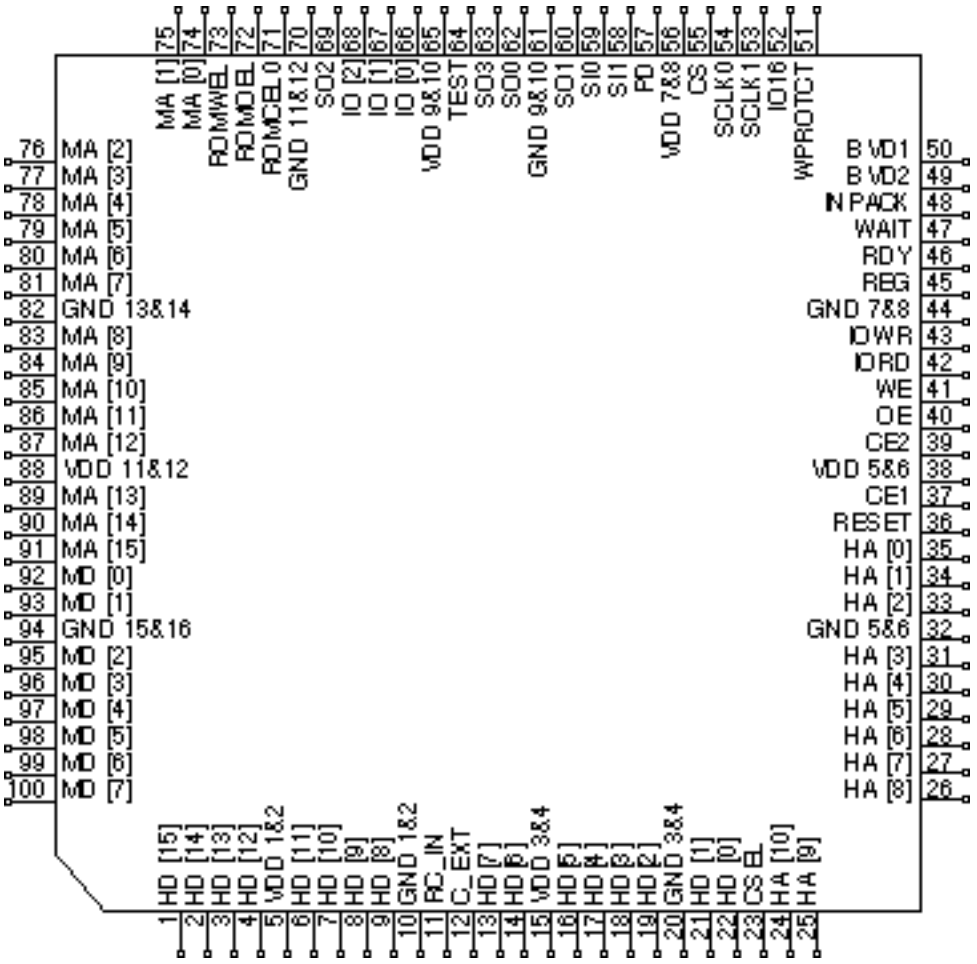


Figure 4-1 FCS Controller Pinout Drawing

4.5 FCS Controller Package Drawing (1)

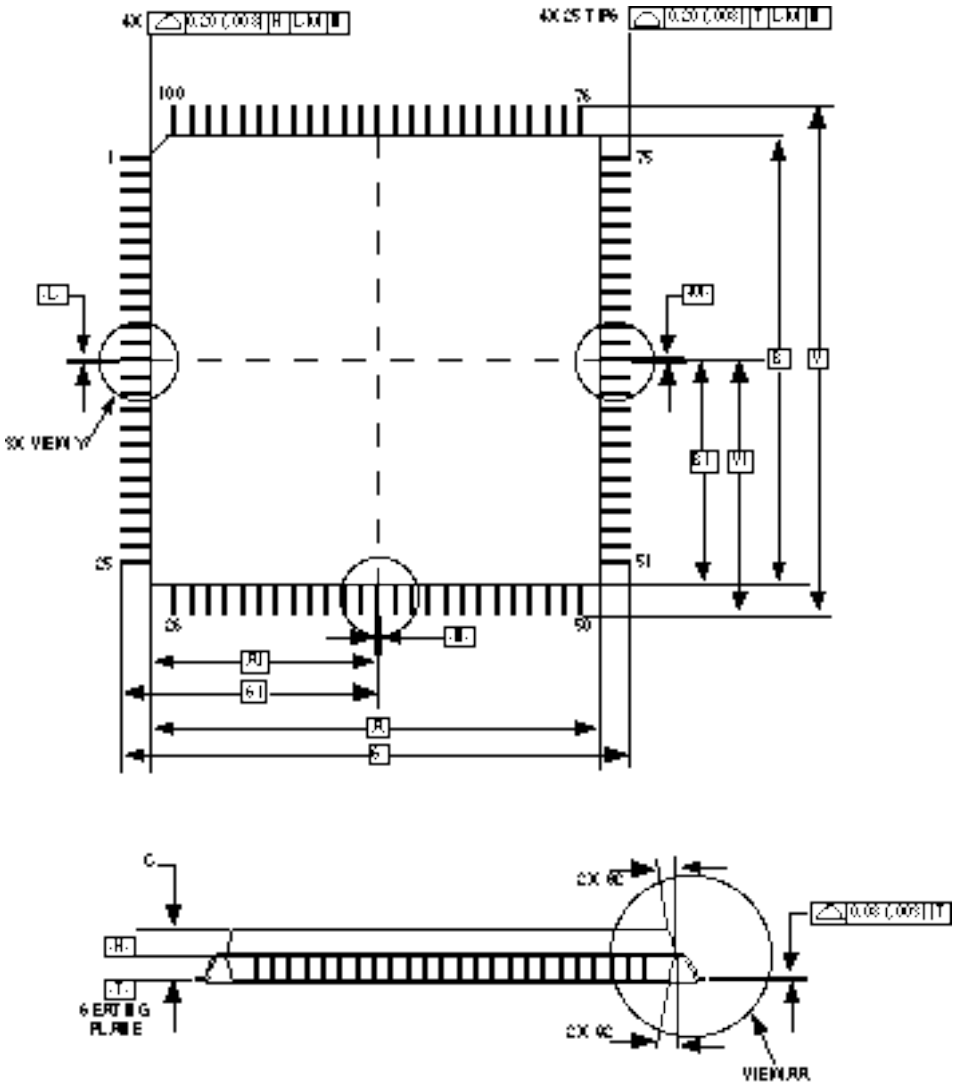


Figure 4-2 FCS Controller Package Drawing Page 1

4.5 FCS Controller Package Drawing (2)

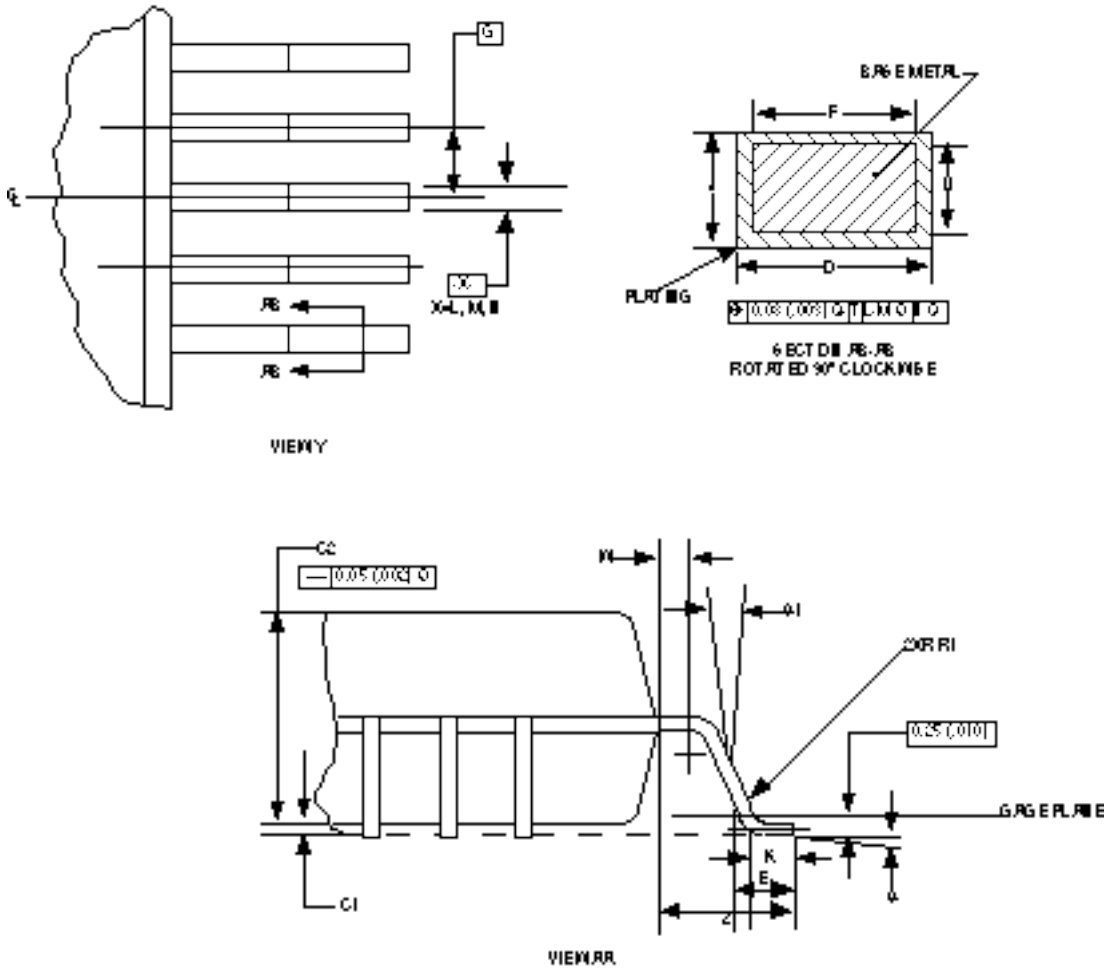


Figure 4-2 FCS Controller Package Drawing Page 2

4.5 FCS Controller Package Drawing (3)

NOTES

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L- , -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35 (.014). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (.003).

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.00 BSC		.551 BSC	
A1	7.00 BSC		.276 BSC	
B	14.00 BSC		.551 BSC	
B1	7.00 BSC		.276 BSC	
C	---	1.20	---	.048
C1	0.05	0.15	.002	.006
C2	.95	1.05	.037	.042
D	0.17	0.27	.007	.011
E	0.45	0.75	.018	.030
F	0.17	0.23	.007	.009
G	0.50 BSC		.020 BSC	
J	0.09	0.20	.004	.008
K	0.50 REF		.020 REF	
R1	0.10	0.20	.004	.008
S	16.00 BSC		.630 BSC	
S1	8.00 BSC		.315 BSC	
U	0.09	0.16	.004	.006
V	16.00 BSC		.630 BSC	
V1	8.00 BSC		.315 BSC	
W	0.20 REF		.008 REF	
Z	1.00 REF		.039 REF	
0	0°	7°	0°	7°
01	0°	---	0°	---
02	12° REF		12° REF	
03	5°	13°	5°	13°

Figure 4-2 FCS Controller Package Drawing Page 3

5.0 Flash ChipSet TSOP Interface Description

5.1 FCS TSOP Introduction

The SanDisk Flash ChipSet TSOP is a Thin Small Outline Package (TSOP) packaged in a 56 lead chip carrier manufactured using chip on board technology. This memory device is supplied by SanDisk in a preformatted and tested state. All initial defects are reassigned at the factory and will appear to the user as a perfect memory array. The four megabyte TSOP appears as a memory array configuration of 123 cylinders, 2 heads and 32 sectors/track for a total capacity of 4,030,464 bytes of data. The eight megabyte TSOP appears as a memory array configuration of 245 cylinders, 2 heads and 32 sectors/track for a total capacity of 8,028,160 bytes of data. The 16 megabyte TSOP appears as a memory array configuration of of 490 cylinders, 2 heads and 32 sectors/track for a total capacity of 16,056,320 bytes of data.

5.2 FCS TSOP Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 5-1. Pin type is input, output or input/output.

5.3 FCS TSOP Electrical Description

Table 5-2 describes the I/O signals. Signals whose source is the Flash ChipSet controller are designated as inputs while signals which the controller receives are outputs.

Table 5-1 FCS TSOP Pin Assignments and Pin Type

Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type
1	VDD_A	Power	56	VDD_B	Power
2	C1_1_A	Cap	55	C1_1_B	Cap
3	C2_1_A	Cap	54	C2_1_B	Cap
4	C3_1_A	Cap	53	C3_1_B	Cap
5	C1_2_A	Cap	52	C1_2_B	Cap
6	C4_1_A	Cap	51	C4_1_B	Cap
7	C3_2_A	Cap	50	C3_2_B	Cap
8	C2_2_A	Cap	49	C2_2_B	Cap
9	C4_2_A	Cap	48	C4_2_B	Cap
10	VSS_A	Power	47	VSS_B	Power
11	VSS1_A	Power	46	VSS1_B	Power
12	A5_A	I	45	A5_B	I
13	SO1_A	O	44	SO1_B	O
14	A0_A	I	43	A0_B	I
15	A0_1_A	I	42	A0_1_B	I
16	SO0_A	O	41	SO0_B	O
17	A1_A	I	40	A1_B	I
18	SO2_A	O	39	SO2_B	O
19	VPP_A	Power	38	VPP_B	Power
20	SO3_A	O	37	SO3_B	O
21	A2_A	I	36	A2_B	I
22	MS_A	I	35	MS_B	I
23	A3_A	I	34	A3_B	I
24	SCLK_A	I	33	SCLK_B	I
25	P/D_A	I	32	P/D_B	I
26	A4_A	I	31	A4_B	I
27	SI1_A	I	30	SI1_B	I
28	SI0_A	I	29	SI0_B	I

Table 5-2 FCS TSOP Signal Description (Controller Interface)

Signal Name	Dir.	Pin	Description
MS_A, MS_B	I	22, 35	These are the chip selects to the memory device from the Flash ChipSet controller chip. These signals allow the select state to be entered for those devices with the proper IDs loaded.
P/D_A, P/D_B	I	25, 32	These input signals from the controller control where the data on the serial interface from the controller to the memory is gated internal to the memory.
SCLK_A, SCLK_B	I	24, 33	These are the clock inputs from the controller and are used in all shifting of data and control information to and from the memory device. These clock signals are also used as the source for the internal switch capacitor DC to DC converter.
SI[0,1]_A, SI[0,1]_B	I	28, 27, 29, 30	These are the serial in data lines from the controller to the memory. They are used to transfer all data and commands into the memory device.
SO[0,1]_A SO[0,1]_B	O	16, 13, 41, 44	These are the serial out data lines from the memory device to the controller. They are used to transfer all data and status to the controller.
SO[2,3]_A, SO[2,3]_B	O	18, 20, 39, 37	These are the high order serial out data lines from the memory device to the controller. They are used to transfer all data to the controller. They are only used with the 64 Mbit Memory and Controller combination.

Table 5-2 FCS TSOP Signal Description (Power and Configuration)

A[0-5]_A, A[0-5]_B A0_1_A, A0_1_B	I	14, 17, 21, 23, 26, 12, 43, 40, 36, 34, 31, 45, 15, 42	These are the address select signals for the memory device. These binary encoded pins allow up to 63 memory devices to be connected in parallel.
C1_1_A, C1_2_A C1_1_B, C1_2_B	Cap	2, 5 55, 52	This is one of the pin pairs that is used in the switched capacitor DC to DC converter. There should be a .1 µf capacitor connected between these pins. The two pins on the B side of the TSOP (55 and 52) are reserved for future use.
C2_1_A, C2_2_A C2_1_B, C2_2_B	Cap	3, 8 54, 49	This is one of the pin pairs that is used in the switched capacitor DC to DC converter. There should be a .1 µf capacitor connected between these pins. The two pins on the B side of the TSOP (54 and 49) are reserved for future use.
C3_1_A, C3_2_A C3_1_B, C3_2_B	Cap	4, 7 53, 50	This is one of the pin pairs that is used in the switched capacitor DC to DC converter. There should be a .1 µf capacitor connected between these pins. The two pins on the B side of the TSOP (53 and 50) are reserved for future use.
C4_1_A, C4_2_A C4_1_B, C4_2_B	Cap	6, 9 51, 48	This is one of the pin pairs that is used in the switched capacitor DC to DC converter. There should be a .1 µf capacitor connected between these pins. The two pins on the B side of the TSOP (51 and 48) are reserved for future use.
VSS_A, VSS_B, VSS1_A, VSS1_B	--	10, 47, 11, 46	Ground
VDD_A, VDD_B	--	1, 56	This is the 5 volt / 3 volt supply pin for the memory device. It is recommended this pin be switched from the host system with a PFET that has an on resistance of less than .5 ohms. The switch is to isolate the leakage current the memory device consumes from the host power supply when the device is not active.
VPP_A, VPP_B	Cap	19, 38	This is an internally generated 12 volt supply voltage that is used for all erase and programming operations. The system should connect this pin to a .22 µf capacitor. The other side of the capacitor should be connected to ground.

5.4 FCS TSOP Pinout Drawing

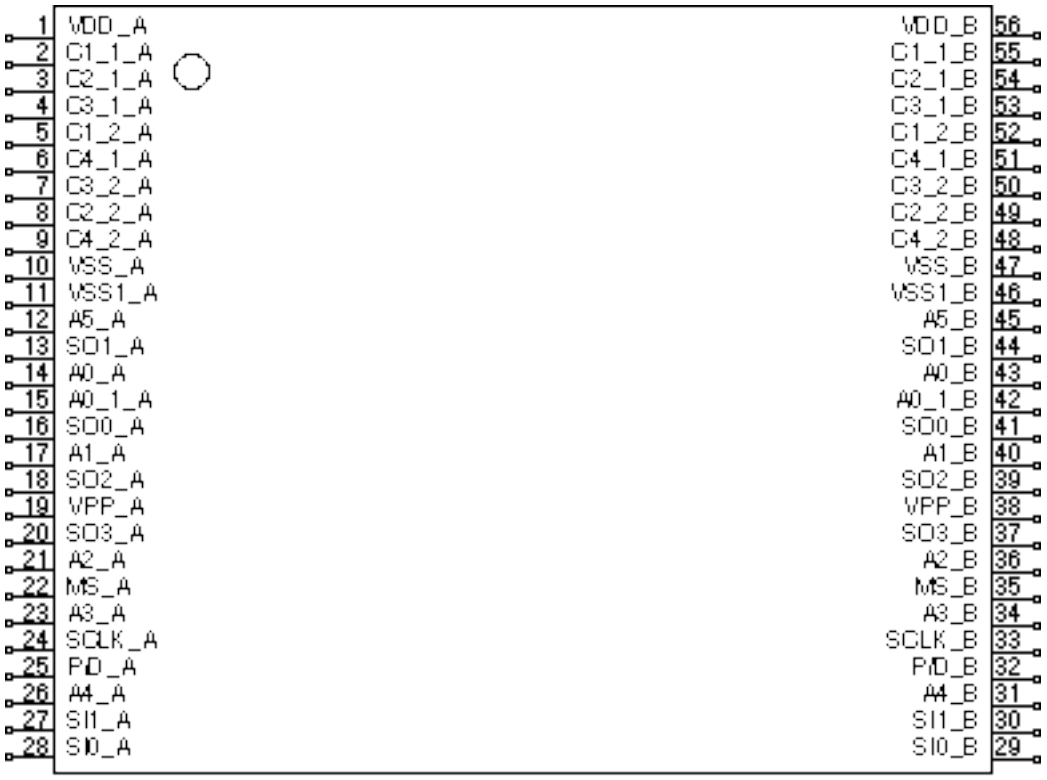


Figure 5-1 FCS TSOP Pinout Drawing

5.5 FCS TSOP Package Drawing

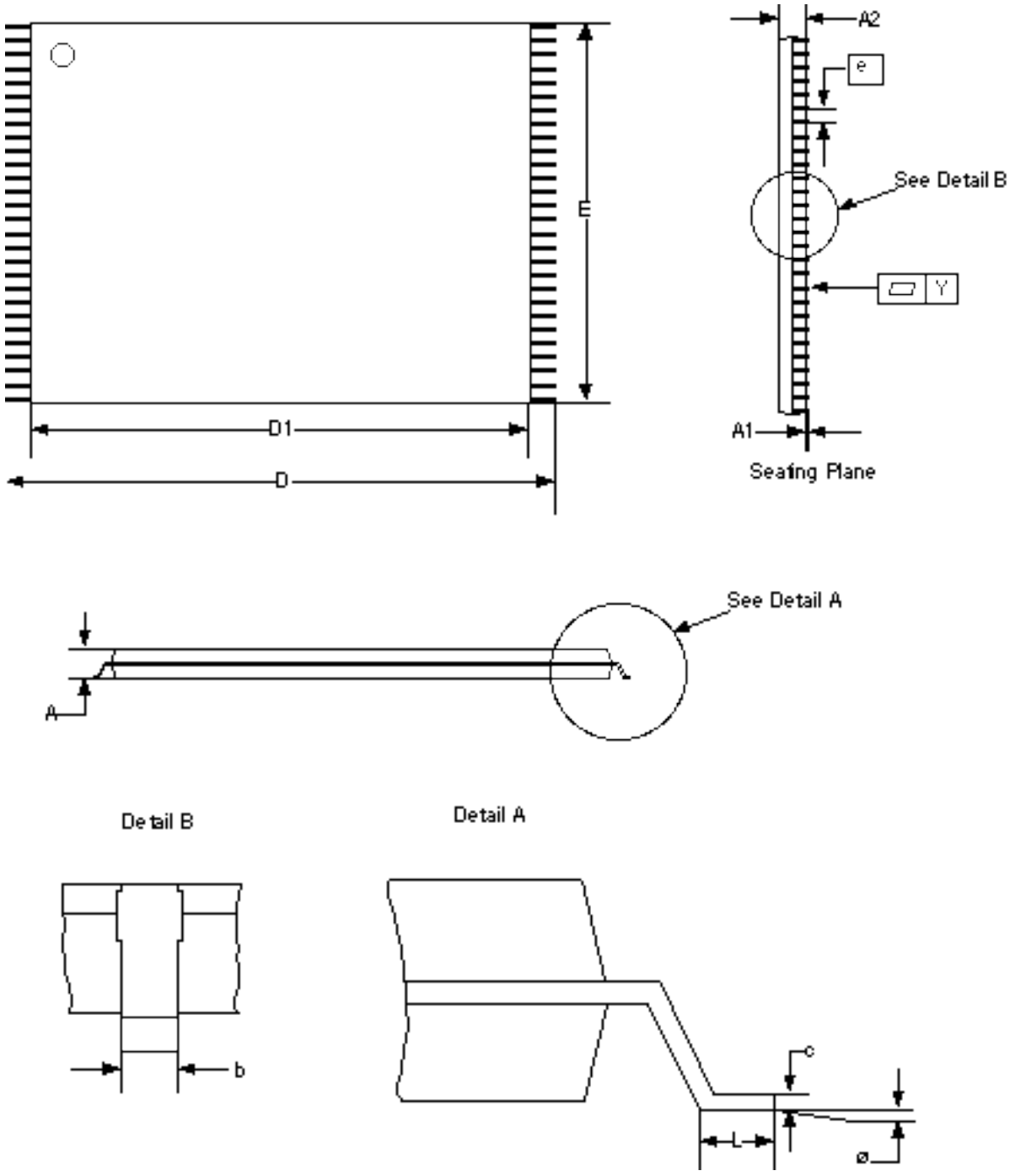


Figure 5-2 FCS TSOP Package Drawing

5.5 FCS TSOP Package Drawing Notes

56 Lead TSOP Specifications

		Millimeters				Inches		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.200				0.047
Standoff	A1	0.050				0.002		
Package Body Thickness	A2	0.95	0.10	1.05		0.038	0.039	0.040
Lead Width	b	0.100	0.150	0.200	1	0.004	0.006	0.008
Lead Thickness	c	0.10		0.16		0.0045	0.0049	0.0053
Package Body Length	D1	18.15	18.400	18.65		0.717	0.724	0.732
Package Body Width	E	13.800	14.000	14.200		0.543	0.551	0.559
Pitch	e		0.500				0.0197	
Terminal Dimension	D	19.800	20.000	20.200		0.780	0.787	0.795
Lead Tip Length	L		0.25			0.020	0.024	0.028
Lead Count	N		56				56	
Lead Tip Angle	ø	0°	3°	5°		0°	3°	5°
Seating Plane Coplanarity	Y			0.100				0.004

Note 1: Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition.
Note 2: Lead frame material—alloy 42.

Figure 5-2 FCS TSOP Package Drawing Notes

5.6 FCS TSOP Recommended Pad Structure

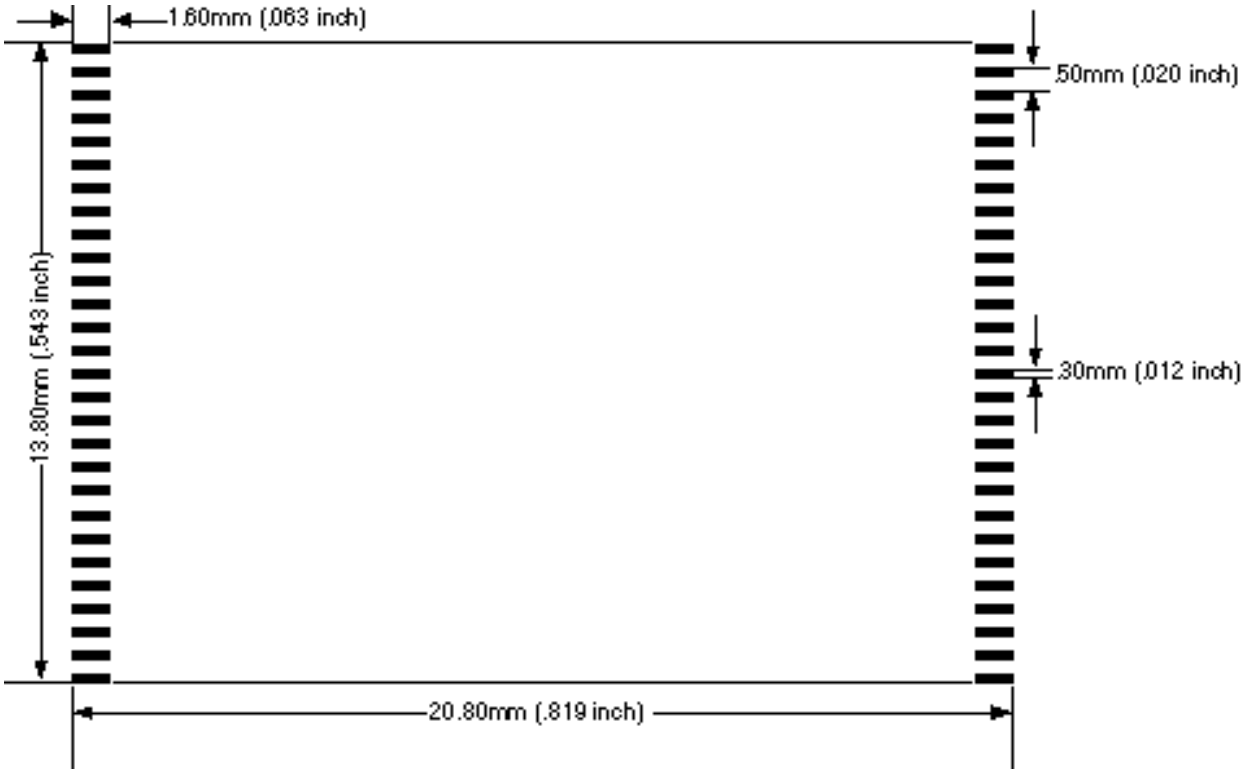


Figure 5-3 FCS TSOP Recommended Pad Structure

6.0 Flash ChipSet Electrical Interface Description

6.1 Interface/Bus Timing

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, a direct mapped I/O transfer and a memory access. The two timing sequences are explained in detail in the PCMCIA PC Card Standard Release 2.1. The Flash ChipSet conforms to the timing in that reference document.

6.2 Attribute Memory Read Timing Specification

The Attribute Memory access time is defined as 300 ns. Detailed timing specifications are shown in Table 6-1.

Table 6-1 Attribute Memory Read Timing

Speed Version			300 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVWL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

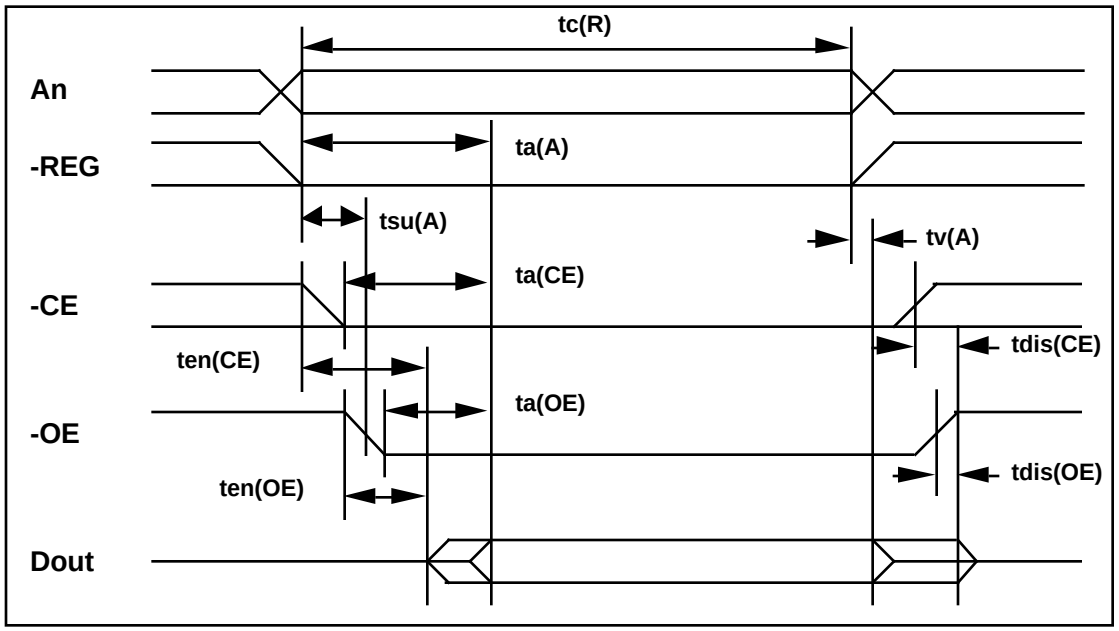


Figure 6-1 Attribute Memory Read Timing Diagram

Notes: All times are in nanoseconds. Dout signifies data provided by the Flash ChipSet to the system. The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

6.3 Attribute Memory Write Timing Specification

The Card Configuration write access time is defined as 250 ns. Detailed timing specifications are shown in Table 6-2.

Note: SanDisk does not allow writing from the Host to CIS Memory. Only writes to the Configuration register are allowed.

Table 6-2 Attribute Memory Write Timing

Speed Version			250 ns	
Item	Symbol	IEEE Symbol	Min ns	Max ns
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

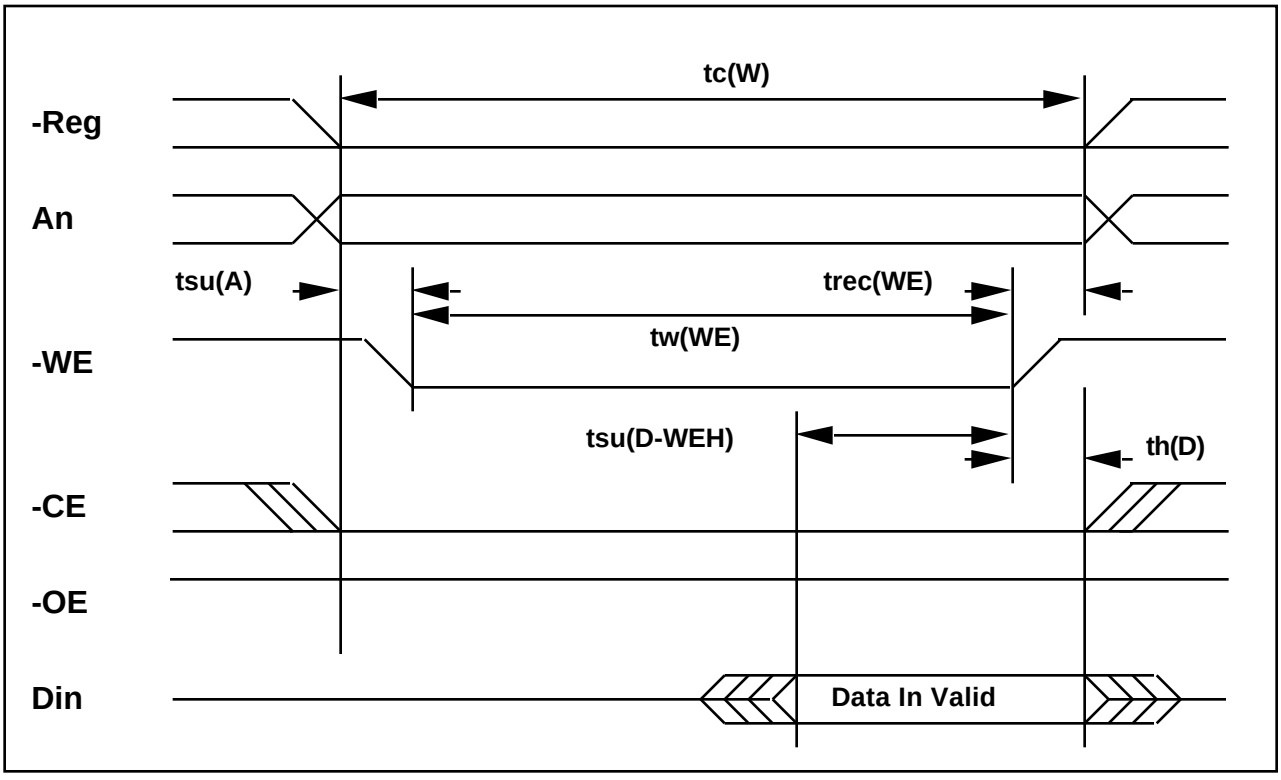


Figure 6-2 Attribute Memory Write Timing Diagram

Notes: All times are in nanoseconds.
Din signifies data provided by the system to the Flash ChipSet.

6.4 Common Memory Read Timing Specification

Table 6-3 Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Address Hold Time	th(A)	tGHAX	20	
CE Setup before OE	tsu(CE)	tELGL	0	
CE Hold following OE	th(CE)	tGHEH	20	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35
Data Setup for Wait Release	tv(WT)	tQVWTH		0
Wait Width Time (Default Speed)	tw(WT)	tWTLWTH		350

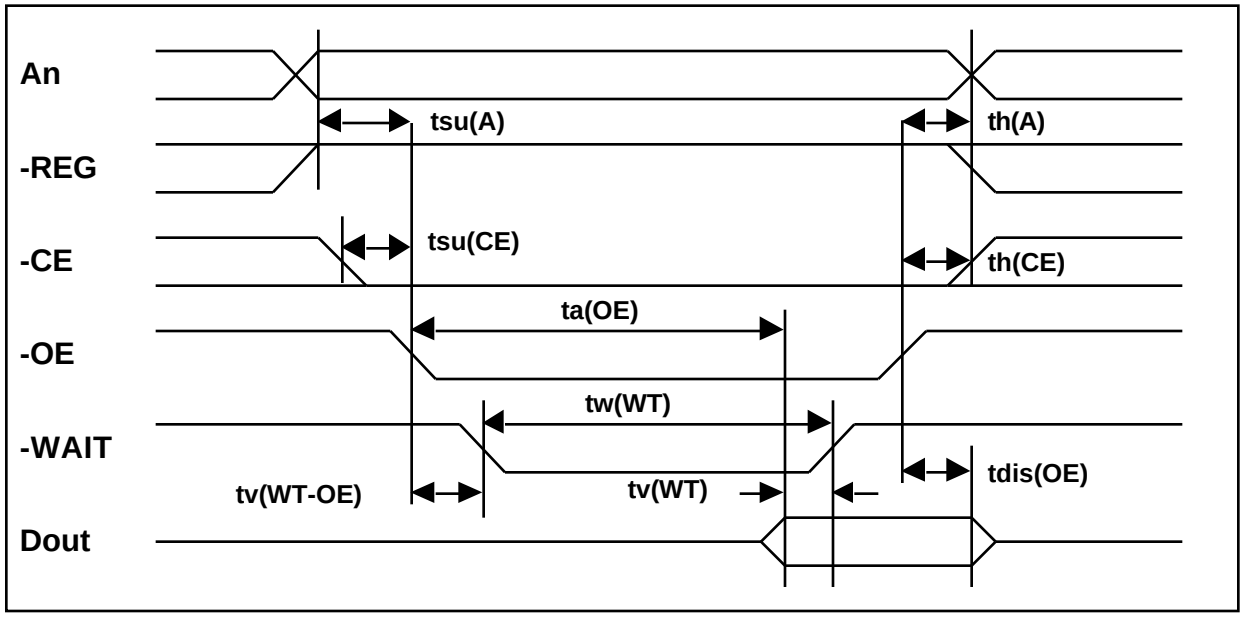


Figure 6-3 Common Memory Read Timing Diagram

Notes: The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Dout signifies data provided by the Flash ChipSet to the system.
The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time.
The Max Wait Width time (in the slowest mode) can be determined from the Card Information Structure.

6.5 Common Memory Write Timing Specification

Table 6-4 Common Memory Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before WE	tsu(D-WEH)	tDVWH	80	
Data Hold following WE	th(D)	tlWMDX	30	
WE Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
CE Setup before WE	tsu(CE)	tELWL	0	
Write Recovery Time	trec(WE)	tWMAX	30	
CE Hold following WE	th(CE)	tGHEH	20	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35
WE High from Wait Release	tv(WT)	tWTHWH	0	
Wait Width Time (Default Speed)	tw (WT)	tWTLWTH		350

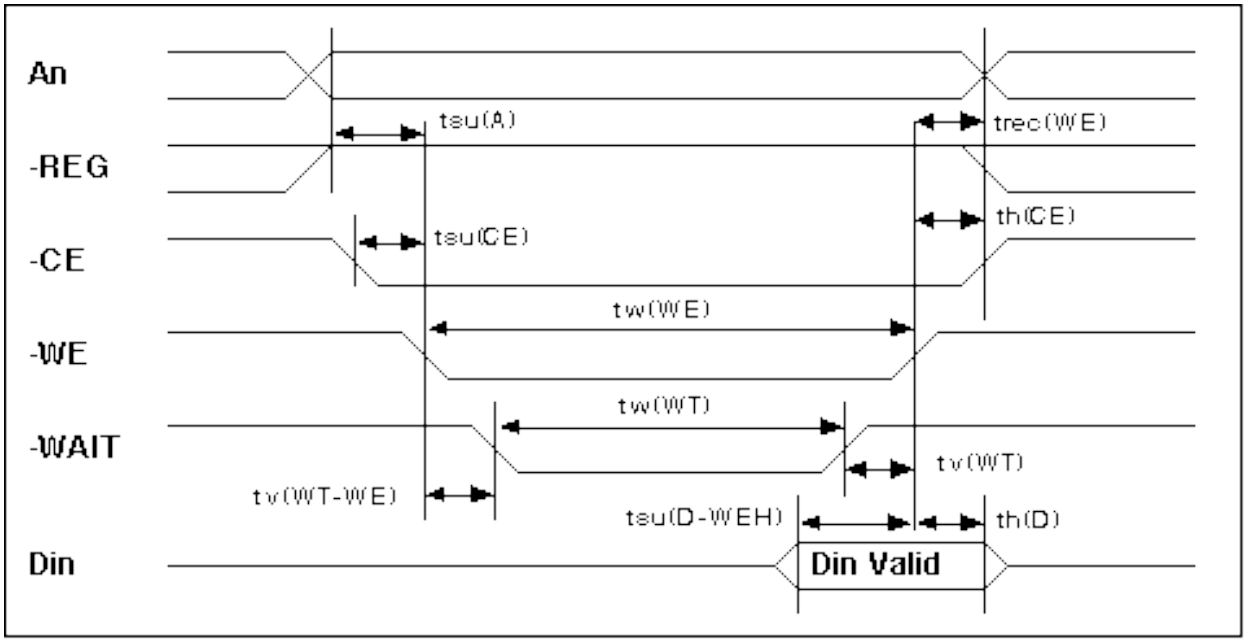


Figure 6-4 Common Memory Write Timing Diagram

Notes: The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Din signifies data provided by the system to the Flash ChipSet.
The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time.
The Max Wait Width time (in the slowest mode) can be determined from the Card Information Structure.

6.6 I/O Input (Read) Timing Specification

Table 6-5 I/O Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL		35
Data Delay from Wait Rising	td(WT)	tWTHQV		0
Wait Width Time (Default Speed)	tw(WT)	tWTLWTH		350

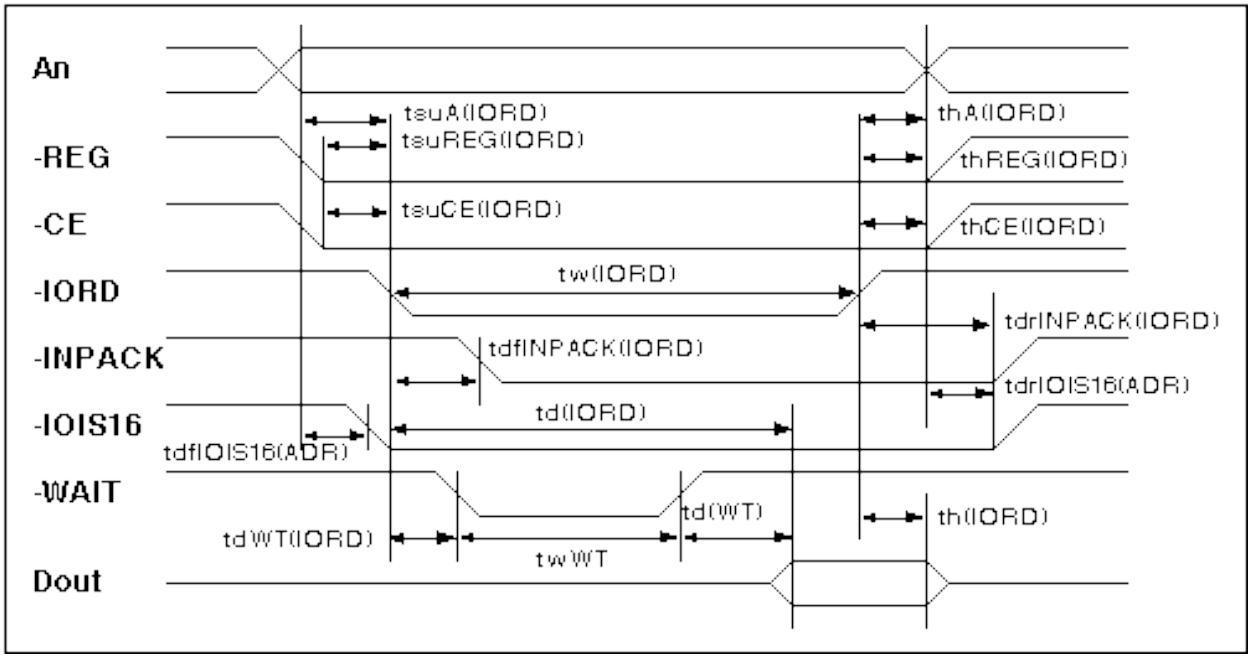


Figure 6-5 I/O Read Timing Diagram

Notes: The maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width must still be met.
Dout signifies data provided by the Flash ChipSet to the system.

6.7 I/O Output (Write) Timing Specification

Table 6-6 I/O Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	twIOWR	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL		35
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	
Wait Width Time (Default Speed) (Set Feature Speed <68 mA.)	tw(WT)	tWTLWTH		350 700

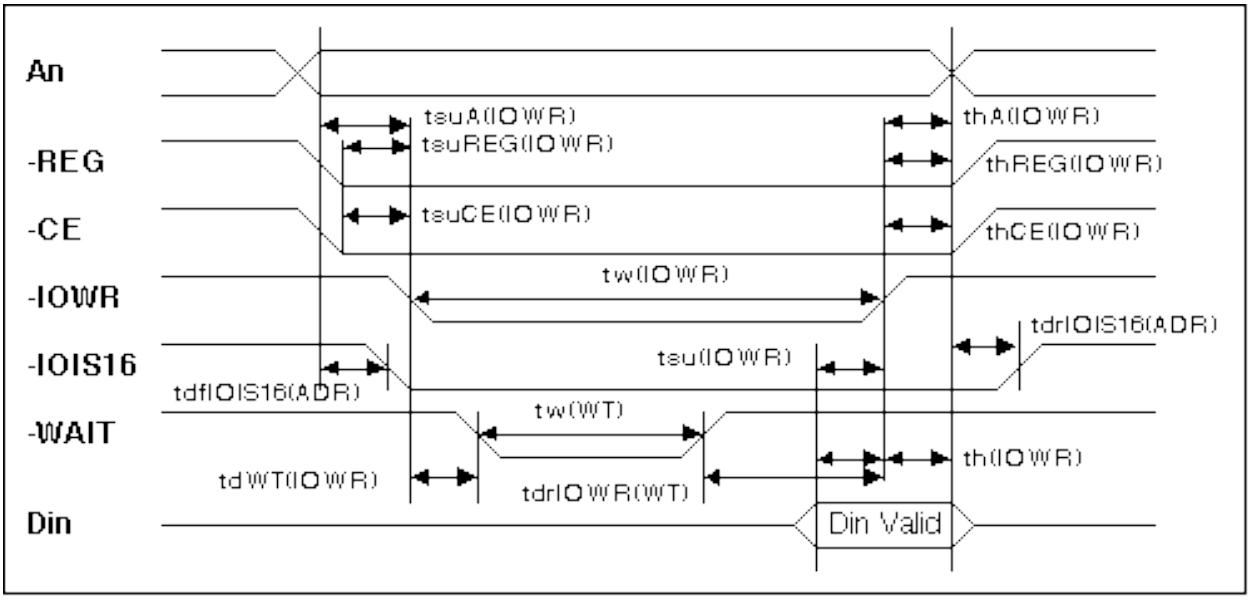


Figure 6-6 I/O Write Timing Diagram

Notes: The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width must still be met.
Din signifies data provided by the system to the Flash ChipSet.

6.8 True IDE Mode I/O Input (Read) Timing Specification

Table 6-7 True IDE Mode I/O Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tlGLQV		100
Data Hold following IORD	th(IORD)	tlGHQX	0	
IORD Width Time	tw(IORD)	tlGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tlGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tlGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

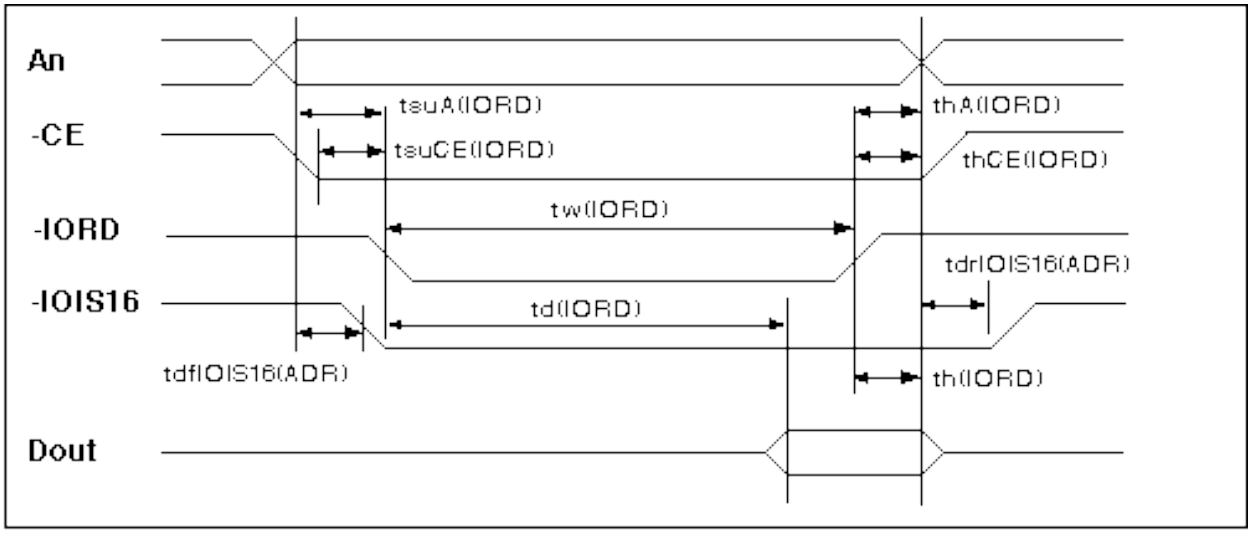


Figure 6-7 True IDE Mode I/O Read Timing Diagram

Notes: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width must still be met.
Dout signifies data provided by the Flash ChipSet to the system.

6.9 True IDE Mode I/O Output (Write) Timing Specification

Table 6-8 True IDE Mode I/O Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

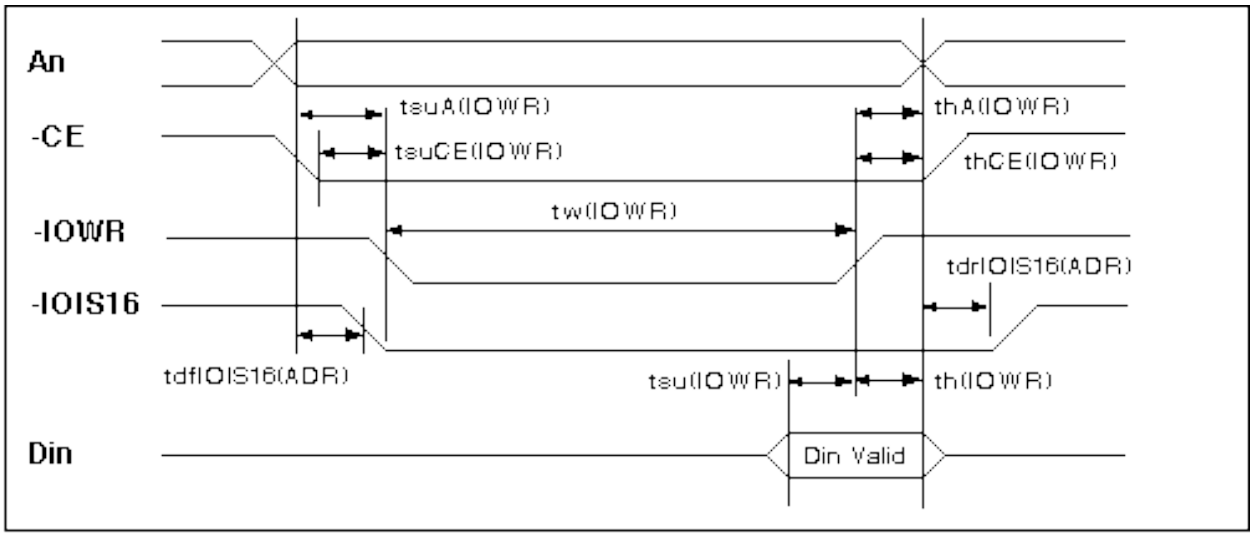


Figure 6-8 True IDE Mode I/O Write Timing Diagram

Notes: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width must still be met.
Din signifies data provided by the system to the Flash ChipSet.

7.0 Card Configuration

The Flash ChipSet is identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the Flash ChipSet that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

Table 7-1 Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Note: The location of the card configuration registers should always be read from the CIS since these locations may vary in future products. No writes should be performed to the Flash ChipSet attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

7.1 Attribute Memory Function

Attribute memory is a space where Flash ChipSet identification and configuration information is stored, and is limited to 8-bit wide accesses only at even addresses. The card configuration registers are also located here.

For the Attribute Memory Read function, signals -REG and -OE must be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 7-2 below for signal states and bus validity for the Attribute Memory function.

Table 7-2 Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	H	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	H	X	H	L	Don't Care	Even Byte

Note: The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

7.2 Configuration Option Register (Address 200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the Flash ChipSet.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET Soft Reset - Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the Flash ChipSet in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the Flash ChipSet in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevlREQ This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5 - Conf0 Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the Flash ChipSet as shown below.

Note: Conf5 and Conf4 are reserved and must be written as zero (0)

Table 7-3 Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	I/O Mapped, 170-177/376-377

7.3 Card Configuration and Status Register (Address 202h in Attribute Memory)

The Card Configuration and Status Register contains information about the Flash ChipSet's condition.

Card Configuration and Status Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed Indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the Flash ChipSet is configured for the I/O interface.

SigChg This bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the Flash ChipSet is configured for I/O.

IOis8 The host sets this bit to a one (1) if the Flash ChipSet is to be configured in an 8 bit I/O mode. The Flash ChipSet is always configured for both 8- and 16-bit I/O, so this bit is ignored.

PwrDwn This bit indicates whether the host requests the Flash ChipSet to be in the power saving or active mode. When the bit is one (1), the Flash ChipSet enters a power down mode. When zero (0), the host is requesting the Flash ChipSet to enter the active mode. The PCMCIA Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The Flash ChipSet automatically powers down when it is idle and powers back up when it receives a command.

Int This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

7.4 Pin Replacement Register (Address 204h in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	RRdy/-Bsy	RWProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

CRdy/-Bsy This bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

CWProt This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

RRdy/-Bsy This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

RWProt This bit is always zero (0) since the Flash ChipSet does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRdy/-Bsy This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

MWProt This bit when written acts as a mask for writing the corresponding bit CWProt.

Table 7-4 Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final	Comments
	"C" Bit	"M" Bit	"C" Bit	
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

7.5 Socket and Copy Register (Address 206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the Flash ChipSet's Configuration Index Register.

Socket and Copy Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive # (0)	X	X	X	X

Reserved This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive # This bit indicates the drive number of the card if twin card configuration is supported. This revision of the Flash ChipSet does not support twin card configuration therefore this bit must be a zero (0).

X The socket number is ignored by the Flash ChipSet.

7.6 I/O Transfer Function

7.6.1 I/O Function

The I/O transfer to or from the Flash ChipSet can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal -IOIS16 is asserted by the Flash ChipSet. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the Flash ChipSet, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The Flash ChipSet permit both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the Flash ChipSet responds.

The Flash ChipSet may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 7-5 I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

7.7 Common Memory Transfer Function

7.7.1 Common Memory Function

The Common Memory transfer to or from the Flash ChipSet can be either 8 or 16 bits.

The Flash ChipSet permits both 8 and 16 bit accesses to all of its Common Memory addresses.

The Flash ChipSet may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 7-6 Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte ReadAccess (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

7.8 True IDE Mode I/O Transfer Function

7.8.1 True IDE Mode I/O Function

The Flash ChipSet can be configured in a True IDE Mode of operation. Flash ChipSets are configured in this mode only when the -OE input signal is asserted low by the host during the power off to power on cycle. In this True IDE Mode, the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode, no Memory or Attribute Registers are accessible to the host. Flash ChipSets permit 8 bit data accesses if the user issues a Set Feature Command to put the device in 8 bit Mode.

Note: Removing and reinserting a device with the Flash ChipSet while the host computer's power is on will reconfigure the Flash ChipSet to PC Card ATA mode from the original True IDE Mode. To configure the Flash ChipSet in True IDE Mode, the 68-pin socket must be power cycled with the device with the Flash ChipSet inserted and -OE (output enable) asserted.

The following table defines the function of the operations for the True IDE Mode.

Table 7-7 IDE Mode I/O Function

Function Code	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out

8.0 ATA Drive Register Set Definition and Protocol

The Flash ChipSet can be configured as a high performance I/O device through:

a.) Standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary); 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).

b.) Any system decoded 16 byte I/O block using any available IRQ.

c.) Memory space.

The communication to or from the Flash ChipSet is done using the Task File registers which provide all the necessary registers for control and status information. The PCMCIA interface connects peripherals to the host using four register mapping methods. The following is a detailed description of these methods:

Table 8-1 I/O Configurations

Standard Configurations				
Config Index	**IO or Memory**	**Address**	**Drive #**	**Description**
0	Memory	0-F, 400-7FF	0	Memory Mapped
1	I/O	XX0-XXF	0	I/O Mapped 16 Contiguous Registers
2	I/O	1F0-1F7, 3F6-3F7	0	Primary I/O Mapped Drive 0
2	I/O	1F0-1F7, 3F6-3F7	1	Primary I/O Mapped Drive 1
3	I/O	170-177, 376-377	0	Secondary I/O Mapped Drive 0
3	I/O	170-177, 376-377	1	Secondary I/O Mapped Drive 1

8.1 I/O Primary and Secondary Address Configurations

Table 8-2 Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)	0	0	0	0	Even RD Data	Even WR Data	1, 2
0	1F(17)	0	0	0	1	Error Register	Features	1
0	1F(17)	0	0	1	0	Sector Count	Sector Count	
0	1F(17)	0	0	1	1	Sector No.	Sector No.	
0	1F(17)	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)	0	1	1	1	Status	Command	
0	3F(37)	0	1	1	0	Alt Status	Device Control	
0	3F(37)	0	1	1	1	Drive Address	Reserved	

Notes: 1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers which lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

2. A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

8.2 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the Flash ChipSet, the registers are accessed in the block of I/O space decoded by the system as follows:

Table 8-3 Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card /Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

Notes: 1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.
Repeated byte accesses to register 8 or 0 will access consecutive (even than odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Address lines which are not indicated are ignored by the Flash ChipSet for accessing all the registers in this table.

8.3 Memory Mapped Addressing

When the Flash ChipSet registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as follows:

Table 8-4 Memory Mapped Decoding

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	X	0	0	0	1	1	Error	Features	2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card /Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

Notes: 1. Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.
Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 Kbyte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.
Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the Flash ChipSet.

8.4 True IDE Mode Addressing

When the Flash ChipSet is configured in the True IDE Mode the I/O decoding is as follows:

Table 8-5 True IDE Mode I/O Decoding

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0	Note
1	0	0	0	0	Even RD Data	Even WR Data	
1	0	0	0	1	Error Register	Features	
1	0	0	1	0	Sector Count	Sector Count	
1	0	0	1	1	Sector No.	Sector No.	
1	0	1	0	0	Cylinder Low	Cylinder Low	
1	0	1	0	1	Cylinder High	Cylinder High	
1	0	1	1	0	Select Card/Head	Select Card/Head	
1	0	1	1	1	Status	Command	
0	1	1	1	0	Alt Status	Device Control	
0	1	1	1	1	Drive Address	Reserved	

8.5 ATA Registers

Note: In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted) and an I/O cycle is being performed.

8.5.1 Data Register (Address - 1F0[170]; Offset 0,8,9)

The Data Register is a 16 bit register, and it is used to transfer data blocks between the Flash ChipSet data buffer and the host. This register overlaps the Error Register. The table below describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

Note that because of the overlapped registers, access to the 1F1, 171 or offset 1 are not defined for word (-CE2 = 0 and -CE1 = 0) operations. SanDisk products treat these accesses as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed by the socket.

Data Register	CE2-	CE1-	A0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	D15-D0
Even Data Register	1	0	0	0,8	D7-D0
Odd Data Register	1	0	1	9	D7-D0
Odd Data Register	0	1	X	8,9	D15-D8
Error / Feature Register	1	0	1	1, Dh	D7-D0
Error / Feature Register	0	1	X	1	D15-D8
Error / Feature Register	0	0	X	Dh	D15-D8

8.5.2 Error Register (Address - 1F1[171]; Offset 1, 0Dh Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -CE2 low and -CE1 high.

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a Flash ChipSet status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

8.5.3 Feature Register (Address - 1F1[171]; Offset 1, 0Dh Write Only)

This register provides information regarding features of the Flash ChipSet that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high.

8.5.4 Sector Count Register (Address - 1F2[172]; Offset 2)

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the Flash ChipSet. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

8.5.5 Sector Number (LBA 7-0) Register (Address - 1F3[173]; Offset 3)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any Flash ChipSet data access for the subsequent command.

8.5.6 Cylinder Low (LBA 15-8) Register (Address - 1F4[174]; Offset 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

8.5.7 Cylinder High (LBA 23-16) Register (Address - 1F5[175]; Offset 5)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

8.5.8 Drive/Head (LBA 27-24) Register (Address 1F6[176]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.

Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5 This bit is set to 1.

Bit 4 (DRV) This bit will have the following meaning. DRV is the drive number. When DRV=0, drive (card) 0 is selected When DRV=1, drive (card) 1 is selected. The Flash ChipSet is set to be Card 0 or 1 using the copy field of the PCMCIA Socket & Copy configuration register.

Bit 3 (HS3) When operating in the Cylinder , Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

8.5.9 Status & Alternate Status Registers (Address 1F7[177] & 3F6[376]; Offsets 7 & Eh)

These registers return the Flash ChipSet status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the Flash ChipSet Card has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing Flash ChipSet operations. This bit is cleared at power up and remains cleared until the Flash ChipSet is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the Flash ChipSet is ready.

Bit 3 (DRQ) The Data Request is set when the Flash ChipSet requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

8.5.10 Device Control Register (Address - 3F6[376]; Offset Eh)

This register is used to control the Flash ChipSet interrupt request and to issue an ATA soft reset to the card. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is an X (don't care).

Bit 6 This bit is an X (don't care).

Bit 5 This bit is an X (don't care).

Bit 4 This bit is an X (don't care).

Bit 3 This bit is ignored by the Flash ChipSet.

Bit 2 (SW Rst) This bit is set to 1 in order to force the Flash ChipSet to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration Registers (7.2 to 7.5) as a hardware Reset does. The Card remains in Reset until this bit is reset to '0.'

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the Flash ChipSet are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 1 at power on and Reset.

Bit 0 This bit is ignored by the Flash ChipSet.

8.5.11 Card (Drive) Address Register (Address 3F7[377]; Offset Fh)

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.
Implementation Note:
Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the Flash ChipSet. Following are some possible solutions to this problem for the PCMCIA implementation:
1. Locate the Flash ChipSet at a non-conflicting address, i.e. Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses.
2. Do not install a Floppy and a Flash ChipSet in the system at the same time.
3. Implement a socket adapter which can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a Flash ChipSet is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use Flash ChipSet's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the Flash ChipSet or b) if provided use an additional Primary / Secondary configuration in the Flash ChipSet which does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

9.0 ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the Flash ChipSet. Commands are issued to the Flash ChipSet by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 9-1) of command acceptance, all dependent on the host not issuing commands unless the Flash ChipSet is not busy. (The BUSY bit in the status and alternate status registers is 0.)

- Upon receipt of a Class 1 command, the Flash ChipSet sets the BUSY bit within 400 nsec.
- Upon receipt of a Class 2 command, the Flash ChipSet sets the BUSY bit within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 µsec, and clears the BUSY bit within 400 nsec of setting DRQ.
- Upon receipt of a Class 3 command, the Flash ChipSet sets the BUSY bit within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec (assuming no re-assignments), and clears the BUSY bit within 400 nsec of setting DRQ.

9.1 ATA Command Set

Table 9-1 summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 9-1 ATA Command Set

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Drive Diagnostic	90h	-	-	-	-	D	-
1	Erase Sector(s) (Note 1)	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Drive	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense (Note 1)	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Stand By	E2h or 96h	-	-	-	-	D	-
1	Stand By Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector (Note 1)	87h	-	Y	Y	Y	Y	Y
1	Wear Level (Note 1)	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase (1)	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase (1)	38h	-	Y	Y	Y	Y	Y
2	Write Verify Sector(s)	3Ch	-	Y	Y	Y	Y	Y

Note 1: This command is not a standard PC Card ATA command but provides additional functionality.
Definitions: FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Card/Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use).
Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the Flash ChipSet and head parameters are used; D - only the Flash ChipSet parameter is valid and not the head parameter.

9.1.1 Check Power Mode - 98H, E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E5H or 98H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode.

If the Flash ChipSet is in, going to, or recovering from the sleep mode, the Flash ChipSet sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the Flash ChipSet is in Idle mode, the Flash ChipSet sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

9.1.2 Execute Drive Diagnostic - 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command performs the internal diagnostic tests implemented by the Flash ChipSet.

The Diagnostic codes shown in Table 9-2 are returned in the Error Register at the end of the command.

Table 9-2 Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Failed (True IDE Mode)

9.1.3 Erase Sector(s) - C0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but since an implied write ID (header) operation is performed, a Write Fault error status can occur.

9.1.4 Format Track - 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

This command writes the desired head and cylinder of the selected drive with a FFh pattern. To remain host backward compatible, the Flash ChipSet expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the Flash ChipSet. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256).

9.1.5 Identify Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify Drive command enables the host to receive parameter information from the Flash ChipSet. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 9-3. All reserved bits or words are zero. Table 9-3 is the definition for each field in the Identify Drive Information.

Table 9-3 Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848AH	2	General configuration bit-significant information
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	XXXXH	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	0240H	2	Number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7-8	XXXX	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000H	2	Reserved
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0002H	2	Buffer type (dual ported)
21	0002H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII (Rev M.ms) set by code Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0200H	2	Capabilities: DMA NOT Supported (bit 8), LBA supported (bit 9)
50	0000H	2	Reserved
51	0100H	2	PIO data transfer cycle timing mode 1
52	0000H	2	DMA data transfer cycle timing mode Not Supported
53	0001H	2	Translation parameters are valid
54	XXXX	2	Current numbers of cylinders
55	XXXX	2	Current numbers of heads
56	XXXX	2	Current sectors per track
57-58	XXXX	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	010XH	2	Multiple sector setting is valid
60-61	XXXX	4	Total number of sectors addressable in LBA Mode
62-127	0000H	138	Reserved
128-159	0000H	64	Reserved vendor unique bytes
160-255	0000H	192	Reserved

9.1.5.1 General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 mb/sec and is not MFM encoded.

9.1.5.2 Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

9.1.5.3 Default Number of Heads

This field contains the number of translated heads in the default translation mode.

9.1.5.4 Number of Unformatted Bytes per Track

This field contains the number of unformatted bytes per translated track in the default translation mode.

9.1.5.5 Number of Unformatted Bytes per Sector

This field contains the number of unformatted bytes per sector in the default translation mode.

9.1.5.6 Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

9.1.5.7 Number of Sectors per Card

This field contains the number of sectors per Flash ChipSet. This double word value is also the first invalid address in LBA translation mode.

9.1.5.8 Memory Card Serial Number

The contents of this field are right justified and padded with spaces (20h).

9.1.5.9 Buffer Type

This field defines the buffer capability with the 0002h meaning a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the Flash ChipSet.

9.1.5.10 Buffer Size

This field defines the buffer capacity of 2 sectors or 1 kilobyte of SRAM.

9.1.5.11 ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands.

9.1.5.12 Firmware Revision

This field contains the revision of the firmware for this product.

9.1.5.13 Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

9.1.5.14 Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

9.1.5.15 Double Word Support

This field indicates this product will not support double word transfers.

9.1.5.16 Capabilities

This field indicates this product will not support DMA Data transfers but does support LBA mode.

9.1.5.17 PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer.

9.1.5.18 DMA Data Transfer Cycle Timing Mode

This field states this product doesn't support any DMA data transfer mode.

9.1.5.19 Translation Parameters Valid

This field contains the value 0001h indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors.

9.1.5.20 Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

9.1.5.21 Current Capacity

This field contains the product of the current cylinders times heads times sectors.

9.1.5.22 Multiple Sector Setting

This field contains a validity flag in the odd byte and the current number of sectors that can be transferred per interrupt for R/W Multiple in the even byte. The odd byte is always 01H which indicates that the even byte is always valid.

The even byte value depends on the value set by the Set Multiple command. The even byte of this word by default contains a 00H which indicates that R/W Multiple commands are not valid. The only other value returned by the Flash ChipSet in the even byte is a 01H value which indicates that 1 sector per interrupt can be transferred in R/W Multiple mode.

9.1.5.23 Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the Flash ChipSet in LBA mode only.

9.1.6 Idle - 97H, E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E3H or 97H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the Flash ChipSet to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

9.1.7 Idle Immediate - 95H, E1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E1H or 95H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the Flash ChipSet to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

9.1.8 Initialize Drive Parameters - 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

Note: SanDisk recommends NOT using this command in any system because DOS determines the offset to the Boot Record based on the number of heads and sectors per track. If a Flash ChipSet is "formatted" with one head and sector per track value, the same Flash ChipSet will not operate correctly with DOS configured with another heads and sectors per track value.

9.1.9 Read Buffer - E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Buffer command enables the host to read the current contents of the Flash ChipSet's sector buffer. This command has the same protocol as the Read Sector(s) command.

9.1.10 Read Multiple - C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the Flash ChipSet only supports a block count of 1 as indicated in the Identify Drive Information command. This command is provided for compatibility with future products which may support a larger block count.

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = (sector count) - modulo (block count).

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

9.1.11 Read Long Sector - 22H, 23H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22H or 23H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the Flash ChipSet does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of random data transferred in byte mode. Random data is returned instead of ECC bytes because of the nature of the ECC system used. This command has the same protocol as the Read Sector(s) command.

9.1.12 Read Sector(s) - 20H, 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H or 21H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the Flash ChipSet sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

9.1.13 Read Verify Sector(s) - 40H, 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the Flash ChipSet sets BSY.

When the requested sectors have been verified, the Flash ChipSet clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

9.1.14 Recalibrate - 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the Flash ChipSet and is provided for compatibility purposes. After this command is executed the Cyl High and Cyl Low as well as the Head number will be 0 and Sec Num will be 1 if LBA=0 and 0 if LBA=1 (i.e. the first block in LBA is 0 while CHS mode the sector number starts at 1).

9.1.15 Request Sense - 03H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03H							
C/D/H (6)	1	X	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests an extended error code after a command ends with an error. Table 9-4 defines the valid extended error codes for the Flash ChipSet. The extended error code is returned to the host in the Error Register. This command must be the next command issued to the Flash ChipSet following the command which returned an error.

Table 9-4 Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38H, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed

9.1.16 Seek - 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the Flash ChipSet although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

9.1.17 Set Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 9-5 defines all features that are supported. Please note that the 9AH feature is unique to the Flash ChipSet and are not part of the ATA Specification.

Table 9-5 Features Supported

Feature	Operation
01H	Enable 8 bit data transfer.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69H	Accepted for backward compatibility with the SDP Series but has no impact on the Flash ChipSet.
81H	Disable 8 bit data transfer.
96H	Accepted for backward compatibility with the SDP Series but has no impact on the Flash ChipSet.
9AH	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
BBH	4 bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01H and 81H are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01H feature command is issued, all data transfers will occur on the low order D7-D0 data bus and the IOIS16 signal will not be asserted for data register accesses.

Features 55H and BBH are the default features for the Flash ChipSet; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

The 9AH Feature is a Flash ChipSet unique option that provides a mechanism for the host system to adjust how much current the Flash ChipSet will use. The Flash ChipSet reduces the current drawn by reducing operating frequency. This has the impact of also reducing the performance of the Flash ChipSet. The default for the Flash ChipSet, after a power on reset, is to operate at the highest performance and therefore the highest current mode. However after a power on, the Flash ChipSet will not draw more than the minimum current as long as the host does not issue any command which reads or writes to the flash memory. This allows the host to issue the Set Features command to set the desired power level without exceeding the minimum requirement of the Flash ChipSet.

To reduce the current the Flash ChipSet draws, the host issues the Set Features command with the Feature register set to 9AH and the Sector Count register (Config) set to a current value which is equal to 4 mA times the value in the Sector Count register. When this is done, the controller will utilize a look-up table to program the controller's frequency, microprocessor's speed and flash clocks with an optimum value to provide the highest performance without exceeding the host's current limit. For example, if a host can supply 75 mA of current to the Flash ChipSet, the Sector Count register would be set to 75 divided by 4 (rounded down) or a value of 18. The Flash ChipSet would then automatically reduce its clock frequencies so that it will not draw more than 75 mA (average, at nominal Vcc and room temperature) of current. If the host always wanted to operate at the lowest possible current, the Sector Count value should be set to 1. The Flash ChipSet will then operate at the lowest possible current (and also the lowest performance).

At the completion of this command, the controller will update the Cylinder Low register with the controller's minimum valid current value (i.e. the minimum current with which the Flash ChipSet can operate) and the Cylinder High register with the maximum current it will use (i.e. the maximum current the Flash ChipSet will draw at the highest performance level). The controller will use its minimum value for any Sector Count value which is less than its minimum value. For example, if the Sector Count is set to 4 which is equivalent to 16 mA, the controller will operate at the lowest possible power point but will not reject the command. Similarly the controller will use its maximum value for any Sector Count value which is more than the maximum current it can use.

There is no error associated with the 9AH feature.

Features 66H and CCH can be used to enable and disable whether the Power On Reset (POR) Defaults will be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs. POR defaults the number of heads and sectors along with 16 bit data transfers and the read / write multiple block count.

9.1.18 Set Multiple Mode - C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the Flash ChipSet to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. The current version of the Flash ChipSet supports only a block size of 1 sector per block. Future versions may support larger block sizes. Upon receipt of the command, the Flash ChipSet sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

9.1.19 Set Sleep Mode- 99H, E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E6H or 99H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the Flash ChipSet to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the read to sleep timer is 5 milliseconds. Note that this time base (5 msec) is different from the ATA Specification.

9.1.20 Standby - 96H, E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E2H or 96H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the Flash ChipSet to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

9.1.21 Standby Immediate - 94H, E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E0H or 94H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the Flash ChipSet to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

9.1.22 Translate Sector - 87H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 byte buffer of information on the desired cylinder, head and sector with the actual Logical Address along with the Hot Count for that sector. Table 9-6 represents the information in the buffer. Please note that this command is unique to the SanDisk Flash ChipSet.

Table 9-6 Translate Sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased 00h = Not Erased
14h - 17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A)
1Bh-1FFh	Reserved

9.1.23 Wear Level - F5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5H							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

This command is effectively a NOP command and only implemented for backward compatability with earlier SanDisk SDP series products. The Sector Count Register will always be returned with an 00H indicating Wear Level is not needed.

9.1.24 Write Buffer - E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write Buffer command enables the host to overwrite contents of the Flash ChipSet's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

9.1.25 Write Long Sector - 32H, 33H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32H or 33H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state Flash ChipSet, the four bytes of ECC transferred by the host cannot be used by the Flash ChipSet. The Flash ChipSet discards these four bytes and writes the sector with valid ECC fields. This command has the same protocol as the Write Sector(s) command.

9.1.26 Write Multiple Command - C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the Flash ChipSet only supports a block count of 1 as indicated in the Identify Drive Command information. This command is provided for compatibility with future products which may support a larger block count.

This command is similar to the Write Sectors command. The Flash ChipSet sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector / block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = remainder (sector count / block count).

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

9.1.27 Write Multiple without Erase - CDH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDH							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued.

9.1.28 Write Sector(s) - 30H, 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H or 31H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the Flash ChipSet sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

9.1.29 Write Sector(s) without Erase - 38H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased with the Erase Sector(s) command, a normal write sector operation will occur.

This command is much faster than a Write Sector(s) command if the sector is pre-erased. The overall performance of the combined Erase Sector(s) command along with the Write Sector(s) without Erase command is less than the normal Write Sector(s) command but has the advantage of splitting up the overall time so the write only portion is more than two times the transfer rate of the normal Write Sector(s) command.

9.1.30 Write Verify Sector(s) - 3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3CH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the Flash ChipSet sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

9.2 Error Posting

The following table summarizes the valid status and error value for all the ATA Command set.

Table 9-7 Error and Status Register

	Error Register					Status Register				
Command	**BBK**	**UNC**	**IDNF**	**ABRT**	**AMNF**	**DRDY**	**DWF**	**DSC**	**CORR**	**ERR**
Check Power Mode				V		V	V	V		V
Execute Drive Diagnostic*						V		V		V
Erase Sector(s)	V		V	V	V	V	V	V		V
Format Track			V	V	V	V	V	V		V
Identify Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Drive Parameters						V		V		V
Read Buffer				V		V	V	V		V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request Sense				V		V		V		V
Seek			V	V		V	V	V		V
Set Features				V		V	V	V		V
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Stand By				V		V	V	V		V
Stand By Immediate				V		V	V	V		V
Translate Sector	V		V	V	V	V	V	V		V
Wear Level	V	V	V	V	V	V	V	V		V
Write Buffer				V		V	V	V		V
Write Long Sector	V		V	V	V	V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V
Write Multiple w/o Erase	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Sector(s) w/o Erase	V		V	V	V	V	V	V		V
Write Verify Sector(s)	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

V = valid on this command
* See Table 9-2.

10.0 CIS Description

This section describes the Card Information Structure (CIS) for the Flash ChipSet. This section is only applicable if the Flash ChipSet is being designed into a PCMCIA product.

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
000h	01h	CISTPL_DEVICE								Device Info Tuple	Tuple Code
002h	04h									Link is 4 bytes	Link to next tuple
004h	DFh	Dev ID Type Dh = I/O				W 1	Speed 7h = ext			I/O Device, No WPS, ext speed	Device ID, WPS, Speed
006h	72h	X	Spd Mantis Eh == 7.0				Spd Expo 2h=100 nsec			700 nsec if no wait	Extended Speed
008h	01h	1x					2K units			2 Kilobytes of Address Space	Device Size
00Ah	FFh	List End Marker								End of Devices	End Marker
00Ch	1Ch	CISTPL_DEVICE_OC								Other Conditions Info Tuple	Tuple Code
00Eh	04h									Link is 4 bytes	Link to next tuple
010h	03h	Reserved 0						3 0	W 1	Conditions: 3V operation is allowed, and WAIT is used	3 Volts Operation, Wait Function
012h	D9h	Dev ID Type Dh = I/O				W 1	Speed 01h=250nsec			I/O Device, No WPS, Speed is 250 nsec with Wait	Device ID, WPS, Speed
014h	01h	1x					2K units			2Kilobytes of Address Space	Device Size
016h	FFh	List End Marker								End of Devices	End Marker
018h	18h	CISTPL_JEDEC_C								JEDEC ID Common Mem	Tuple Code
01Ah	02h									Link is 2 bytes	Link Length
01Ch	DFh	PCMCIA JEDEC Manufacturer's ID								First Byte of JEDEC ID for SanDisk PC Card-ATA 12V	Byte 1, JEDEC ID of Device 1 (0-2K)
01Eh	01h	PCMCIA Code for PC Card-ATA No Vpp Required								Second Byte of JEDEC ID	Byte 2, JEDEC ID
020h	20h	CISTPL_MANFID								Manufacturer's ID Tuple	Tuple Code
022h	04h									Link is 4 bytes	Link Length
024h	45h	Low Byte of PCMCIA Manufacturer's Code								SanDisk JEDEC Manufacturer's ID	Low Byte of PCMCIA Mfg ID
026h	00h	High Byte of PCMCIA Manufacturer's Code								Code of 0 because other byte is JEDEC 1 byte Manufacturer's ID	High Byte of PCMCIA Mfg ID
028h	01h	Low Byte of Product Code								SanDisk Code for SDP Series	Low Byte Product Code
02Ah	04h	High Byte of Product Code								SanDisk Code for PC CARD ATA	High Byte Product Code

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
02Ch	15h	CISTPL_VER_1								Level 1 version / product info	Tuple Code
02Eh	17h									Link to next tuple is 23 bytes	Link Length
030h	04h	TPPLV1_MAJOR								PCMCIA 2.0 /JEIDA 4.1	Major Version
032h	01h	TPPLV1_MINOR								PCMCIA 2.0 /JEIDA 4.1	Minor Version
034h	53h	ASCII Manufacturer String								'S'	String 1
036h	75h									'u'	
038h	6Eh									'n'	
03Ah	44h									'D'	
03Ch	69h									'i'	
03Eh	73h									's'	
040h	6Bh									'k'	
042h	00h	End of Manufacturer String								Null terminator	
044h	53h	ASCII Product Name String								'S'	Info String 2
046h	44h									'D'	
048h	50h									'P'	
04Ah	00h	End of Product Name String								Null terminator	
04Ch	35h									'5'	Info String 3
04Eh	2Fh									'/'	
050h	33h									'3'	
052h	20h									' '	
054h	30h	SanDisk Card CIS Revision Number								'0'	
056h	2Eh									'.'	
058h	36h									'6'	
05Ah	00h	End of CIS Revision Number								Null terminator	
05Ch	FFh	End of List Marker								FFh List terminator	No Info String 4

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
05Eh	80h	CISTPL_VEND_SPECIF_80								SanDisk Parameters Tuple	Tuple Code
060h	03h	(Field Bytes 3-4 taken as 0)								Link length is 3 byte	Link to next tuple and length of info in this tuple
062h	14h	W 0	12 0	NI 0	PP 1	PDNA 0	RIA 1	RIR 0	SP 0	No Wear Level & NO Vpp W:No Wear Level 12:Vpp Not used on Write NI:-INPACK connected PP:Programmable Power PDNA:Pwr Down Not Abort--Cmd RIA:RBsy, ATBsy connected RIR:RBsy Inhibited at Reset SP:No Security Present This definition applies only to cards with Manufacturer's ID tuple 1st 3 bytes 45 00 01.	SanDisk Fields, 1 to 4 bytes limited by link length.
064h	08h	R 0	R 0	R 0	R 0	E 1	TPR 0	TAR 0	R8 0	R8:8 bit ROM present TAR:Temp Bsy on AT Reset TPR:Temp Bsy on PCMCIA -- Reset E:Erase Ahead Available R:Reserved, 0 for now This definition applies only to card with Manufacturer's ID tuple 1st 3 bytes 45 00 01.	SanDisk Fields, 1 to 4 bytes limited by link length.
066h	00h										For Specific platform use Only
068h	21h	CISTPL_FUNCID								Function ID Tuple	Tuple Code
06Ah	02h									Link length is 2 bytes	Link to next tuple
06Ch	04h	Function Type Code								Disk Function	Function Code
06Eh	01h	R 0	R 0	R 0	R 0	R 0	R 0	R 0	P 1	Attempt installation at Post P:Install at POST R:Reserved(0)	
070h	22h	CISTPL_FUNCE								Function Extension Tuple	Tuple Code
072h	02h									Link length is 2 bytes	Link to next tuple
074h	01h	Disk Function Extension Tuple Type								Extension tuple describes the Interface Protocol	Extension Tuple Type for Disk
076h	01h	Interface Type Code								PC Card-ATA Interface	Extension Info

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
078h	22h	CISTPL_FUNCE								Function Extension tuple	Tuple Code
07Ah	03h									This tuple has 3 info bytes	Link Length
07Ch	02h	Disk Function Extension Tuple Type								Basic PCMCIA-ATA Extension tuple	Extension Tuple Type for Disk
07Eh	0Ch	R 0	R 0	R 0	R 0	U 1	S 1	V 0		No Vpp, Silicon Drive with Unique Manufacturer / Serial Number combined string V=0:No Vpp Required V=1:Vpp on Modify Media V=2:Vpp on any operation V=3:Vpp continuous S:Silicon, else Rotating U:ID Drive Mfg/SN Unique	Basic ATA Option Parameters
080h	0Fh	R 0	I 0	E 0	N 0	P3 1	P2 1	P1 1	P0 1	All power down modes and power commands are not needed to minimize power. P0:Sleep Mode Supported P1:Standby Mode Supported P2:Idle Mode Supported P3:Drive Auto Power Control N:Some Config Excludes 3X7 E:Index Bit is Emulated I:Twin -IOis16 Data Reg Only	Extended ATA Option Parameters
082h	1Ah	CISTPL_CONF								Configuration Tuple	Tuple Code
084h	05h									Link Length is 5 bytes	Link to next tuple
086h	01h	RFS 00			RMS 00			RAS 01		Size of Reserved Field is 0 bytes, Size of Register Mask is 1 Byte, Size of Config Base Address is 2 bytes RFS:Bytes in Reserved Field RMS:Bytes in Reg Mask-1 RAS:Bytes in Base Addr-1	Size of fields byte (TPCC_SZ)
088h	07h	TPCC_LAST								Entry with Config Index of 07h is final entry in table	Last entry of configuration table
08Ah	00h	TPCC_RADR (lsb)								Configuration Registers are located at 200h in Reg Space.	Location of Config Registers
08Ch	02h	TPCC_RADR (msb)									
08Eh	0Fh	R 0	R 0	R 0	R 0	S 1	P 1	C 1	I 1	First 4 Configuration Registers are present I:Configuration Index C:Configuration and Status P:Pin Replacement S:Socket and Copy R:Reserved for future use	TPCC_RMSK

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
090h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
092h	0Bh									Link to next tuple is 11 bytes. Also limits size of this tuple to 13 bytes.	Link to next tuple
094h	C0h	I 1	D 1	Configuration Index 0						**Memory Mapped I/O Configuration** Configuration Index for this entry is 0. Interface Byte follows this byte. Default Configuration, so is not dependent on previous Default Configuration. D:Default Configuration I:Interface Byte Follows	TPCE_INDX
096h	C0h	W 1	R 1	P 0	B 0	Interface Type 0				Memory Only Interface(0), Bvd's and wProt not used, Ready/-Busy and Wait for memory cycles active. B:Battery Volt Detects Used P:Write Protect Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF
098h	A1h	M 1	MS 1		IR 0	IO 0	T 0	P 1		Vcc only Power; No Timing, I/O, or IRQ; 2 Byte Mem Space Length; Misc Entry Present P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present	TPCE_FS
09Ah	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage LV:Mimimum Voltage HB:Maximum Voltage SI:Static Current AI:Average Current PI:Peak Current DI:Power Down Current	Power Parameters for Vcc
09Ch	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5 Volts	Vcc Nominal Value
09Eh	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			Vcc Nominal is 4.5 Volts	Vcc Minimum Value
0A0h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			Vcc Nominal is 5.5 Volts	Vcc Maximum Value

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0A2h	75h	X 0	Mantissa Eh = 8.0				Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current
0A4h	08h	Length in 256 bytes pages (lsb)								Length of Mem Space is 2 KB	TPCE_MS Length LSB
0A6h	00h	Length in 256 bytes pages (msb)								Start at 0 on card	TPCE_MS Length MSB
0A8h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T:Twin Cards Allowed A:Audio Supported RO:Read Only Mode P:Power Down Supported R:Reserved X:More Misc Fields Bytes	TPCE_MI
0AAh	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0ACh	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
0AEh	00h	I 0	D 0	Configuration Index 0						Memory mapped I/O 3.3V configuration.	TPCE_INDX
0B0h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type	TPCE_FS
0B2h	21h	R 0	DI 0	PI 1	AI 0	SI 0	H 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	TPCE_PD
0B4h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
0B6h	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
0B8h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45mA	Max Average Current

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0BAh	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0BCh	0Dh									Link to next tuple is 13 bytes. Also limits size of this tuple to 15 bytes.	Link to next tuple
0BEh	C1h	I 1	D 1	Configuration Index 1						**I/O Mapped Contiguous 16 registers configuration** Configuration Index for this entry is 1. Interface Byte follows this byte. Default Configuration, so is not dependent on previous Default Configuration. D:Default Configuration I:Interface Byte Follows	TPCE_INDX
0C0h	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Used P:Write Protect Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF
0C2h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		Vcc Only Power Descriptors; No Timing; I/O and IRQ present; No Mem Space; Misc Entry Present P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present	TPCE_FS
0C4h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage LV:Mimimum Voltage HB:Maximum Voltage SI:Static Current AI:Average Current PI:Peak Current DI:Power Down Current	Power Parameters for Vcc
0C6h	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5Volts	Vcc Nominal Value
0C8h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			Vcc Nominal is 4.5 Volts	Vcc Minimum Value
0CAh	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			Vcc Nominal is 5.5Volts	Vcc Maximum Value

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0CCh	75h	X 0	Mantissa Eh = 8.0				Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current
0CEh	64h	R 0	S 1	E 1	IO AddeLines 4					Supports both 8 and 16 bit I/O hosts. 4 Address lines and no range so 16 registers and host must do all selection decoding. IO AddrLines:#lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO
0D0h	F0h	S 1	P 1	L 1	M 1	V 0	B 0	I 0	N 0	IRQ Sharing Logic Active in Card Control & Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Present V:Vendor Unique IRQ B:Bus Error IRQ I:IO Check IRQ N:Non-Maskable IRQ	TPCE_IR
0D2h	FFh	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 1	IRQ Levels to be routed 0 - 15 recommended.	TPCE_IR Mask Extension Byte 1
0D4h	FFh	F 1	E 1	D 1	C 1	B 1	A 1	9 1	8 1	Recommended routing to any "normal, maskable" IRQ.	TPCE_IR Mask Extension Byte 2
0D6h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T:Twin Cards Allowed A:Audio Supported RO:Read Only Mode P:Power Down Supported R:Reserved X:More Misc Fields Bytes	TPCE_MI

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0D8h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0DAh	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
0DCh	01h	I 0	D 0	Configuration Index 1						I/O mapped contiguous 16 3.3V configuration	TPCE_INDX
0DEh	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type	TPCE_FS
0E0h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	Power Parameters for Vcc
0E2h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
0E4h	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
0E6h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45 mA	Max Average Current
0E8h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0EAh	12h									Link to next tuple is 18 bytes. Also limits size of this tuple to 20 bytes.	Link to next tuple
0ECh	C2h	I 1	D 1	Configuration Index 2						**AT Fixed Disk Primary I/O Address Configuration** Configuration Index for this entry is 2. Interface Byte follows this byte. Default Configuration	TPCE_INDX
0EEh	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Used P:Write Protect Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0F0h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		Vcc Only Power Description; No Timing; I/O and IRQ present; No Mem Space; Misc Entry present P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present	TPCE_FS
0F2h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage LV:Mimimum Voltage HB:Maximum Voltage SI:Static Current AI:Average Current PI:Peak Current DI:Power Down Current	Power Parameters for Vcc
0F4h	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5Volts	Vcc Nominal Value
0F6h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			Vcc Nominal is 4.5Volts	Vcc Minimum Value
0F8h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			Vcc Nominal is 5.5Volts	Vcc Maximum Value
0FAh	75h	X 0	Mantissa Eh = 8.0				Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current
0FCh	EAh	R 1	S 1	E 1	IO AddeLines Ah = 10					Supports both 8 and 16 bit I/O hosts. 10 Address lines with range so card will respond only to indicated (1F0-1F7, 3F6-3F7) on A9 through A0 for I/O cycles. IO AddrLines:#lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0FEh	61h	LS 1		AS 2		N Ranges - 1 1				Number of Ranges is 2; Size of each address is 2 bytes; Size of each length is 1 byte. AS:Size of Addresses 0:No Address Present 1:1Byte (8 bit) Addresses 2:2Byte (16 bit) Addresses 3:4Byte (32 bit) Addresses LS:Size of length 0:No Lengths Present 1:1Byte (8 bit) Lengths 2:2Byte (16 bit) Lengths 3:4Byte (32 bit) Lengths	I/O Range Format Description
100h	F0h	1st I/O Base Address (lsb)								First I/O Range base is	
102h	01h	1st I/O Base Address (msb)								1F0h	
104h	07h	1st I/O Range Length - 1								8 bytes total ==> 1F0-1F7h	I/O Length - 1
106h	F6h	2nd I/O Base Address (lsb)								2nd I/O Range base is	
108h	03h	2nd I/O Base Address (msb)								3F6h	
10Ah	01h	2nd I/O Range Length - 1								2 bytes total ==> 3F6-3F7h	I/O Length - 1
10Ch	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14				IRQ Sharing Logic Active in Card Control & Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Present M=0 so bits 3-0 are single level, binary encoded	TPCE_IR
10Eh	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T:Twin Cards Allowed A:Audio Supported RO:Read Only Mode P:Power Down Supported R:Reserved X:More Misc Fields Bytes	TPCE_MI

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
110h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
112h	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
114h	02h	I 0	D 0	Configuration Index 2						AT Fixed Disk Primary I/O 3.3V configuration	TPCE_INDX
116h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type	TPCE_FS
118h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	Power Parameters for Vcc
11Ah	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
11Ch	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
11Eh	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45mA	Max Average Current

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
120h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
122h	12h									Link to next tuple is 18 bytes. Also limits size of this tuple to 20 bytes.	Link to next tuple
124h	C3h	I 1	D 1	Configuration Index 3						**AT Fixed Disk Secondary I/O Address Configuration** Configuration Index for this entry is 3. Interface Byte follows this byte. Default Configuration	TPCE_INDX
126h	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Used P:Write Protect Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF
128h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		Vcc Only Power Descriptors; No Timing; I/O and IRQ present; No Mem Space; Misc Entry Present. P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present	TPCE_FS
12Ah	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage LV:Mimimum Voltage HB:Maximum Voltage SI:Static Current AI:Average Current PI:Peak Current DI:Power Down Current	Power Parameters for Vcc
12Ch	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5Volts	Vcc Nominal Value
12Eh	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			Vcc Nominal is 4.5Volts	Vcc Minimum Value
130h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			Vcc Nominal is 5.5Volts	Vcc Maximum Value
132h	75h	X 0	Mantissa Eh = 1.0				Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
134h	EAh	R 1	S 1	E 1	IO AddeLines Ah = 10					Supports both 8 and 16 bit I/O hosts. 10 Address lines with range so card will respond only to indicated (170-177, 376-377) on A9 through A0 for I/O cycles. IO AddrLines:#lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO
136h	61h	LS 1		AS 2	N Ranges - 1 1					Number of Ranges is 2; Size of each address is 2 bytes; Size of each length is 1 byte. AS:Size of Addresses 0:No Address Present 1:1Byte (8 bit) Addresses 2:2Byte (16 bit) Addresses 3:4Byte (32 bit) Addresses LS:Size of length 0:No Lengths Present 1:1Byte (8 bit) Lengths 2:2Byte (16 bit) Lengths 3:4Byte (32 bit) Lengths	I/O Range Format Description
138h	70h	1st I/O Base Address (lsb)								First I/O Range base is 170h	
13Ah	01h	1st I/O Base Address (msb)									
13Ch	07h	1st I/O Range Length - 1								8 bytes total ==> 170-177h	I/O Length - 1
13Eh	76h	2nd I/O Base Address (lsb)								2nd I/O Range base is 376h	
140h	03h	2nd I/O Base Address (msb)									
142h	01h	2nd I/O Range Length - 1								2 bytes total ==> 376-377h	I/O Length - 1
144h	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14				IRQ Sharing Logic Active in Card Control & Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Present M=0 so bits 3-0 are single level, binary encoded	TPCE_IR

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
146h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T:Twin Cards Allowed A:Audio Supported RO:Read Only Mode P:Power Down Supported R:Reserved X:More Misc Fields Bytes	TPCE_MI
148h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
14Ah	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
14Ch	03h	I 0	D 0	Configuration Index 3						AT Fixed Disk Secondary I/O 3.3V configuration	TPCE_INDX
14Eh	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type	TPCE_FS
150h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	Power Parameters for Vcc
152h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
154h	1Eh	X 0	1Eh				+.30			Nominal Operation Supply Voltage Extension Byte	
156h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45mA	Max Average Current
158h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
15Ah	04h									Link to next tuple is 4 bytes.	Link to next tuple
15Ch	07h	I 0	D 0	Configuration Index 7						AT Fixed Disk Secondary I/O 3.3V configuration	TPCE_INDX
15Eh	00h	M 0	MS 0		IR 0	IO 0	T 0	P 0		P:Power info type	TPCE_FS
160h	028h									SanDisk Code	Reserved
162h	0D3h									SanDisk Code	Reserved
164h	014h	CISTPL_NO_LINK								Prevent Scan of Common Memory	Tuple Code
166h	000h	No Bytes Following								Link Length is 0 Bytes	Link to next tuple
168h	0FFh	End of Tuple Chain								End of CIS	Tuple Code

11.0 Flash ChipSet Manufacturabilty Specifications

11.1 How the Flash ChipSet Controller and TSOP are Received

The Flash ChipSet Controller and TSOP are each shipped in boxes of 360 pieces in 4 trays with 90 pieces in each tray. The FCS controller and TSOP trays conform to JEDEC standards. These trays are dry packed and vacuum sealed with a desiccant in a moisture barrier bag. The shelf life of Flash ChipSet components in a sealed bag is 12 months.

A humidity indicator card is inside the bag and an instruction label is on the outside of the bag. The instruction label includes instructions for opening the bag according to the humidity indication. If the humidity indicator reads higher that 20% relative humidity, the Flash ChipSet Controller or TSOP must be baked at 125°C for 24 hours. Figures 11-1 and 11-2 show the humidity card and instruction label. (Figures 11-3 and 11-4 show the outer and inner packaging. Figures 11-5 and 11-6 show the FCS Controller and TSOP tray specifications.)

The moisture barrier bag with trays is wrapped in plastic bubble wrap and placed inside a cardboard box. Identification labels on the outside of this box identify the Flash ChipSet Controller or TSOP and its sealing date. An outer cardboard shipping box will contain a maximum of four boxes containing Controller or TSOP trays.

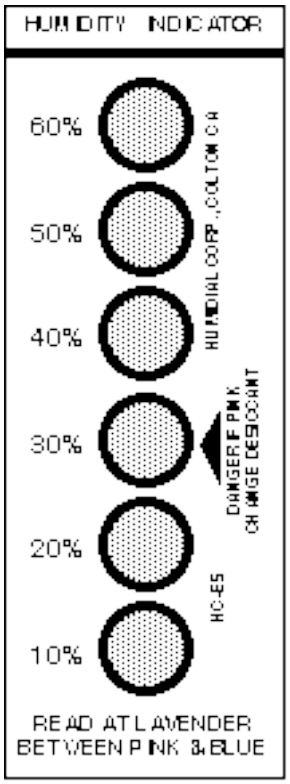


Figure 11-1 Humidity Card

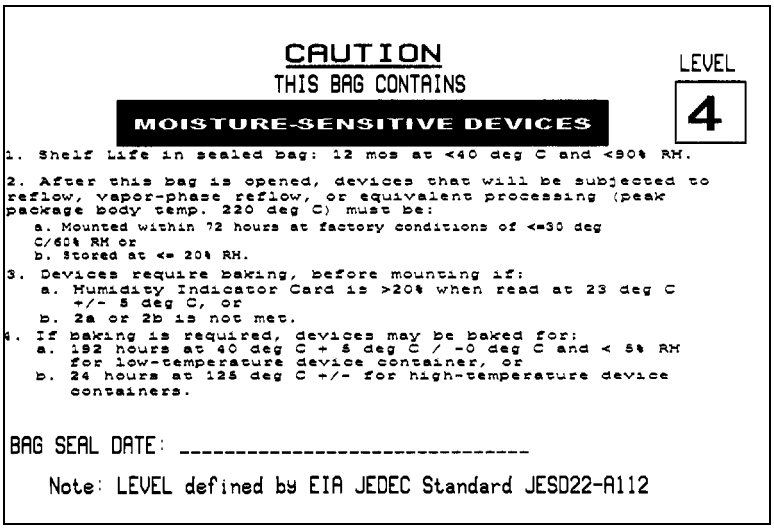
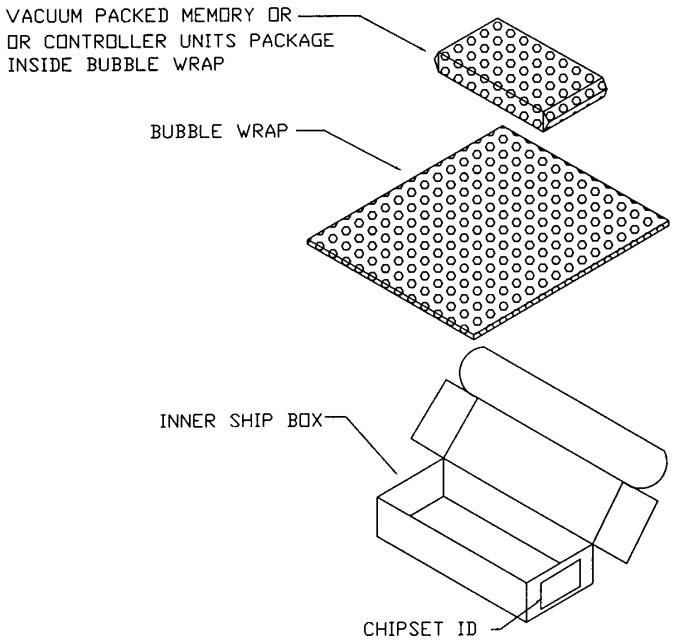


Figure 11-2 Instruction Label

NOTE: Do not open the moisture barrier bag without first reading the opening instructions. Be sure to follow the instructions for opening the bag.



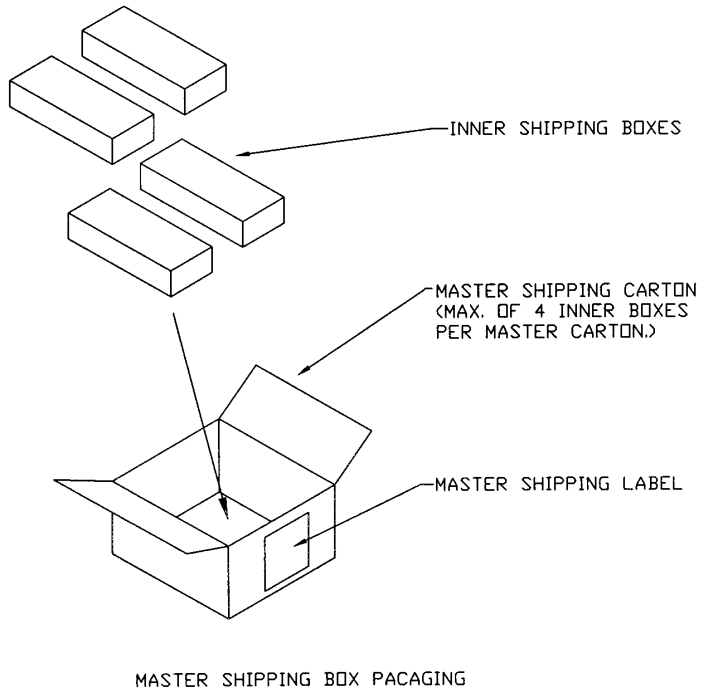


Figure 11-3 Flash ChipSet Outer Packaging

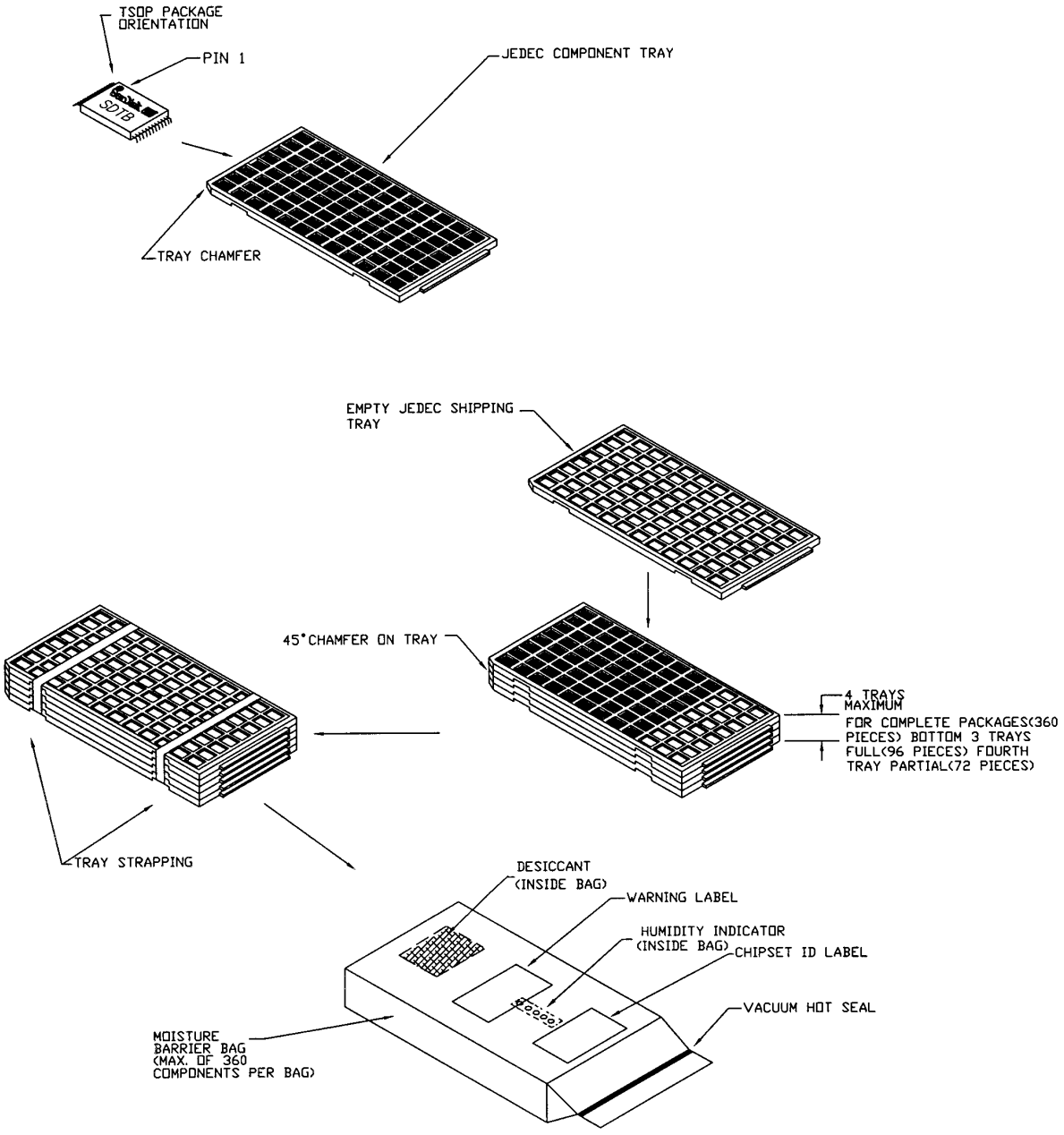


Figure 11-4 Flash ChipSet Inner Packaging

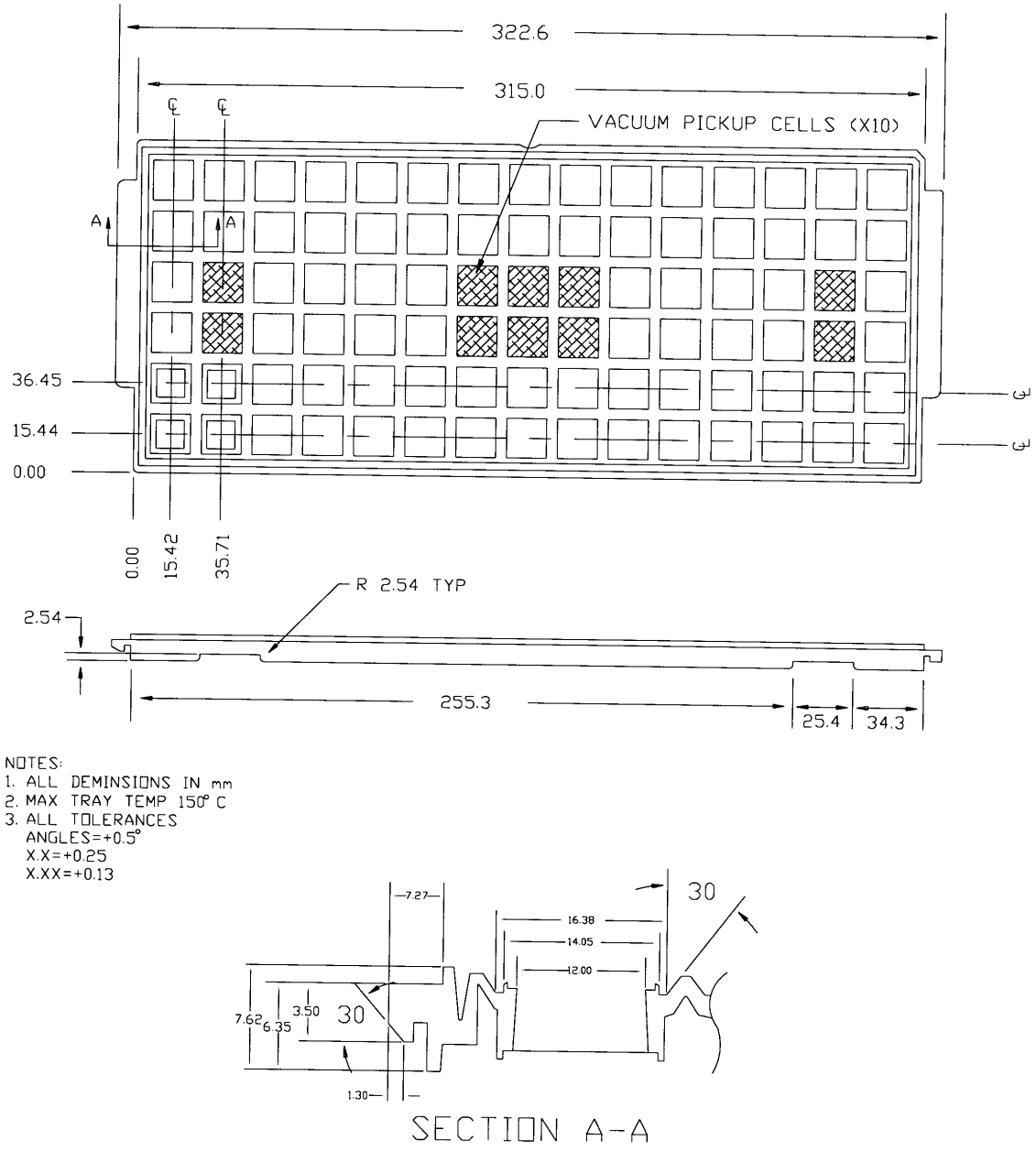


Figure 11-5 Flash ChipSet Controller Tray Specification

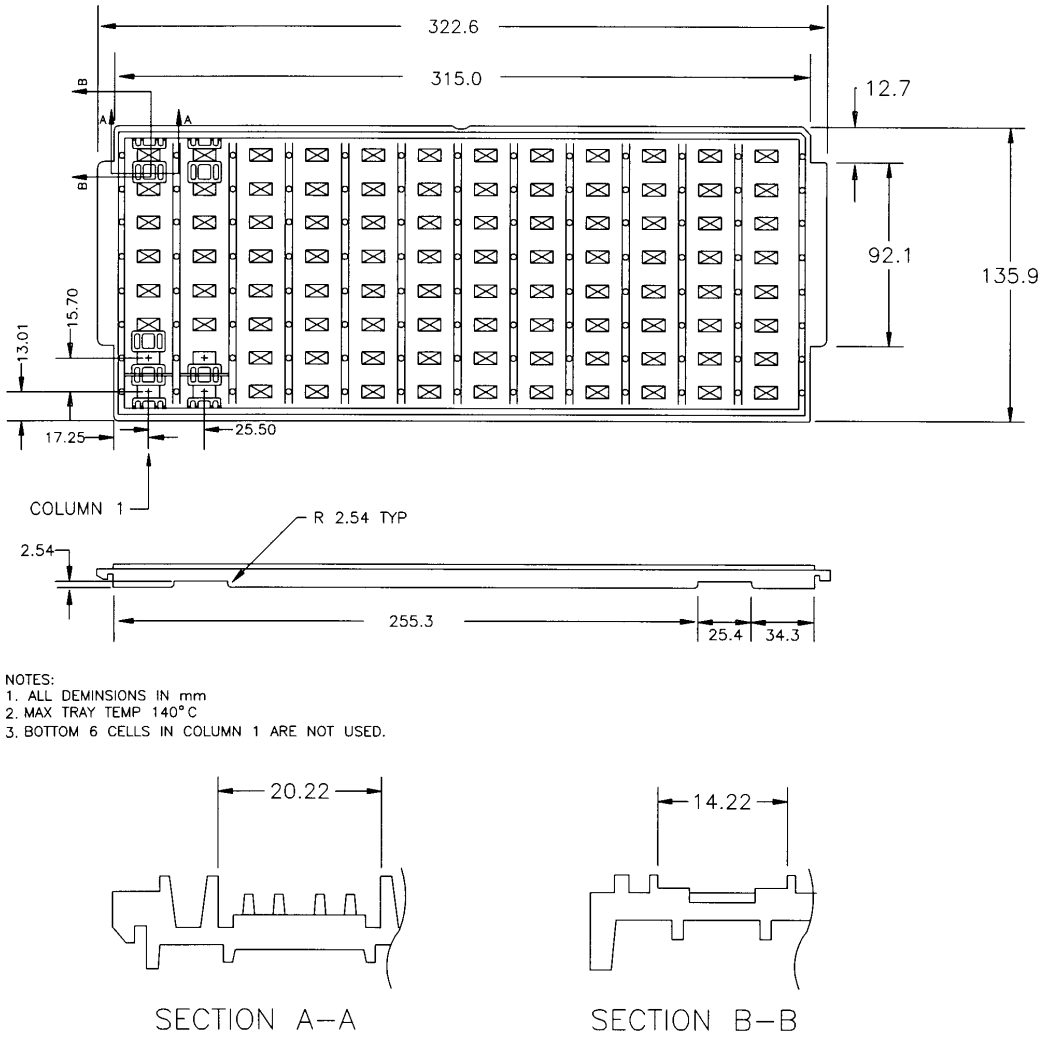


Figure 11-6 Flash ChipSet TSOP Tray Specification

11.2 Flash ChipSet Components on Tape Reel

Flash ChipSet orders of less than 90 units are shipped on tape reel. Flash ChipSet components shipped on tape reel can be ordered in increments of five units.

Note: Flash ChipSet components shipped on tape reel do not go through a bake cycle and should be mounted on the PCB by hand rather than mounted with a “pick and place” vacuum picker. See the following section of this manual for handling specifications for the Flash ChipSet.

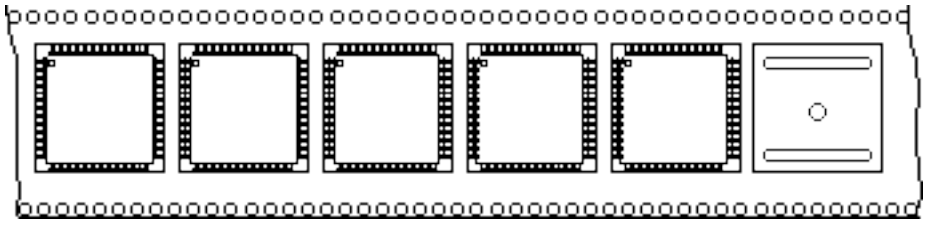


Figure 11-7 Flash ChipSet Controller on Tape Reel

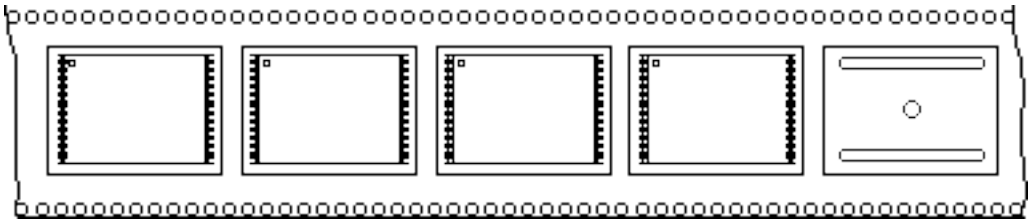


Figure 11-8 Flash ChipSet TSOP on Tape Reel

11.3 Handling Specifications for the Flash ChipSet Controller and TSOP

The Flash ChipSet Controller and TSOP can be installed on a printed circuit board using the "pick and place" method with a vacuum picker.

11.3.1 Soldering the FCS Controller and TSOP to the Printed Circuit Board

SanDisk recommends that the "no-clean" process be used to solder the FCS Controller and TSOP to the printed circuit board. Use the following materials for the "no clean" process:

- Solder paste: Qualitek 670I or equivalent
- Flux: Qualitek 360, Multicore X32/FQ1 or equivalent
- Solderwire: Qualitek Delta NC-600, Multicore X32C or equivalent

The solder joint temperature should not exceed 220°C. The reflow duration is about 50 seconds. The temperature setting on the soldering iron should be 500° to 750°F. The soldering time is approximately 45 seconds.

11.4 Sample Bill of Materials (BOM) for Appendix 3 Schematic

Description	Quantity	Location	Vendor	Part Number
SanDisk Controller 100 PIN TQFP	1	U1	SanDisk	SDCD-3
RES 1.24K 1/10W 0.5% 0805	1	R1	KOA	RN73E2A1241D
CAP .1µf 10% X7R 0805	7	C1-3, 5-8	AVX	08051C104KATMA
CAP .01µF 10% X7R 0805	1	C4, C16	AVX	08051C103KATMA
CAP .22µf 10% X7R 1206	1	C9	AVX	12061C224KATMA
CAP TANT 1.0µF 10% 35V 3528	1	C10	SPRAGUE	592D105X935B2T
CAP 33PF 5% COG 0805	1	C11	AVX	08051A330JATMA
CAP 47PF 5% COG 0805	1	C12	AVX	08051A470JATMA
P-FET SMT SOT-143	1	Q1	MICREL	MIC94030

Note: Equivalent parts produced by other vendors and equivalent package sizes are acceptable. However, SanDisk strongly recommends using the above components when designing in the Flash ChipSet. Using other types of circuits could cause design problems. These components are the same components used in the packaged SanDisk CompactFlash Memory Card.

MIC94030 and MIC94031

P-Channel TinyFET™ MOSFET

Preliminary Information–Production Q1 '94

General Description

The MIC94030 and MIC94031 are 4-terminal silicon gate P-channel MOSFETs that each provide low R_{ON} in a very small package.

Designed for high-side switch applications where space is critical, the MIC94030/1 exhibits an $R_{DS(ON)}$ of typically 0.75Ω at 4.5V gate-to- source voltage. The MIC94030/1 also operates with only 2.7V gate-to- source voltage.

The MIC94030 is the basic 4-lead P-channel MOSFET. The MIC94031 is a variation that includes an internal gate pull-up resistor which can reduce the system parts count in many applications.

The 4-terminal SOT-143 package permits a substrate connection separate from the source connection. This 4-terminal configuration improves the θ_{JA} (improved heat dissipation) and makes analog switch applications practical.

The small size, low threshold, and low $R_{DS(ON)}$ make the MIC94030/1 the ideal choice for PCMCIA card sleep mode or distributed power management applications.

Features

- 0.75Ω typical ON resistance at 4.5V gate to source voltage
- 0.45Ω typical ON resistance at 10V gate-to-source voltage
- Operates with 2.7V gate to source voltage
- Separate substrate connection for added control
- Industry's smallest surface mount package
- V_{GS} and V_{BDSS} to 13.5V

Applications

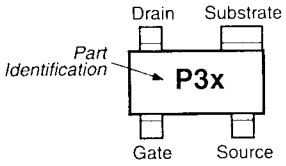
- PCMCIA Card Power Management
- Battery Powered Computers & Peripherals
- Portable Communications Equipment
- Hand Held Bar Code Scanners
- Distributed Power Management

Ordering Information

Part Number	Temperature Range*	Package
MIC94030BM4	–55°C to +150°C	SOT-143
MIC94031BM4	–55°C to +150°C	SOT-143

* Operating Junction Temperature

Pin Configuration

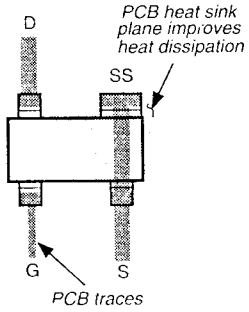


Part Number	Identification
MIC94030BM4	P30
MIC94031BM4	P31

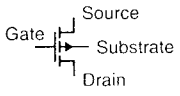
SOT-143 Package (M4)

SOT-143 Package Actual Size

Typical PCB Layout

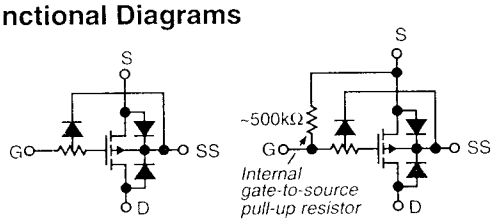


Schematic Symbol



Schematic Symbol

Functional Diagrams



MIC94030 **MIC94031**

Appendix 1 P-Channel TinyFET™ MOSFET Specification

Typical Applications

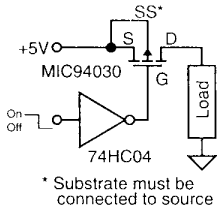


Figure 1. Power Switch Application

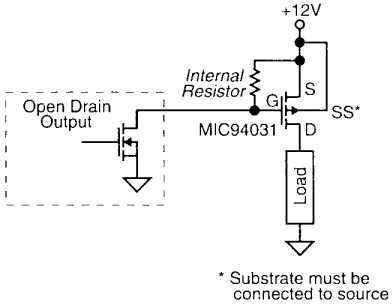
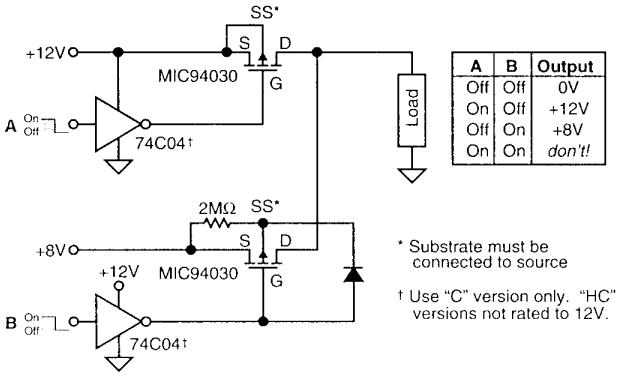


Figure 2. Power Control Application



A	B	Output
Off	Off	0V
On	Off	+12V
Off	On	+8V
On	On	*don't!*

Figure 3. Analog Switch Application

Appendix 1 P-Channel TinyFET™ MOSFET Specification (con't)

Absolute Maximum Ratings

Voltage and current values are negative. Signs not shown for clarity.

Drain to Source Voltage 16V
Gate to Source Voltage 16V
Continuous Drain Current
T_A = 25°C 1A
T_A = 100°C 0.5A
Operating Junction Temperature ..... –55°C to +150°
Storage Temperature ..... –55°C to +150°C

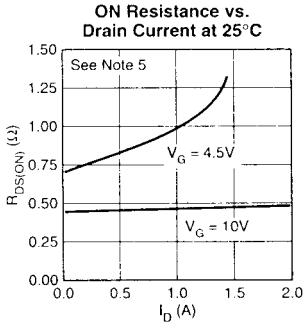
Total Power Dissipation
T_A = 25°C 568mW
T_A = 100°C 227mW
Thermal Resistance
θ_{JA} ..... 220°C/W
θ_{JC} ..... 130°C/W
Lead Temperature
1/16" from case, 10s ..... +300°C

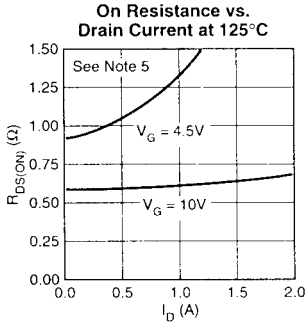
Electrical Characteristics *Voltage and current values are negative. Signs not shown for clarity.*

Symbol	Parameter	Condition (Note 1)	Min	Typ	Max	Units
V_{BDSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	13.5			V
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.6	1.0	1.4	V
I_{GSS}	Gate-Body Leakage	V_{DS} = 0V, V_{GS} = 12V, **Note 2**, **Note 3**			1	µA
R_{GS}	Gate-Source Resistor	V_{DS} = 0V, V_{GS} = 12V, **Note 2**, **Note 4**		500	1000	kΩ
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12V		100		pF
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 12V, V_{GS} = 0V			25	µA
		V_{DS} = 12V, V_{GS} = 0V, T_J = 125°C		0.010	250	µA
$I_{D(ON)}$	On-State Drain Current	V_{DS} = 10V, V_{GS} = 10V, **Note 5**		6.3		A
$R_{DS(ON)}$	Drain-Source ON-State Resist.	V_{GS} = 10V, I_D = 100mA V_{GS} = 4.5V, I_D = 100mA V_{GS} = 2.7V, I_D = 100mA		0.45 0.75 1.20	 1.00 	Ω Ω Ω
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 200mA, **Note 5**		480		mS

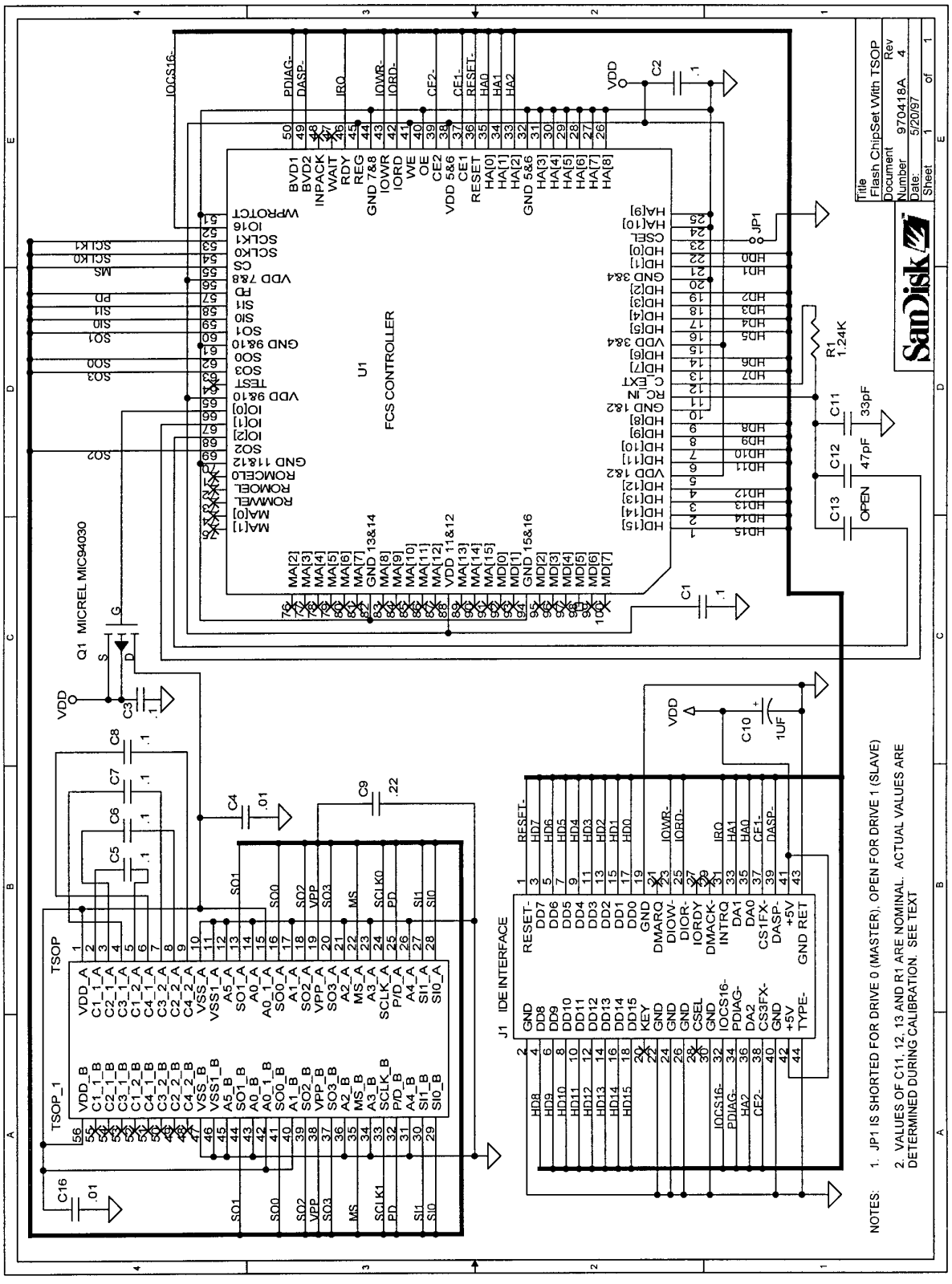
Note 1 T_A = 25°C unless noted. Substrate connected to source for all conditions
Note 2 ESD gate protection diode conducts during positive gate to source voltage excursions.
Note 3 MIC94030 only
Note 4 MIC94031 only
Note 5 Pulse Test: Pulse Width ≤ 80µsec, Duty Cycle ≤ 0.5%

Typical Characteristics

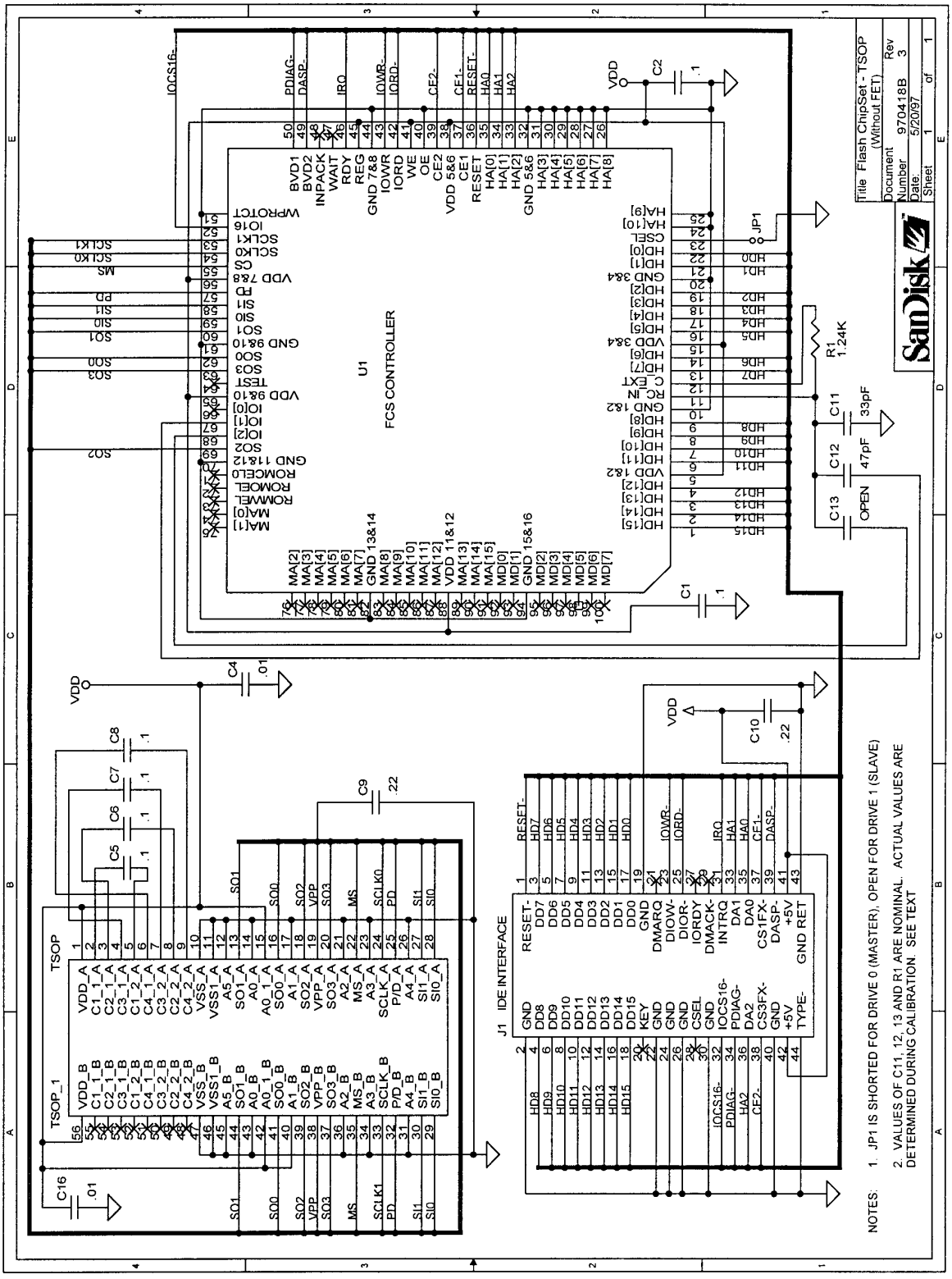




Appendix 1 P-Channel TinyFET™ MOSFET Specification (con't)



Appendix 2 Schematic Flash ChipSet with FET



Appendix 3 Schematic Flash ChipSet without FET

Ordering Information and Technical Support

Ordering Information

To order SanDisk products directly from SanDisk, call **408-542-0595.**

SanDisk Flash ChipSet Series

Flash ChipSet—Standard Product
- **Model SDFCSTB-32-366 (4 MB TSOP and Controller)**
- **Model SDFCSTB-64-366 (8 MB TSOP and Controller)**
- **Model SDFCSTB-128-366 (16 MB TSOP and Controller)**

Flash ChipSet—Industrial Product
- **Model SDFCSTBI-32-366 (4 MB TSOP and Controller)**
- **Model SDFCSTBI-64-366 (8 MB TSOP and Controller)**
- **Model SDFCSTBI-128-366 (16 MB TSOP and Controller)**

Flash ChipSet on Tape Reel—Standard Product
- **Model SDFCSTB-32-366R (4 MB TSOP and Controller on Tape Reel)**
- **Model SDFCSTB-64-366R (8 MB TSOP and Controller on Tape Reel)**
- **Model SDFCSTB-128-366R (16 MB TSOP and Controller on Tape Reel)**

Flash ChipSet on Tape Reel—Industrial Product
- **Model SDFCSTBI-32-366R (4 MB TSOP and Controller on Tape Reel)**
- **Model SDFCSTBI-64-366R (8 MB TSOP and Controller on Tape Reel)**
- **Model SDFCSTBI-128-366R (16 MB TSOP and Controller on Tape Reel)**

Flash ChipSet Components—Standard Product
- **Model SDCD-3 (Controller)**
- **Model SDTB-32-366 (4 MB TSOP)**
- **Model SDTB-64-366 (8 MB TSOP)**
- **Model SDTB-128-366 (16 MB TSOP)**

Flash ChipSet Components —Industrial Product
- **Model SDCDI-3 (Controller)**
- **Model SDTBI-32-366 (4 MB TSOP)**
- **Model SDTBI-64-366 (8 MB TSOP)**
- **Model SDTBI-128-366 (16 MB TSOP)**

Flash ChipSet Components on Tape Reel—Standard Product
- **Model SDCD-3R (Controller on Tape Reel)**
- **Model SDTB-32-366R (4 MB TSOP on Tape Reel)**
- **Model SDTB-64-366R (8 MB TSOP on Tape Reel)**
- **Model SDTB-128-366R (16 MB TSOP on Tape Reel)**

Flash ChipSet Components on Tape Reel —Industrial Product
- **Model SDCDI-3R (Controller on Tape Reel)**
- **Model SDTBI-32-366R (4 MB TSOP on Tape Reel)**
- **Model SDTBI-64-366R (8 MB TSOP on Tape Reel)**
- **Model SDTBI-128-366R (16 MB TSOP on Tape Reel)**

SanDisk Flash ChipSet Evaluation Kit

The Flash ChipSet Evaluation Kit (Model SDFCSEV-03) permits designers to quickly and easily evaluate the Flash ChipSet.

Hardware

- Evaluation adapter board
- 4 MB Flash ChipSet (SDFCSTB-32) installed in test adapter
- Card extender
- AB7 adapter board

Software

- FlashDisk Driver and Utilities diskette
- Diskette with ORCAD Schematics Capture Library file

The Flash ChipSet Evaluation Kit (Model SDFCSEV-03) includes the following items:

Documentation

- Read Me First flyer
- Flash ChipSet Evaluation Kit User's Guide
- Flash ChipSet Product Manual
- Application Note: Pre-Erase Command
- Application Note: How to Design the Flash ChipSet into User Applications

Model SDFCSEV-03

To order, or for more information call:
408-542-0595

Technical Support Services

Direct SanDisk Technical Support

Call SanDisk Applications Engineering at 408-542-0405 for technical support.

SanDisk Worldwide Web Site

Internet users can obtain technical support and product information along with SanDisk news and much more from the SanDisk Worldwide Web Site, 24 hours a day, seven days a week. The SanDisk Worldwide Web Site is frequently updated. Visit this site often to obtain the most up-to-date information on SanDisk products and applications. The SanDisk Web Site URL is http://www.sandisk.com.

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FAX 408-542-0503
http://www.sandisk.com

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FAX 949-442-8371

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Yokohama 222-0033, Japan
81-45-474-0181
FAX 81-45-474-0371

Asia/Pacific Rim

89 Queensway, Lippo Center
Tower II, Suite 2207-9
Admiralty, Hong Kong
852-2712-0501
FAX 852-2712-9385

To order SanDisk products directly from SanDisk, call 408-542-0595.

Limited Warranty

I. WARRANTY STATEMENT

SanDisk warrants its products to be free of any defects in materials or workmanship that would prevent them from functioning properly for one year from the date of purchase. This express warranty is extended by SanDisk Corporation.

II. GENERAL PROVISIONS

This warranty sets forth the full extent of SanDisk's responsibilities regarding the SanDisk FlashDisk. In satisfaction of its obligations hereunder, SanDisk, at its sole option, will either repair, replace or refund the purchase price of the product.

NOTWITHSTANDING ANYTHING ELSE IN THIS LIMITED WARRANTY OR OTHERWISE, THE EXPRESS WARRANTIES AND OBLIGATIONS OF SELLER AS SET FORTH IN THIS LIMITED WARRANTY, ARE IN LIEU OF, AND BUYER EXPRESSLY WAIVES ALL OTHER OBLIGATIONS, GUARANTIES AND WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR INFRINGEMENT, TOGETHER WITH ANY LIABILITY OF SELLER UNDER ANY CONTRACT, NEGLIGENCE, STRICT LIABILITY OR OTHER LEGAL OR EQUITABLE THEORY FOR LOSS OF USE, REVENUE, OR PROFIT OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION PHYSICAL INJURY OR DEATH, PROPERTY DAMAGE, LOST DATA, OR COSTS OF PROCUREMENT OF SUBSTITUTE GOODS, TECHNOLOGY OR SERVICES. IN NO EVENT SHALL THE SELLER BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, ARISING OUT OF THE USE OR INABILITY TO USE SUCH PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

SanDisk's products are not warranted to operate without failure. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or back-up features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within one year of purchase, SanDisk will have the option of repairing or replacing the defective product, if the following conditions are met:

A. A warranty registration card for each defective product was submitted and is on file at SanDisk. If not, a warranty registration card must accompany each returned defective product. This card is included in each product's original retail package.

B. The defective product is returned to SanDisk for failure analysis as soon as possible after the failure occurs.

C. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

D. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding storage or maximum ratings or operating conditions.

All failing products returned to SanDisk under the provisions of this limited warranty shall be tested to the product's functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs.

SanDisk reserves the right to repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

SanDisk may, at its discretion, ship repaired or rebuilt products identified in the same way as new products, provided such cards meet or exceed the same published specifications as new products. Concurrently, SanDisk also reserves the right to market any products, whether new, repaired, or rebuilt, under different specifications and product designations if such products do not meet the original product's specifications.

IV. RECEIVING WARRANTY SERVICE

According to SanDisk's warranty procedure, defective product should be returned only with prior authorization from SanDisk Corporation. Please contact SanDisk's Customer Service department at 408-542-0595 with the following information: product model number and description, serial numbers, nature of defect, conditions of use, proof of purchase and purchase date. If approved, SanDisk will issue a Return Material Authorization or Product Repair Authorization number. Ship the defective product to:

SanDisk Corporation
Attn: RMA Returns
(Reference RMA or PRA #)
140 Caspian Court
Sunnyvale, CA 94089

V. STATE LAW RIGHTS

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES, OR LIMITATION ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY TO YOU. This warranty gives you specific rights and you may also have other rights that vary from state to state.

VI. OUT OF WARRANTY REPAIRS

Please contact SanDisk Customer Service at 408-542-0595 for the current out of warranty and repair price list.