University of Sargodha

BS 2nd Semester/Term Exam 2021

Subject: Information Technology **Paper: Digital Logic and Design (ITSC-102)**

Time Allowed: 02:30 Hours **Maximum Marks: 60**

Note: Objective part is compulsory. Attempt any three questions from subjective part.

Objective Part (Compulsory)

Q.1. Write short answers of the following in 2-3 lines each on your answer sheet. (2*12)

i. What are literals?
ii. Write dual of $0 \cdot 1 = 1 \cdot 0 = 0$
iii. Define null element theorem
iv. What are decoders?
v. What are priority circuits?
vi. What are arithmetic circuits?
vii. What is a propagation delay?
viii. What is minimum number of bits that can be added using a full adder?
ix. What are synchronous sequential circuits?
x. A flip-flop copies input to output on which edge of the clock?
xi. A divide-by-N counter has how many outputs?
xii. What is a synchronizer?

Subjective Part (3*12)

Q.2. Simplify the following Boolean equations using Boolean theorems. Check for correctness using a truth table or K-map.

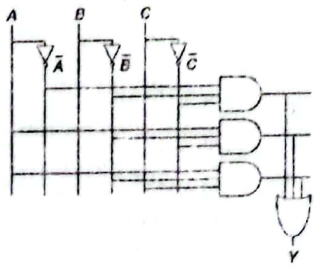
$$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}\,\overline{C} + A\overline{B}C\overline{D} + ABD + \overline{A}\,\overline{B}C\overline{D} + B\overline{C}D + \overline{A}$$

Q.3. Draw a 4:1 multiplexer with minimum number of gates.

Q.4. Following table shows the truth table for a Boolean function Y. Using De Morgan's Theorem, derive the product-of-sums canonical form of Y from the sum-of-products form of complement of Y.

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Q.5. Given the following logic circuit, draw an equivalent logic circuit with max-terms.



Q.6. Find the propagation delay and contamination delay of the circuit shown in the following circuit. According to his data book, each gate has a propagation delay of 80 picoseconds (ps) and a contamination delay of 50 ps.