University of Sargodha

BS 2nd Term Exam 2016

Subject: I.T **Paper: Digital Logic Design (CMP-2210)**

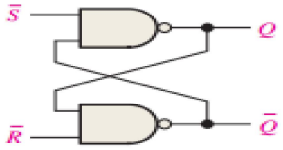
Time Allowed: 2:30 Hours **Maximum Marks: 80**

Objective Part Compulsory

Q.No.1: Attempt all parts and each require answer 2 – 3 lines (16*2=32)

1. What is S-R Latch? Draw Logic diagram using NAND Gates.

An S-R Latch is implemented by connecting two NAND or two NOR gates together. In S-R Latch there are two inputs called S (SET) and R (RESET) inputs and there are two outputs Q and its complement. The logic diagram using NAND gate, also called active LOW input S-R Latch, as follows:



2. What is ROM also draw logic circuit for ROM?

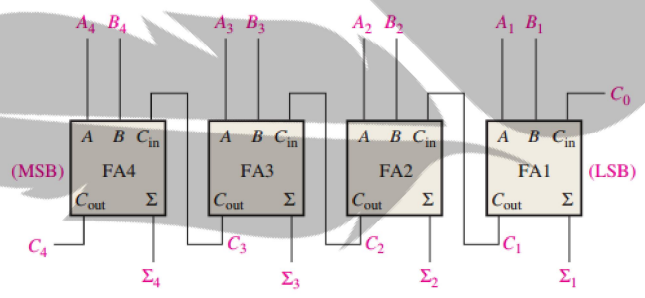
A ROM is a combinational component for storing data. The data might be a truth table or the data might be the control words for a micro programmed CPU.

3. What is difference between Combinational & Sequential circuit?

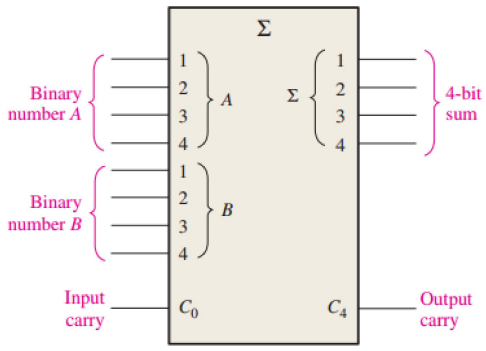
Combinational logic (sometimes also referred to as time-independent logic) is a type of digital logic which is implemented by Boolean circuits, where the output is a pure function of the present input only. Sequential logic is a type of logic circuit whose output depends not only on the present value of its input signals but on the sequence of past inputs.

4. What is 4-bit binary parallel Adder?

A basic 4-bit parallel adder is implemented with four full-adder stages. 4-bit binary full adder with two. 4-bit data inputs (A0 to A3, B0 to B3), a carry input (C_{IN}), four sum outputs (S0 to S3), and. a carry output (C_{OUT}). The outputs give the sum of the two 4-bit.



(a) Block diagram



(b) Logic symbol

5. What is carry propagation time?

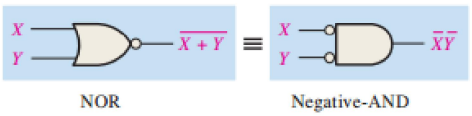
Carry propagation delay or time is the time required for a digital signal to travel from the input(s) of a logic gate to the output. It is measured in microseconds (µs), nanoseconds (ns), or picoseconds (ps). The propagation delay for an integrated circuit (IC) logic gate may differ for each of the inputs.

6. Express -121 as an 8-bit number in sign magnitude, 2's complement form.

8-bit sign magnitude of -121 is 01111001, 1's complement is 10000110 and 2's complement is 10000111.

7. State DE Morgan's Law to verify that negative-AND gate is equivalent to NOR gate.

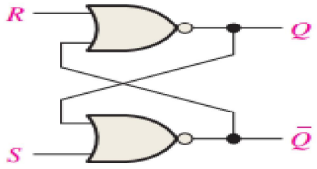
According to De Morgan's Law $\overline{X + Y} = \overline{X}\,\overline{Y}$:



Inputs		Output	
X	Y	$\overline{X+Y}$	$\overline{X}\,\overline{Y}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

9. Draw Diagram of S-R Latch using NOR gates.

S-R Latch using NOR Gates is also called an active HIGH input S-R Latch. It logic diagram is as follows:



10. Explain how an Exclusive-NOR gate is used to compare binary bits.

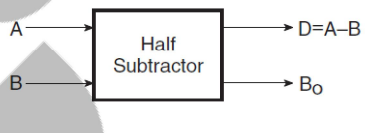
11. Convert $(F16)_{16}$ into octal number.

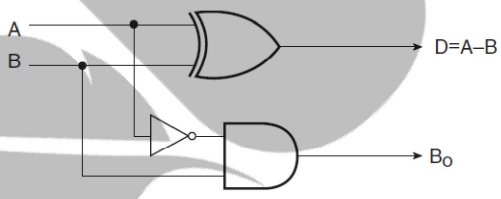
The conversion of hexadecimal number $(F16)_{16}$ to octal number is $(7426)_8$

12. What is Half-subtractor? Draw its logic diagram.

Half-subtractor is used to subtract one binary digit from another to give DIFFERENCE output and a BORROW output. The truth table of a half-subtractor is shown in figure. The Boolean expressions for half-subtractor are,
D = A'B+AB' and B_o= A'B.

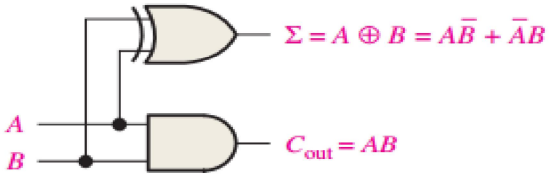
A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0





13. Draw the logic diagram of D-Flip flops using only NAND gates.

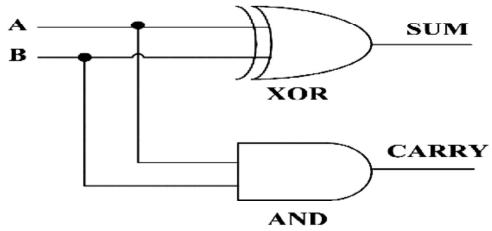
Logic diagram if D flip flop using NAND gate only.



14. Determine the decimal value of signed binary number expressed in 1's complement: 11101100

15. Draw Logic diagram for Half Adder.

Logic Diagram of Half Adder is as follows:



16. What are comparators?

A comparator is a circuit that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals and one binary digital output.