29394

University of Sargodha

BS 2nd Semester/Term Examination 2020

Subject: I.T

Paper: Digital Logic Design (ITCS-102)

Time Allowed: 2:30 Hours

(New Course)

Maximum Marks; 80

Note: Objective part is compulsory. Attempt any three questions from subjective part.

Objective Part

(Compulsory)

Q.1. Write short answers of the following in 2-3 lines each on your answer sheet.

(2*16)

- i. Express + 19 and 19 in sign-magnitude, I's complement, and 2's complement.
- ii. Add the signed numbers: a 1000100, 00011011, 00001110, and 00010010.
- iii. Perform each of the following subtractions of the signed numbers
 - a) 00001000 00000011
- b) 00001100 11110111
- iv. Convert the following binary numbers to hexadecimal
 - a) 1001010010101111
- b) 11111100001101001
- v. How does an exclusive-OR gate differ from an OR gate in its logical operation?
- vi. Apply De Morgan's theorems to each of the following expressions

$$\frac{1}{(A + B + C)D}$$
 (b) $\overline{AB + CD + EF}$

- vii. Simplify the following Boolean expression: $[A\overline{B}(C + BD) + \overline{AB}]C$
- viii. Convert the following Boolean expression into standard SOP form $A\overline{B}C + \overline{A} \overline{B} + AB\overline{C}D$
- ix. Develop a truth table for the standard SOP expression $\overline{A} \, \overline{B} \, C + A \overline{B} \, \overline{C} + A B \, C$
- x. Map the following standard SOP expression on a Karnaugh map: $\overline{A} \, \overline{B} \, C + \overline{A} \, B \, \overline{C} + A \, B \, \overline{C} + A \, B \, \overline{C}$
- xi. Group the 1s in the following Karnaugh maps.

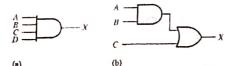
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- xii. Define Don't Care Conditions
- xiii. Identify the law of Boolean algebra upon which each of the following equalities is based

(a)
$$A\overline{B} + CD + A\overline{C}D + B = B + A\overline{B} + A\overline{C}D + CD$$

(b)
$$AB\overline{C}D + \overline{A}\overline{B}\overline{C} = D\overline{C}BA + \overline{C}BA$$

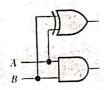
xiv. Write the Boolean expression for each of the logic circuits.



Design a logic circuit to implement the operation specified in the following truth table. XV.

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0	0	0	0	
0	0	1	0	h = 2
U	. 1	0	0	4 Ty 4 Land
0	1	- Constitution	1	ABC
1	0	0	0	
1	0	1	1	ABC ABC
1	1	0	1	ABC
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What is the functionality of the following Logic Diagram? xvi.



Subjective part (3*16)

- Draw Full Adder Logic diagram and its truth table. Q.2.
- Draw seven segment logic diagram and its truth table Q.3.
- What is decoder? Draw truth table for four bit decoder Q.4.
- Simplify the following Boolean functions, using Karnaugh maps Q.5.
 - (a) $F(x, y, z) = \sum (2, 3, 6, 7)$ (b) $F(A, B, C, D) = \sum (4, 6, 7, 15)$
- Obtain the simplified Boolean expressions for output F and G in terms of the input variables in the Q.6. circuit given below.

