

University of Sargodha

BS 2nd Term Examination 2022

Subject: CS/I.T

Paper: Digital Logic Design (CMP-2210/ITSC-102)

Maximum Marks: 60

Time Allowed: 02:30 Hours

Note: Objective part is compulsory. Attempt any three questions from subjective part.

Objective Part (Compulsory)

- Q.1. Write short answers of the following in 2-3 lines each on your answer sheet. (2*12)
- i. What is a Half Adder?
 - ii. If $A=1$, $B=0$ and $C=1$ and A , B , C represent the input of three input NAND gate, what will be the output?
 - iii. What is the difference between Decoder and Encoder?
 - iv. Draw SR latch using NOR gate.
 - v. Find the 8 bit 2's complement binary equivalent of -91.
 - vi. Prove that exclusive-OR is the compliment of exclusive-NOR.
 - vii. Differentiate between Combinational and Sequential circuit.
 - viii. Explain the Boolean Rule $A+A = A$ and $A+A' = 1$.
 - ix. State De Morgan's Law to verify that negative OR gate is equivalent to NAND gate.
 - x. Describe the basic concept of multiplexer.
 - xi. Define comparators.
 - xii. What is function of basic shift register?

Subjective Part (3*12)

- Q.2. Draw the circuit diagram of half adder and full adder. Draw truth table of half adder. Also write Boolean expression of half adder only.
- Q.3. ▲ Draw a 4-bit BCD to 7-segment decoder. Make the truth table for "c" and simplify expression? Design a BCD to 7-segment decoder? ✓
- Q.4. Simplify the function with following Karnaugh Map. Find both SOP and POS expression.
 $F(A,B,C,D) = (A'+B'+D')(A+B'+C')(A'+B+D')(B+C'+D')$
- Q.5. Draw the truth table and logic diagram to explain the basic operation of Edge triggered JK FLIP-FLOP?
- Q.6. a) Simplify to 3 number of literals $[(CD') + A]' + A + CD + AB$
 b) Implement the Boolean function using NAND gates.
 $F = B'D' + A'C'D + AB'C'D + A'BC'D'$

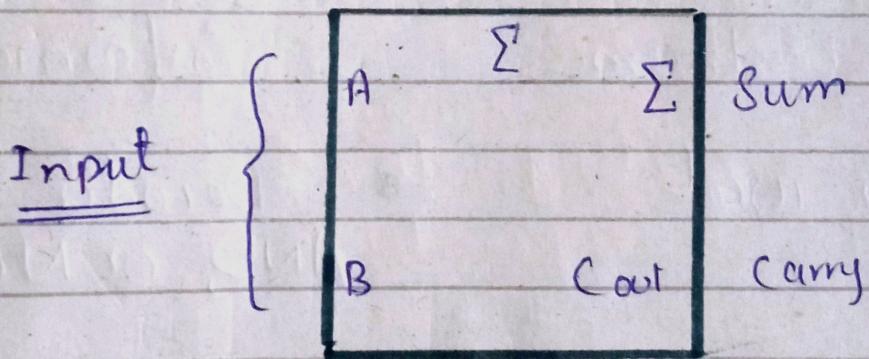
Short Question

— (i) —

A half adder adds two number / bits and produce a sum and a carry output.

$$\begin{aligned}0 + 0 &= 0 \\0 + 1 &= 1 \\1 + 0 &= 1 \\1 + 1 &= 10\end{aligned}$$

Symbol:-



— (ii) —

If three inputs $A = 1, B = 0, C = 1$
Because it multiplication or
reciprocal of AND gate

| A | B | C | Output |
|---|---|---|--------|
| 1 | 0 | 1 | 1 |

So output is '1'

— (iii) —

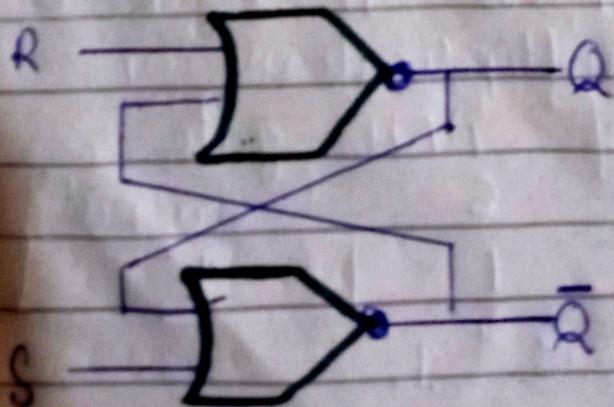
Encoder

- There are 2^n input lines in the encoder.
- There are n output lines in encoder.
- It is combinational circuit that convert informational signal code to digital bitstream.
- Encoder uses OR gate.

Decoder

- There are n input lines in the decoder.
- There are 2^n output lines in decoder.
- It is combinational circuit that convert coded bits to original information.
- Decoder uses AND, or NOT gate.

— (iv) —
S-R latch using NOR gate:-



— (v) —

Find 8 bits 2's complement binary equivalent -91.

→ Binary representation of positive 91 is

64 32 16 8 4 2 1

1 0 1 1 0 1 1

Now find 2's complement

0 1 0 0 1 0 0 - 1's

and 1 added to 1's complement

1 + 0 1 0 0 1 0 0

= 0 1 0 0 1 0 1

— (vi) —

The XOR operation defined:

$A \oplus B = 1$ if A different from B

$A \oplus B = 0$ if $A = B$

The XNOR operation

$A \odot B = 0$ if A different from B

$A \odot B = 1$ if $A = B$

Case 1:- $A=0 \quad B=0$
 XOR- $A \oplus B = 0 \oplus 0 = 0$
 $0 \oplus 0 = 1$

Case 2:- $A=0 \quad B=1$
 $0 \oplus 1 = 1$
 $0 \oplus 1 = 0$

Case 3:- $A=1 \quad B=0$
 $1 \oplus 0 = 1$
 $1 \oplus 0 = 0$

Case 4:- $A=1 \quad B=1$
 $1 \oplus 1 = 0$
 $1 \oplus 1 = 1$

— (vii) —

Combinational
circuit

Sequential
circuit.

- It gives output depending upon present input
- It gives output depending upon present input and previous output
- If it is not time dependent
- It uses clock-pulse or

time dependent.

- Its elementary building blocks

AND, OR, NOT,
NAND, NOR
gate

- Its elementary building blocks

Flip - Flops

- It is easy to build

- It is complex to build.

— (viii) —

Explain Boolean Rule

$A + A$ and $A + A'$

$A + A$

If it is logical OR operation.

$$\rightarrow A + A = A$$

$$\because 0 + 0 = 0$$

$$1 + 1 = 1$$

$$\rightarrow A + A' = 1$$

$$\because 0 + 1 = 1$$

$$1 + 0 = 1$$

— (ix) —

There are two demorgan law.

①

$$\overline{A+B} = \bar{A} \cdot \bar{B}$$

②

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

Statement That demorgan verify That negation OR=NAND

- OR = $A+B$
negation = $\overline{A+B}$

- NAND = $\bar{A} \cdot \bar{B}$

So according to ~~2nd~~^{1st} rule
of demorgan law

$$\overline{A+B} = \bar{A} \cdot \bar{B}$$

negating OR equivalent to NAND gate

— (x) —

Multiplexer:

Multiplexer is a combinational digital circuit that takes multiple data input and provides single output.

It has 2^n input lines

One output line

It is also known as data selector.

Its abbreviation is MUX

8:1 MUX

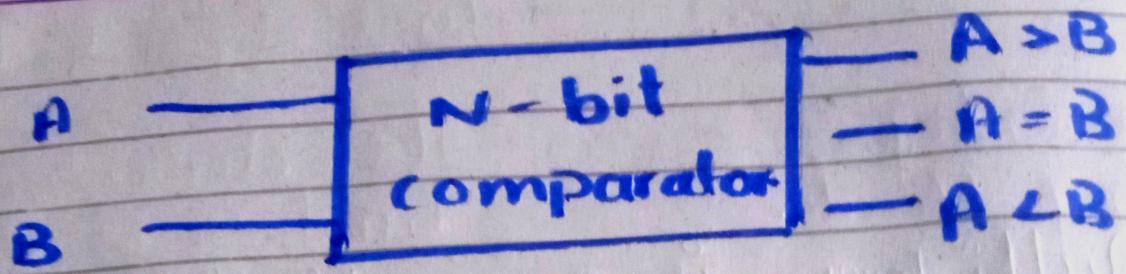
16:1 MUX

32:1 MUX.

— (xi) —

Comparators:

The function of comparator is to compare the magnitudes of two binary numbers to determine relationship between them.



— (xii) —

Function of Basic Shift register.

It consist of an arrangement of flipflops.

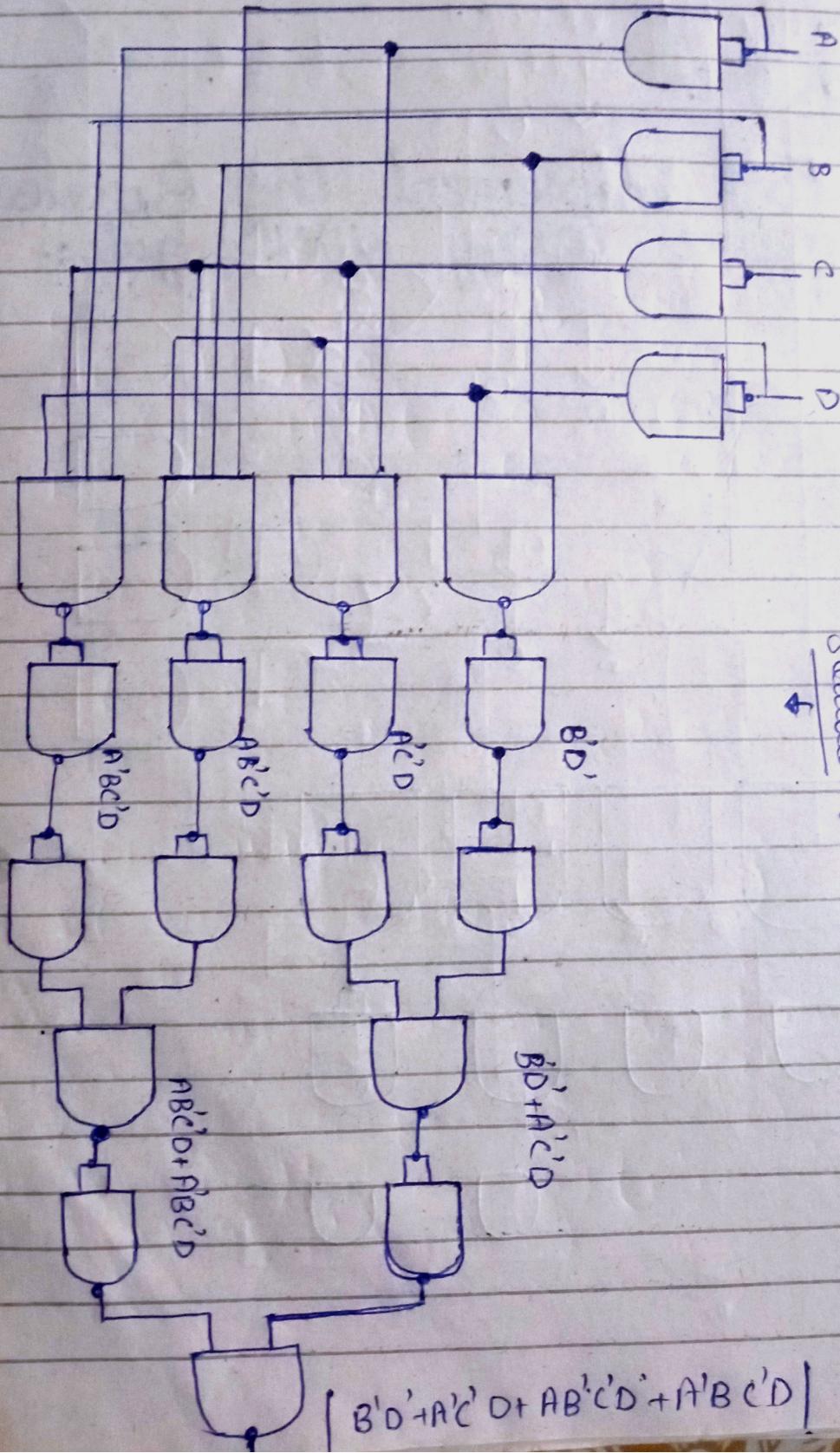
It important application involving storage and transfer of data.

It used for storing and shifting data (1's and 0's entered into it from an external source).

Long Question:-

Q6

(b) Implement the Boolean algebra using NAND gate.



$$B'D' + A'C'D + AB'C'D' + A'B'C'D$$

Solution:-

Q6 (a)

Si

[IC]

= (C

= CA' + A

= A + C

A +

1

Q6(a)

Simplify to 3 number
of literal.

$$[(CA) + A'] + A + CD + AB$$

Removing parentheses

$$= (CA') + A' + A + CD + AB$$

$$= CA' + A + A' + CD + AB \quad \therefore A + \bar{A}B = A + B$$

$$A + A'C = A + C$$

$$= A + C + A' + CD + AB$$

as $A + A' = 1$

$$= 1 + C + CD + AB$$

$\because A + AB = A$

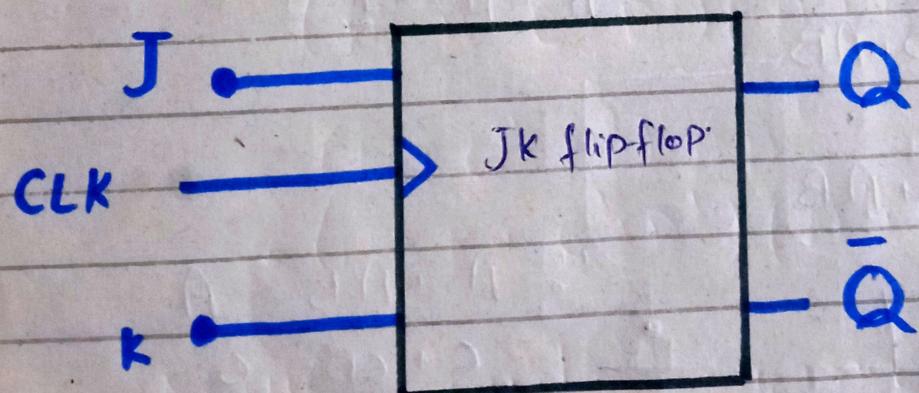
$$1 + C + AB$$

Q5:-

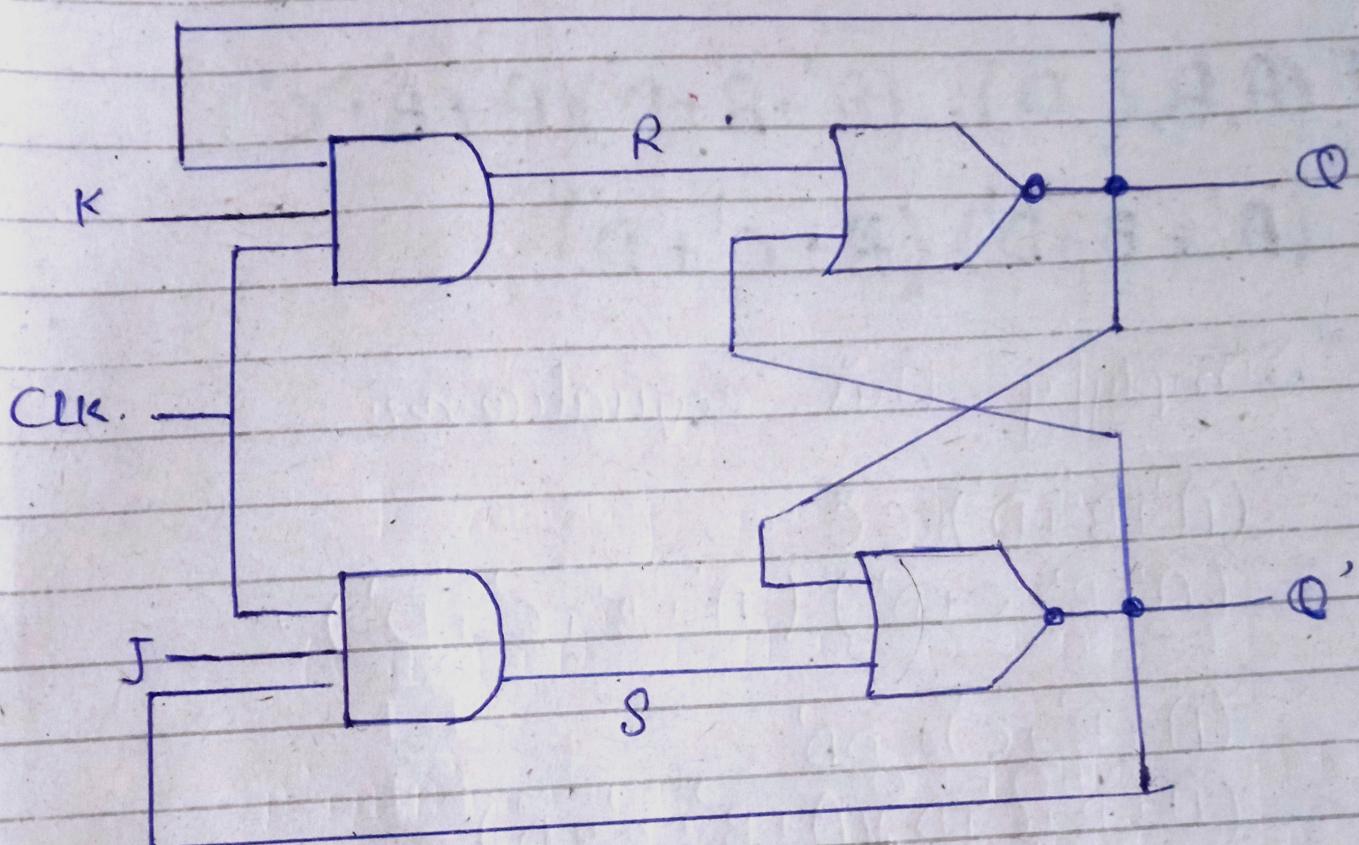
Draw truth table and logic diagram to explain Edge triggered JK Flip-Flop.

| Inputs | | | Outputs | | Comments |
|--------|---|-----|----------------|----------------|-----------|
| J | K | CLK | Q | \bar{Q} | |
| 0 | 0 | ↑ | Q ₀ | \bar{Q}_0 | No change |
| 0 | 1 | ↑ | 0 | 1 | Reset |
| 1 | 0 | ↑ | 1 | 0 | Set |
| 1 | 1 | ↑ | \bar{Q}_0 | Q ₀ | Toggle |

Symbol:-



Circuit diagram:-



Q 4:-

Simplify the function
The Karnaugh Map. Find SOP
and POS

$$F(A, B, C, D) = (A' + B' + D')(A + B' + C') \\ (A' + B + D')(B + C' + D')$$

Simplify this equation..

$$= (A' + B' + D') + C\bar{C} \\ = (A' + B' + C + D')(A' + B' + C' + D')$$

$$= (A + B' + C') + DD' \\ = (A + B' + C' + D')(A + B' + C' + D')$$

$$= (A' + B + D') + CC' \\ = (A' + B + C + D')(A' + B + C' + D')$$

$$= (B + C' + D')AA' \\ = (A' + B + C' + D')(A' + B + C' + D')$$

Now write arrange equation.

$$(A' + B' + C + D')(A' + B' + D' + D')(A + B' + C' + D), \\ (A' + B' + C' + D')(A' + B + C + D')(A' + B + C' + D) \\ (A + B + C' + D')(A' + B + C' + D')$$

| AB | CD | | 00 | 01 | 11 | 10 |
|------|------|---|----|----|----|----|
| 00 | 1 | 1 | 0 | 0 | 0 | 1 |
| 01 | 1 | 1 | 0 | 0 | 0 | 1 |
| 11 | 1 | 0 | 0 | 0 | 1 | |
| 10 | 1 | 0 | 0 | 0 | 1 | |

POS expression = ~~$A'D' + C'D + A'B'C'$~~
 $(A'+D')(C'+D')(A' B' C')$

| AB | CD | | 00 | 01 | 11 | 01 |
|------|------|---|----|----|----|----|
| 00 | 1 | 1 | 0 | 1 | | |
| 01 | 1 | 1 | 0 | 0 | | |
| 11 | 1 | 0 | 0 | 0 | | |
| 10 | 1 | 0 | 0 | 1 | | |

SOP :- $C'D' + A'C' + A'B'C'D + AC'D$
 expression.

Q 2:-

Draw circuit diagram of Half or Full adder. Draw truth table of half adder and boolean expression of half adder.

Half adder:-

$$0+0 = 0$$

$$0+1 = 1$$

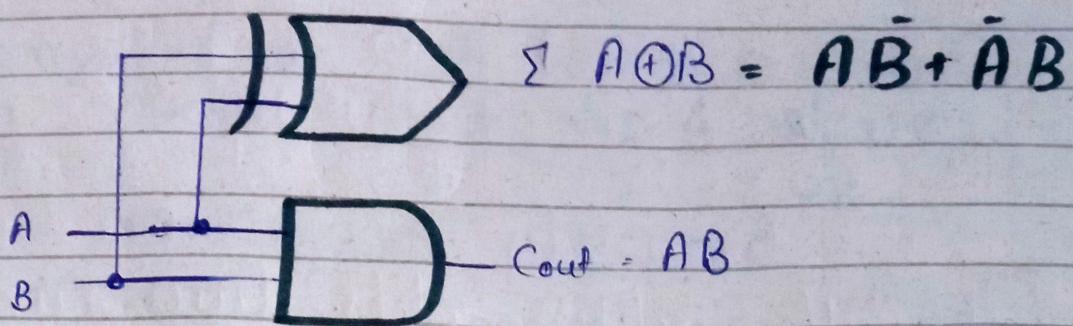
$$1+0 = 1$$

$$1+1 = 10$$

Truth table of Half adder

| A | B | C_{out} | Σ |
|---|---|-----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

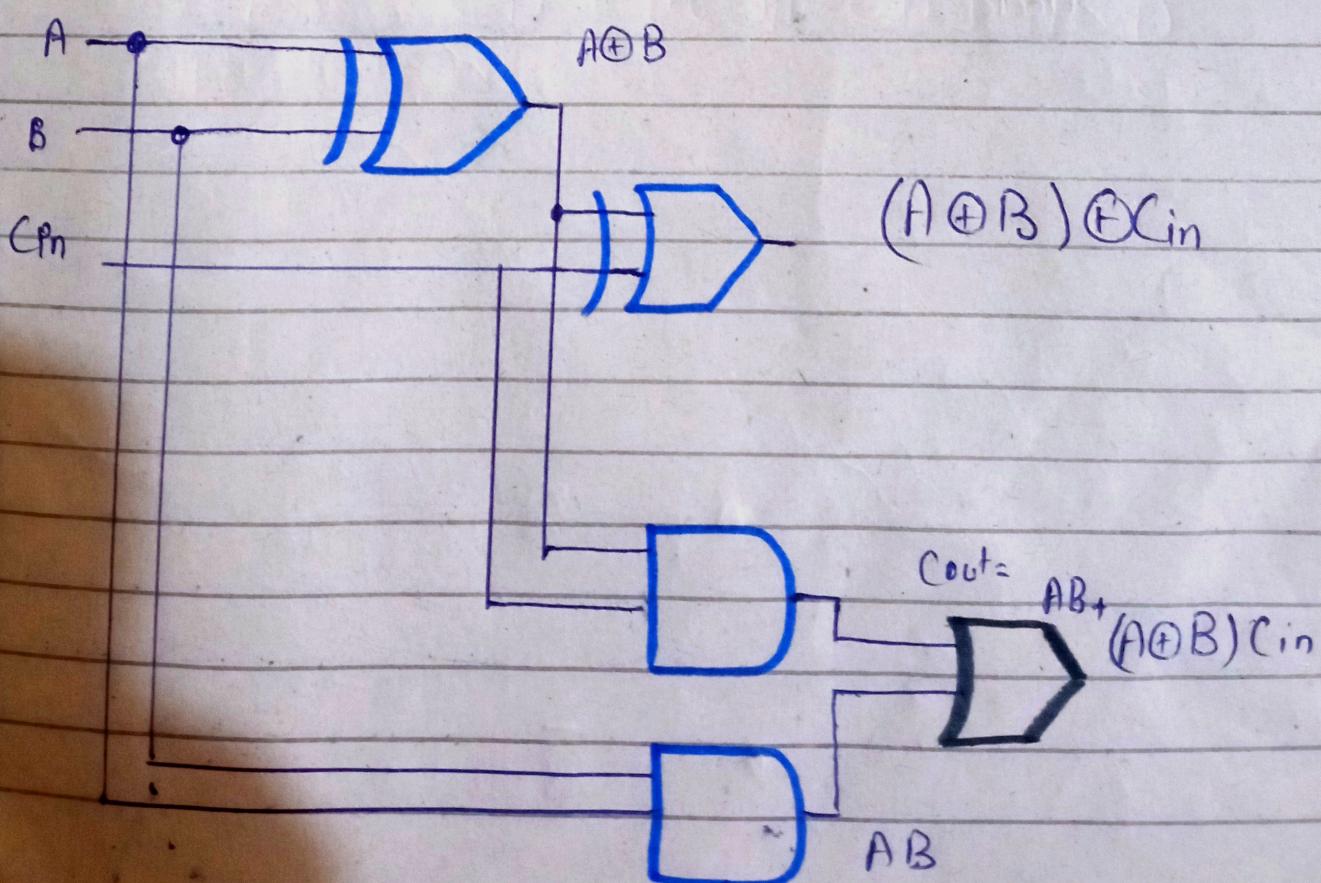
→ Circuit diagram (Half Adder)



Boolean Expression of
half adder.

$$A \oplus B = (\bar{A}\bar{B} + \bar{A}B)$$

→ Circuit diagram (Full adder)



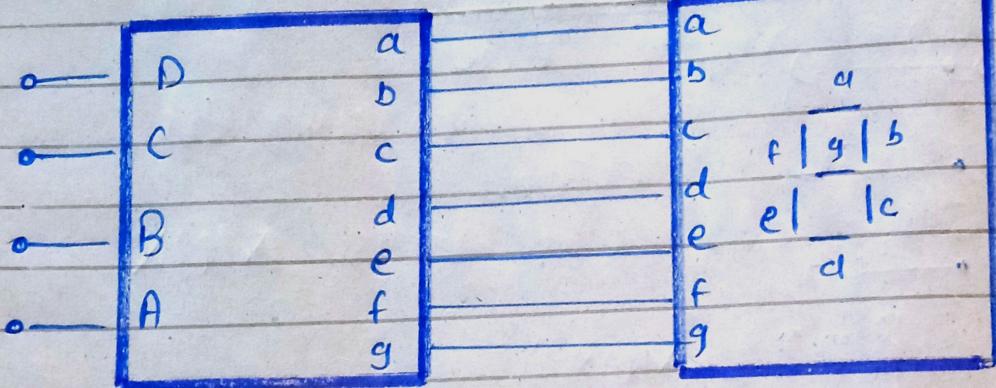
Q 3

Draw a 4-bit BCD to 7 segment and make truth table for C and Simplify:

$$= \bar{A}\bar{B}\bar{C}\bar{D}$$

$$\bar{A}BCD$$

$$AB$$



| A | B | C | D | a | b | c | d | e | f | g |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

$$\bar{A}BCD$$

$$+ A$$

$$\begin{aligned} & \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{B}CD \\ & + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + AB\bar{C}\bar{D} + A\bar{B}\bar{C}D \end{aligned}$$

| AB | | CD | | | |
|----|----|----|----|----|----|
| | | 00 | 01 | 11 | 10 |
| 00 | 00 | 1 | 1 | 1 | 0 |
| | 01 | 1 | 1 | 1 | 1 |
| 11 | X | X | X | X | X |
| 10 | 1 | 1 | X | X | X |

~~C = D'~~

$$C = \bar{C} + D + B$$