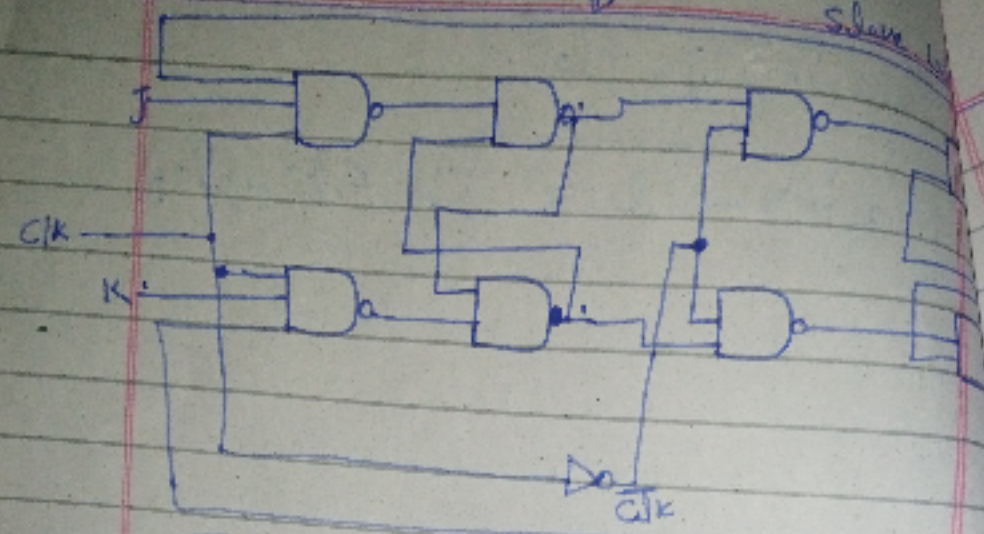
Master Latch

Slave



Table

Trigger ~~Clk~~ Clk	Inputs J	Inputs K	present state Q	present state $\overline{Q}$	next state Q	next state $\overline{Q}$
⎍	0	0	0	1	0	1
⎍	0	0	1	0	1	0
⎍	0	1	0	1	0	1
⎍	0	1	1	0	0	1
⎍	1	0	0	1	1	0
⎍	1	0	1	0	1	0
⎍	1	1	0	1	1	0
⎍	1	1	1	0	0	1

Two JK flip flop.

Master-Slave JK Flip-flop

The master-salve flip-flop eliminates all the timing problems by using two SR flip-flops connected together in a series configuration. one flip-flop acts as the "Master" circuit which triggers on the leading edge of the clock pulse while The other acts as the "Slave" circuit, which triggers on the falling edge of the clock pulse. This result in the two sections, the master section and the slave section being enabled during opposite half-cycles of the clock signal.

Example:-

TTL 74LS73 is a dual JK flip-floop IC.

Glitch in digital logic

Gleaches are unwanted signals that occur in the circuit.

the Gleaches can observed in flipflops.

Gleach will damag the circuit at times.

What is the Identity Law

Identity Law in which The term of the OR gate is end with a "0" or AND gate end with a "1" will always equal that the variable is called the Identity Law.

Proof:-

A variable, OR gate end with 0 is always equal to the variable.

$A+0=A$
$A+A+0=A$
$A+0+0=A$
$A+A+A+0=A$
$A+0+0+0=A$

In which OR gate contain 0 and variable its identity Law otherwise its law invalid.

is always equal to the variable because it end on the "0".

If it end on the "1" it is not equal to variable

$A+1=1 \Rightarrow \neq A$

$A+A+A+A+1=1 \Rightarrow \neq A$

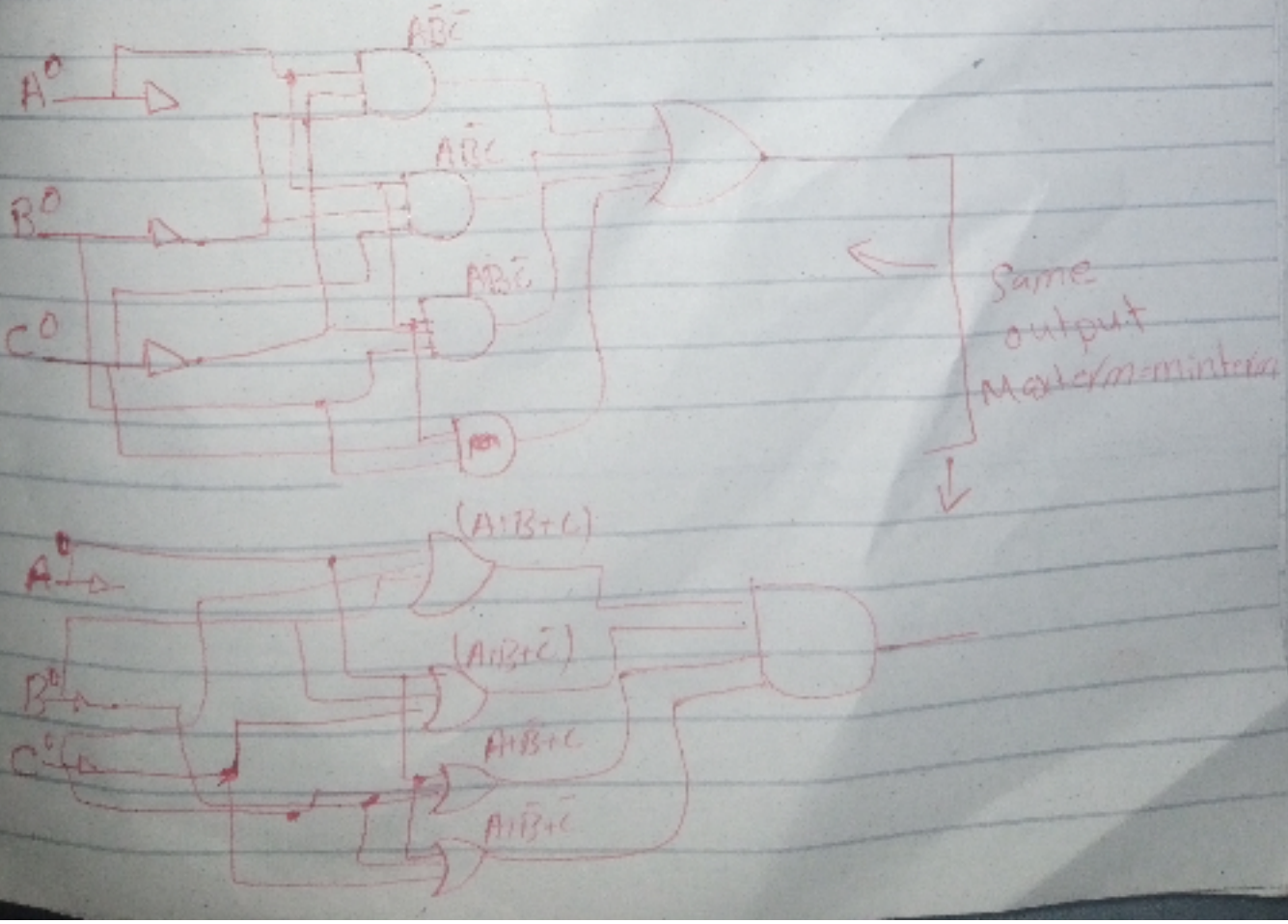
Ex

$(A+AB)(A+C)$

A	B	C	AB	(A+AB)	A+C	(A+AB)(A+C)	
0	0	0	0	0	0	0	
0	0	1	0	0	1	0	Max term
0	1	0	0	0	0	0	
0	1	1	0	0	1	0	
1	0	0	0	1	1	1	
1	0	1	0	1	1	1	Minterm
1	1	0	1	1	1	1	
1	1	1	1	1	1	1	

$Minterm = A\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C} + ABC$

$Maxterm = (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})$



What is the Identity Law

Identity Law in which The term of the OR gate is end with a "0" or AND gate end with a "1" will always equal that the variable is called the Identity Law.

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$A + 0 = A$
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$A + 0 + 0 = A$
$A + A + A + 0 = A$
$A + 0 + 0 + 0 = A$

In which OR gate contain 0 and variable its identity Law otherwise it's law invalid.

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$A + 1 = 1 \Rightarrow \neq A$

$A + A + A + A + 1 = 1 \Rightarrow \neq A$

What is glitch?

A glitch happens sometimes as signals propagate through combinational logic. Before reaching the final steady state value, sometimes a wrong intermediate value shows up at the output during the setting phase. This is called a glitch.

Reason

The reason why it happens is because of the different signal paths have different delays. So when one input reaches the input of a gate while the other input is delayed the wrong output may occur. The output signal will be corrected once all of the correct input has propagated through.

$f = \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}\bar{C} + ABC$

Minterm

A	B	C	$\bar{A}$	$\bar{B}$	$\bar{C}$	$AB\bar{C}$	$A\bar{B}\bar{C}$	ABC	$A\bar{B}C$	f
0	0	0	1	1	1	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0
1	0	0	0	1	1	0	1	0	0	1
1	0	1	0	1	0	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	1	0	0	0	0	0	1	0	1

$f = (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})$

Maxterm

A	B	C	$\bar{A}$	$\bar{B}$	$\bar{C}$	$(A+B+C)$	$A+B+\bar{C}$	$A+\bar{B}+C$	$A+\bar{B}+\bar{C}$	f
0	0	0	1	1	1	0	1	1	1	0
0	0	1	1	1	0	1	0	1	1	0
0	1	0	1	0	1	1	1	0	1	0
0	1	1	1	0	0	1	1	1	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	1	0	1	0	1	1	1	1	1
1	1	0	0	0	1	1	1	1	1	1
1	1	1	0	0	0	1	1	1	1	1

Some function so we convert correctly to maxterm to minterm and minterm to maxterm.

f

$A\bar{B}\bar{C}+A\bar{B}C+AB\bar{C}+ABC$

Minterm

A	B	C	$\bar{A}$	$\bar{B}$	$\bar{C}$	$A\bar{B}\bar{C}$	$A\bar{B}C$	$AB\bar{C}$	ABC	f
0	0	0	1	1	1	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0
1	0	0	0	1	1	1	0	0	0	1
1	0	1	0	1	0	0	1	0	0	1
1	1	0	0	0	1	0	0	1	0	1
1	1	1	0	0	0	0	0	0	1	1

f

$(A+B+C)(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})$

Maxterm

A	B	C	$\bar{A}$	$\bar{B}$	$\bar{C}$	$(A+B+C)$	$A+B+\bar{C}$	$A+\bar{B}+C$	$A+\bar{B}+\bar{C}$	f
0	0	0	1	1	1	0	1	1	1	0
0	0	1	1	1	0	1	0	1	1	0
0	1	0	1	0	1	1	1	0	1	0
0	1	1	1	0	0	1	1	1	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	1	0	1	0	1	1	1	1	1
1	1	0	0	0	1	1	1	1	1	1
1	1	1	0	0	0	1	1	1	1	1

same function
so we convert correctly to maxterm to minterm and minterm to maxterm.