University of Sargodha

BS 2nd Term Examination 2019

Subject: Computer Science **Paper: Digital Logic Design (CMP-2210)**

Time Allowed: 2:30 Hours **Maximum Marks: 80**

Note: Objective part is compulsory. Attempt any three questions from subjective part.

Objective Part (Compulsory)

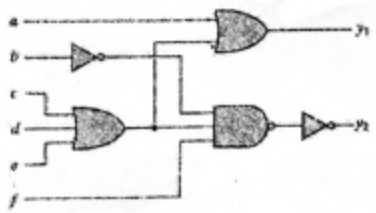
Q.1. Write short answers of the following in 2-3 lines each on your answer sheet. (16*2)

i. Convert the given number $(144)_8$ into binary?
ii. Use10's complement to perform M-N when M=85320 and N=51360
iii. Write the following function into maxterms $F=\sum(2,4,5,6)$
iv. State Duality principle?
v. Using postulates and theorems of Boolean algebra prove x+xy=x
vi. Simplify the following Boolean function using k-map
F(A,B)=A'B'+AB'+AB
vii. Draw the Truth table of half subtractor and write the Boolean function for its Borrow and Difference?
viii. What is the multiplexer?
ix. Draw the logic circuit which performs addition between two input values?
x. Define Register and its type?
xi. What is Karnaugh?
xii. Obtain the 1's and 2's complement of the following binary function
0010001, 0111010, 010100, 1011101
xiii. Draw the gate implementation of the following expression.
AB+A(B+C)+B(B+C)
xiv. Prove that exclusive-OR is the compliment of exclusive-NOR?
xv. Expand the following Boolean functions into their canonical form:
$f(A, B, C) = AB + A'C + AB'C$
xvi. What is 4-bit binary parallel adder?

Subjective Part (3*16)

Q.2 Determine the base b in each of the following cases:
(a) $(361)_{10} = (551)_b$
(b) $(982)_{10} = (1726)_b$

Q.3. Write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the logic diagram.



Q.4. Simplify the Boolean function
$F(w, x, y, z) = \sum (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. Find both SOP and POS expression.

Q.5. Draw circuit diagram of half adder and full adder. Draw truth table of half adder. Also write expression of half adder only. Show how a full adder can be converted to a full subtracter?

Q.6. What is Demultiplexer? Explain with 2 to 4 line Decoder with enable input and define its truth table and block diagram?