University of Sargodha

BS 2nd Term Examination 2017

Subject: Computer Science/Software Engineering **Paper: Digital Logic Design (CMP:2210)**

Time Allowed: 2:30 Hours **Maximum Marks: 80**

Note: Objective part is compulsory. Attempt any three questions from subjective part.

Objective Part (Compulsory)

Q.1. Write short answers of the following in 2-3 lines each. (16*2)

i. Convert into equivalent binary number $(1AF)_{16}$
ii. Write BCD equivalent of Excess-3.
iii. Express -99 as an 8-bit number in the sign-magnitude, 2's complement form.
iv. Add the following BCD numbers: 10110110 + 10011101
v. Using Boolean algebra techniques, simplify this expression: $A \cdot B + A \cdot (B + C) + B \cdot (B + C)$
vi. State Demorgan's law to verify that negative-OR gate is equivalent to NAND gate.
vii. Prove that $A + \overline{A} \cdot B = A + B$
viii. Draw the gate implementation of the function: $A + B \cdot C + A \cdot B \cdot \overline{C}$
ix. Minimize the following SOP using K-Map: $A \cdot B \cdot C + \overline{A} \cdot B \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot \overline{C} + A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C}$
x. Determine the logic required to decode $(1011)_2$ by producing a HIGH on the output.
xi. Draw diagram of SR-Latch using NAND-gates.
xii. Explain how an Exclusive-NOR gate is used to compare to binary bits.
xiii. What is difference between Serial in/ Parallel out registers and Parallel in /Parallel out registers?
xiv. What is latch? Draw logic circuit for SR latch.
xv. What is difference between Asynchronous counter and Synchronous counter?
xvi. Draw the logic diagram of XOR gate using all NAND-gates.

Subjective Part (3*16)

Q.2. What are counters? Draw BCD up/down counter using synchronous counter.

Q.3. Convert the following Boolean expression into Standard SOP:

$\overline{B} \cdot \overline{C} + A \cdot \overline{B} + A \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot C \cdot \overline{D} + \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D + A \cdot \overline{B} \cdot C \cdot D$

Map the standard SOP on a K-map simplify and implement it using logic diagram.

Q.4. Differentiate between Look ahead Carry Adders and Ripple carry.

Q.5. Suppose you are working as a lead engineer in Ferrari Corporation it is observed that in hilly areas Ferrari is experiences fatal accidents due to break failure of all four wheels. You are requested to design a simple and cost effective safety strategy to overcome and reduce chances of accidents.

It is an advice given by your higher management that if two or more than two breaks of wheels fail an alarm must be triggered for the driver. This alarm will help driver to reduce speed or visit workshop for maintenance.

Q.6. Implement an Edge- Triggered T flip flop. Describe its functioning and draw truth table.