Q. No. 2: Simplify the following Boolean equations using Boolean theorems. Check for correctness using a truth table or K-map.

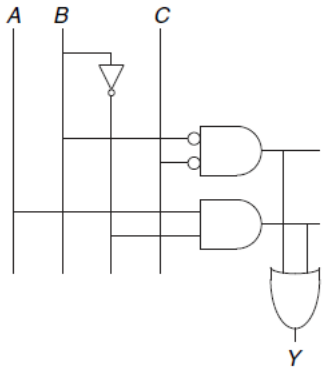
$$Y = ABC + ABD + ABE + ACD + ACE + \overline{(A + D + E)} + \overline{B}\,\overline{C}D + \overline{B}\,\overline{C}E + \overline{B}\,\overline{D}\,\overline{E} + \overline{C}\,\overline{D}\,\overline{E}$$

Q. No. 3: Draw a 3:2 multiplexer with minimum number of gates.

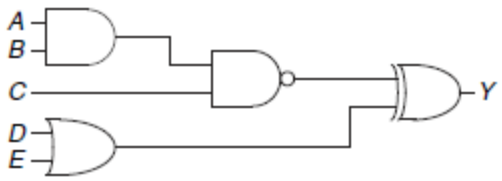
Q. No. 4: Following table shows the truth table for a Boolean function Y. Using De Morgan's Theorem, derive the product-of-sums canonical form of Y from the sum-of-products form of complement of Y.

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Q. No. 5: Given the following logic circuit, draw an equivalent logic circuit with max-terms.



Q. No. 6: Find the propagation delay and contamination delay of the circuit shown in the following circuit. According to his data book, each gate has a propagation delay of 100 picoseconds (ps) and a contamination delay of 60 ps.



Q. No. 2: Simplify the following Boolean equations using Boolean theorems. Check for correctness using a truth table or K-map.

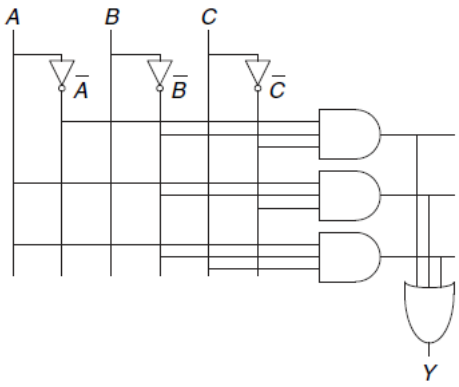
$$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}\,\overline{C} + A\overline{B}C\overline{D} + ABD + \overline{A}\,\overline{B}C\overline{D} + B\overline{C}D + \overline{A}$$

Q. No. 3: Draw a 4:1 multiplexer with minimum number of gates.

Q. No. 4: Following table shows the truth table for a Boolean function Y. Using De Morgan's Theorem, derive the product-of-sums canonical form of Y from the sum-of-products form of complement of Y.

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Q. No. 5: Given the following logic circuit, draw an equivalent logic circuit with max-terms.



Q. No. 6: Find the propagation delay and contamination delay of the circuit shown in the following circuit. According to his data book, each gate has a propagation delay of 80 picoseconds (ps) and a contamination delay of 50 ps.