

University of Sargodha

BS 2nd Semester/Term Exam 2021

Subject: Information Technology

Paper: Digital Logic and Design (ITSC-102)

Time Allowed: 02:30 Hours

Maximum Marks: 60

Note: Objective part is compulsory. Attempt any three questions from subjective part.

Objective Part (Compulsory)

Q.1. Write short answers of the following in 2-3 lines each on your answer sheet (2*12)

- i. What are literals?
- ii. Write dual of $0 \cdot 1 = 1 \cdot 0 = 0$
- iii. Define null element theorem
- iv. What are decoders?
- v. What are priority circuits?
- vi. What are arithmetic circuits?
- vii. What is a propagation delay?
- viii. What is minimum number of bits that can be added using a full adder?
- ix. What are synchronous sequential circuits?
- x. A flip-flop copies input to output on which edge of the clock?
- xi. A divide-by-N counter has how many outputs?
- xii. What is a synchronizer?

Subjective Part (3*12)

Q.2. Simplify the following Boolean equations using Boolean theorems. Check for correctness using a truth table or K-map.

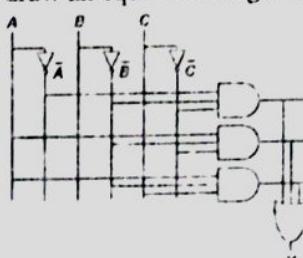
$$Y = \overline{A}BCD + AB\overline{C} + ABC\overline{D} + ABD + \overline{A}\overline{B}CD + B\overline{C}D + \overline{A}$$

Q.3. Draw a 4:1 multiplexer with minimum number of gates.

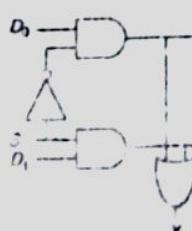
Q.4. Following table shows the truth table for a Boolean function Y. Using De Morgan's Theorem, derive the product-of-sums canonical form of Y from the sum-of-products form of complement of Y.

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Q.5. Given the following logic circuit, draw an equivalent logic circuit with max-terms.



Q.6. Find the propagation delay and contamination delay of the circuit shown in the following circuit. According to his data book, each gate has a propagation delay of 80 picoseconds (ps) and a contamination delay of 50 ps.



2021 Past Paper:

— (i) —

What are literals?

A literal is a Boolean variable
or The complement of a
Boolean variable.

— (ii) —

Write dual of

$$0 \cdot 1 = 1 \cdot 0 = 0$$

In XOR (exclusive or) gate
output true (1) when number
of true input is odd.
It could be represented as

$$0 \oplus 1 = 1 \oplus 0 = 0$$

— (iii) —

Null Element Theorem.

The output value is not
affected by the changes in
the input value

and $x+1=1$
based on duality

$$x \cdot 0 = 0$$

— (iv) —

Decoders:

There are n input lines in the decoder.

If it is combinational circuit
that convert coded bits into original information.

or There 2^n output lines in decoder.

— (v) —

What are priority circuits?

A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs.

It has 2^n input lines and m output lines

— (vi) —

What are arithmetic circuits?

A arithmetic circuit is set gate with separate set of input for each number that has to be processed. The gates are connected so to carry out an arithmetic action. and The output of gates circuit are digit of result (addition, subtraction, multiplication etc.)

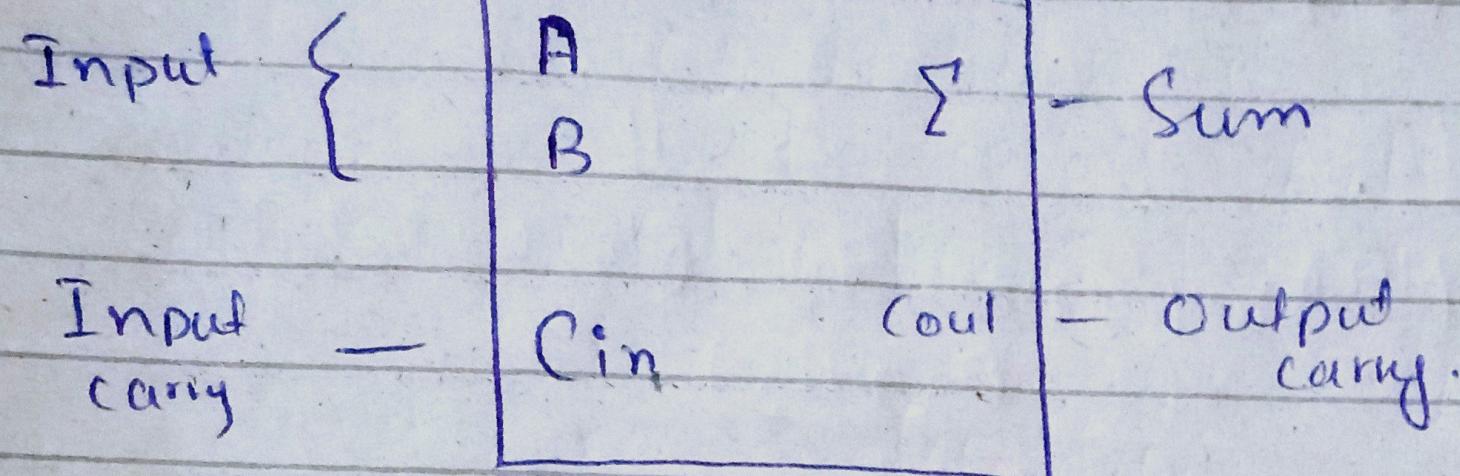
— (vii) —

Propagation delay:-

If is length of time which start when input to a logic gate begins to change, to The time of logic gate output is stable and valid to change.

(v iii)

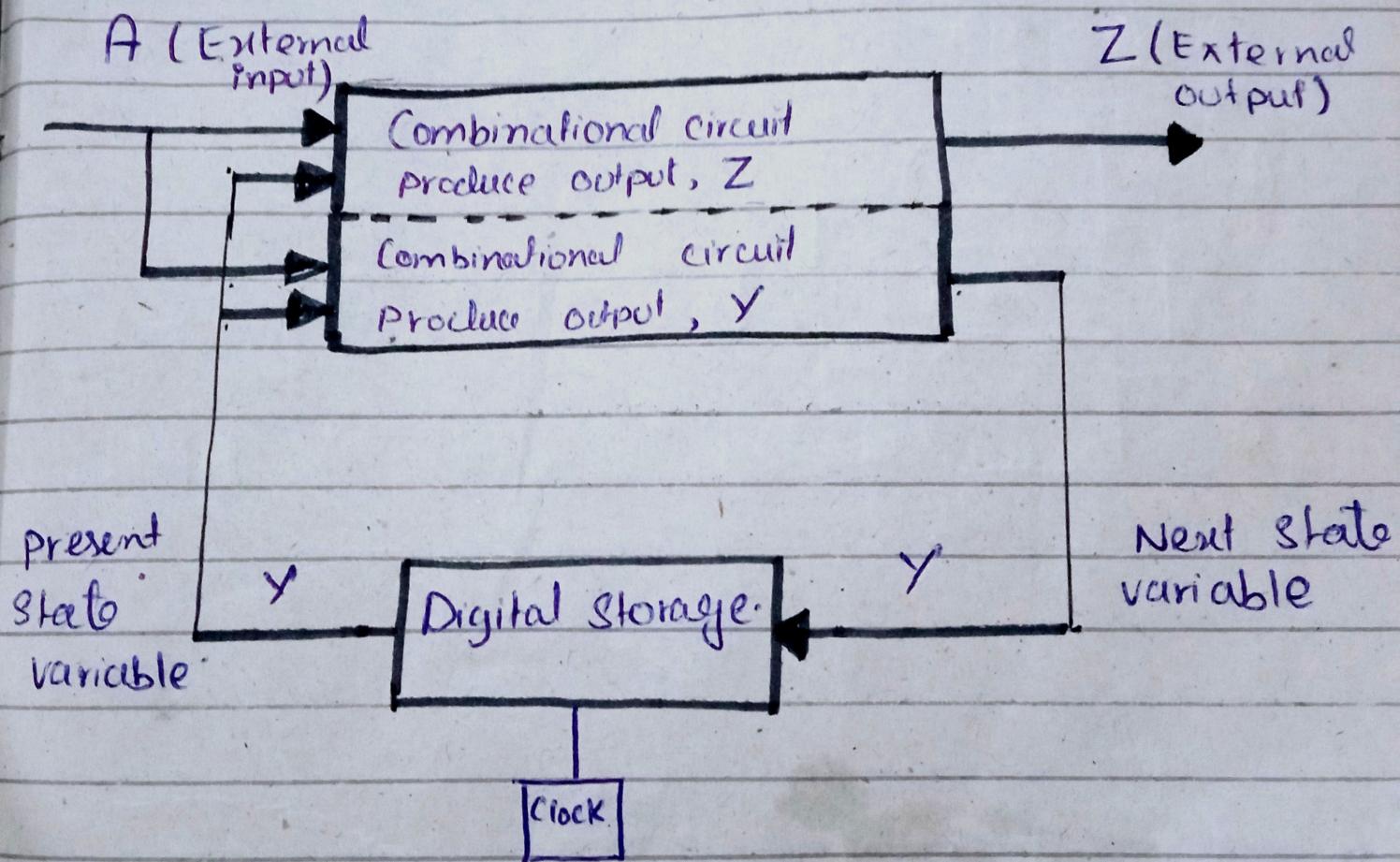
A full adder have three bits (two operands and a carry in) to produce a sum and a carry out.



—(9)—

Synchronous sequential circuit:

Digital circuit that uses clock signal to determine the timing of their operations.

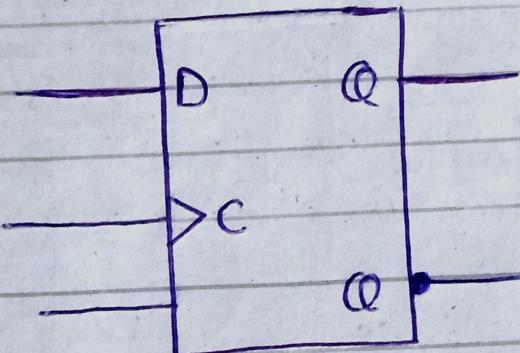


—(10)—

A flip flop copies input to output on which edge of clock?

- Positive edge-triggered.
- Negative edge-triggered.

→ In positive edge-triggered.



(a) positive edge

—(11)—

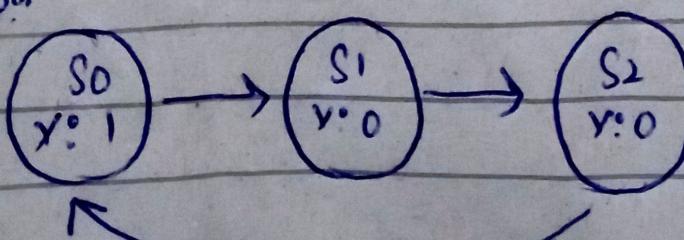
A divided by N-counter how many output

There is only one output without input.

The output y is high for one cycle out every one.

Example:

Reset



Synchronizer:-

A Synchronizer is a digital circuit that converts asynchronous or signals from different clock domains into receiver clock domain so that capturing would not cause any metastability.

Long Answer

Q4:

A	B	C	D	Y
0	0	0	1	0
0	0	0	0	0
0	0	1	0	1
0	0	1	1	1
0	0	0	0	0
0	1	0	1	1
0	1	0	0	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

In POS

$$Y = (A + B + C + D) (A + B + \bar{C} + \bar{D}) (A + \bar{B} + C + \bar{D}) \\ (A + \bar{B} + \bar{C} + D) (\bar{A} + B + C + D) (\bar{A} + B + \bar{C} + D) \\ (\bar{A} + \bar{B} + C + D) (\bar{A} + \bar{B} + \bar{C} + \bar{D})$$

Now apply deMorgan Theorem

$$= \overline{(A + B + C + D)(A + B + \bar{C} + \bar{D})(A + \bar{B} + C + \bar{D})(\bar{A} + \bar{B} + \bar{C} + D)} \\ \overline{(\bar{A} + B + C + \bar{D})(\bar{A} + B + \bar{C} + D)(\bar{A} + \bar{B} + C + D)(\bar{A} + \bar{B} + \bar{C} + \bar{D})}$$

SOF
= AB
AB

Q5:

SOP

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$$

$$A\bar{B}\bar{C}D + A\bar{B}CD + AB\bar{C}\bar{D} + ABCD.$$

See it is expression

Q5:-

In SOP form:

$$\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C$$

AB	C	
00	0	1
01		
10	1	1

$$\bar{B}\bar{C} + A\bar{B}$$

