ALUControl:module3

ALUOP[1..0]
function_field[5..0]
ALU_control_lines[3..0]

control:module2

ALU OP0
ALU OP1
ALUSrc
Branch
MemRead
MemWrite
MemtoReg
RegDst
RegWrite

opcode[5..0]

31:26

5:0

execute:module5

ALU_control_lines[3..0]
ALUSrc
immediate[31..0]
read_data1[31..0]
read_data2[31..0]
ALU_result[31..0]

memory:module6

ALU_result[31..0]
MemRead
MemWrite
MemtoReg
clock
write_data[31..0]
data_out[31..0]

decode:module4

clock
instruction[31..0]
regDst
regWr
reset
write_data[31..0]
immediate[31..0]
read_data1[31..0]
read_data2[31..0]

clock

reset

fetch:module1

clock
reset
instruction[31..0]

ALUSrc
32'h0 write_data[31..0]

ALU_result[31..0]
ALUOP[1..0]
ALUOP0
ALUOP1
Branch
MemRead
MemWrite

data_out[31..0]

RegDst
RegWrite
MemtoReg

5:0 function_field[5..0]
instruction[31..0]
31:26 opcode[5..0]