Experiment #2 General DC Circuits

2.1 Introduction:

In most practical circuits, devices are neither connected in simple series nor simple parallel form. Practical devices are connected in various circuit configurations that generally consist of combinations of both series and parallel forms. Some of these circuit connections have standard forms that are identified by such names as **ladder, lattice, tee, pi, wye,** and **delta** networks, to mention but a few. In the process of designing an electrical system, circuit designers try various circuit configurations, evaluate their performances, and select the one that meets or exceeds the design objectives at minimum cost.

This experiment examines the behavior of a general dc circuit, and deals with the design and performance-evaluation of a simple voltage-divider circuit.

Reference: Text; chapter three.

2.2 Objectives:

- To investigate the performance of a general dc circuit.
- To become familiar with the concept of circuit (reference point) ground.
- To design, construct, and test the performance of a simple voltage-divider circuit.

2.3 Prelab Assignment:

1- Consider the general dc circuit shown in Fig (2.1). Through measurements, it is found that the voltage of node # **3** [w.r.t. circuit ground] is **+6V.** Find all the missing data in the following table.

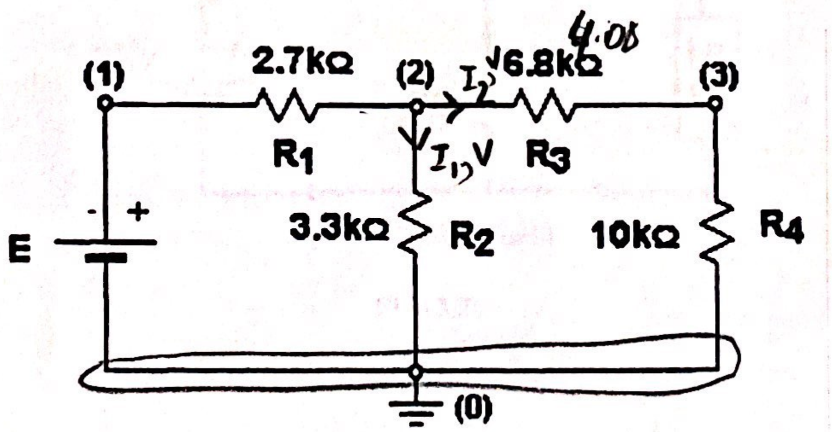


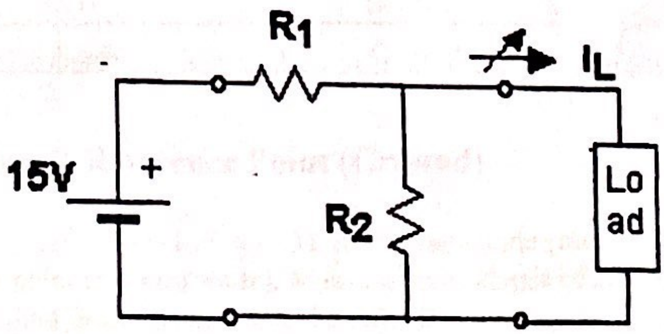
Fig (2.1)

	Device	Voltage across (V)	Current through (mA)	Absorbed Power (mW)
	Source	19.87	0.93	18.5
2.7KΩ	R_1	9.828	0.93	9.141
3.3KΩ	R_2	10.08	0.33	3.31
6.8KΩ	R_3	4.08	0.60	2.45
10KΩ	R_4	6.00	0.60	3.60

2- Given a circuit similar to that in Fig (2.1), but without any numerical values for its components. Use the symbols: "↑" for increase, "↓" for decrease, and "=" for no change, in the following table, to show the effects of an **increase in the value of R_2** on the voltage, current, and power of all devices.

Device	Voltage across	Current through	Absorbed Power
Source "="	=	=	=
R_1 "="	↓	=	↓
R_2 "↑"	↑	=	↑
R_3 "="	↑	=	↑
R_4 "="	↑	=	↑

3- Fig (2.2) shows a **simple voltage-divider** connecting a dc voltage source to a **variable** resistive load. Design the voltage divider to provide a voltage of **about 5V (± 10 %)** across the variable load. The load-current demand varies in the range of **0 to 5mA,** and the available dc-supply voltage is **15V.**



[voltage divider]

Fig (2.2)

2.4 Procedure:

Part I. General DC Circuit

1- Construct the circuit shown in Fig (2.1). Adjust the value of the source voltage **"E"** to set the voltage of node #3 @ **6V.** Measure all node voltages **(w.r.t. the reference node)** and all branch currents. Calculate the voltage across and the power absorbed by each device, and record your results in table (2.1).

Table (2.1)

Device	Voltage across (V)	Current through (mA)	Absorbed Power (mW)
Source	20.00	3.66	73.2
R_1	9.89	3.66	36.2
R_2	10.10	3.01	30.4
R_3	4.09	0.60	2.45
R_4	6.00	0.60	3.60

2- Replace R_2 with a **4.7 kΩ** resistor. Repeat step # 1 and record your results in table (2.2).

Table (2.2)

Device	Voltage across (V)	Current through (mA)	Absorbed Power (mW)
Source	20.00	3.14	62.8
R_1	8.48	3.14	26.6
R_2 =4.7k "↑"	11.53	2.45	28.2
R_3	4.67	0.69	3.22
R_4	6.86	0.69	4.73

Part II. Circuit Reference Point (Ground)

3- Connect the circuit shown in Fig (2.3). Select each node **(one at a time)** in the circuit as the reference point **(ground node).** Measure the voltages of all other nodes w.r.t. the ground node, and record your results in table (2.3).

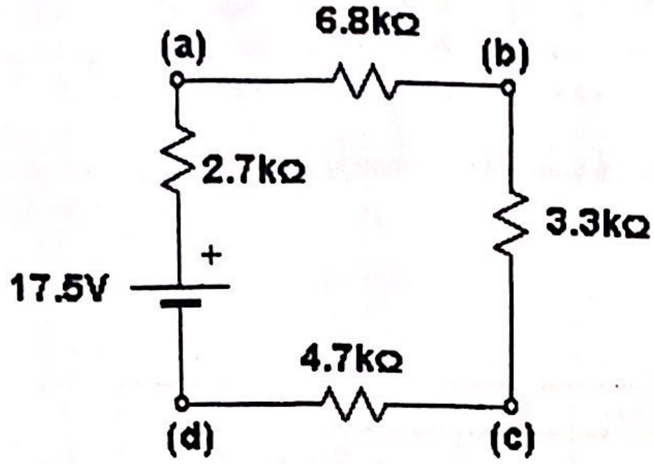


Fig (2.3)

Table (2.3) [Voltage measured @ other nodes w.r.t. the selected ground node (V)]

Ground node #	V_a	V_b	V_c	V_d
a	0.0	6.8	10.1	14.8
b	-6.8	0.0	3.3	8
c	-10.1	-3.3	0.0	4.7
d	-14.8	-8	-4.7	0.0

Part II . Voltage-Divider

4- Connect your own **voltage-divider** circuit as shown in Fig (2.4); use a decade resistance box **(whose settings are at their maximum value)** as the variable resistive load.

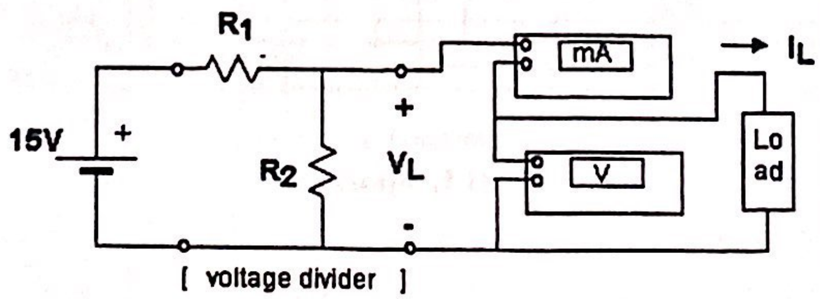
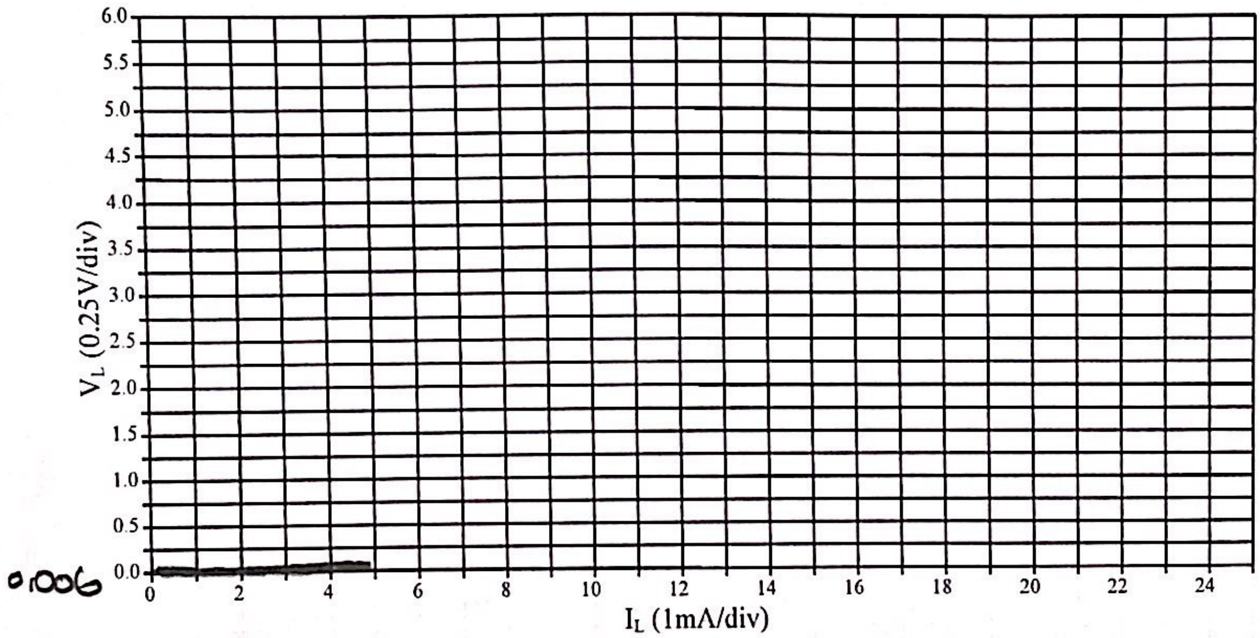


Fig (2.4)

5- With the decade resistance box open circuit; i.e., the load current **I_L = 0.0 A,** measure the value of the load voltage **V_L**. Reconnect the decade box and adjust its resistance settings to provide each of the values of **I_L** shown in table (2.4). For each setting of **I_L** measure the corresponding value of **V_L**.
Use Graph (2.1) to plot **V_L** vs **I_L** [which is known as the **load-regulation characteristic]** of your voltage-divider circuit.

Table (2.4)

I_L(mA)	0	1	3	5	7	10	15	20	25
V_L(V)	0.00623	0.00623	0.00623	0.00623					



Graph (2.1)

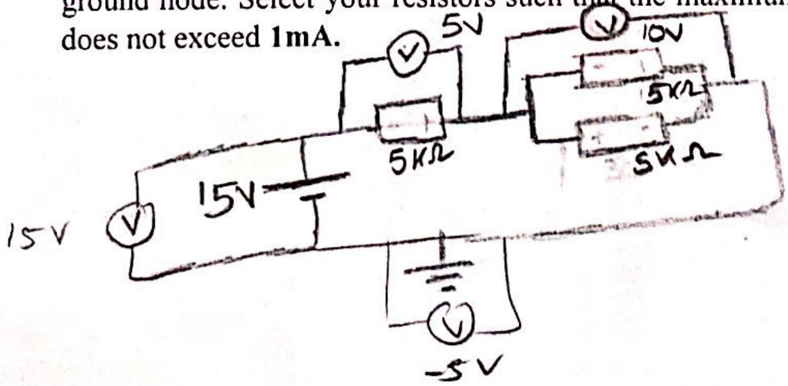
2.5 Conclusions:

1- Use your recorded data in table (2.1) to verify KVL for each loop and KCL at each node for the general dc circuit.
Comment on the possible causes for any deviations from what you would expect theoretically.

KVL: ① voltage is divided according to the ratios of Resistance when componets connected in series but current is constant

KCL: ② Current is divided accross componets inversly to their resistance when connected in parrallel

2- Based on your observations from step # 3, design a dc circuit utilizing a **15V** voltage battery to provide the following node voltages: **+10V**, **+5V**, and **-5V** w.r.t. a circuit ground node. Select your resistors such that the maximum power demand on the battery does not exceed **1mA**.



$V = IR$

$\frac{5}{1} =$ | $\frac{10}{1} =$ 10 KΩ

$\frac{1}{10} = \frac{1}{R_1} + R_2$

$10 = 30 \times I$

$\frac{1}{30} = I$

3- Explain your observation of the **load-regulation characteristic** on Graph (2.1). Does your voltage-divider circuit meet the design objectives?

The ressistance does not
affect the voltage only the current
because The load is connected in parrallel
with another ressistor