Ryerson University Faculty of Science

Department of Physics

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Lab/Tutorial Report No.	*4*

Report Title	*Lab 4 Part 2*

Section No.	*03*
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Objective

The objective of this lab was to build and modify the code for a Johnson counter such that every cycle/count the circuit out puts digit of my student number starting from the 4^{th} digit up to the last a 9^{th} digit spanning a total of 6 cycles.

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Procedure

VHDL code for the Johnson Counter:

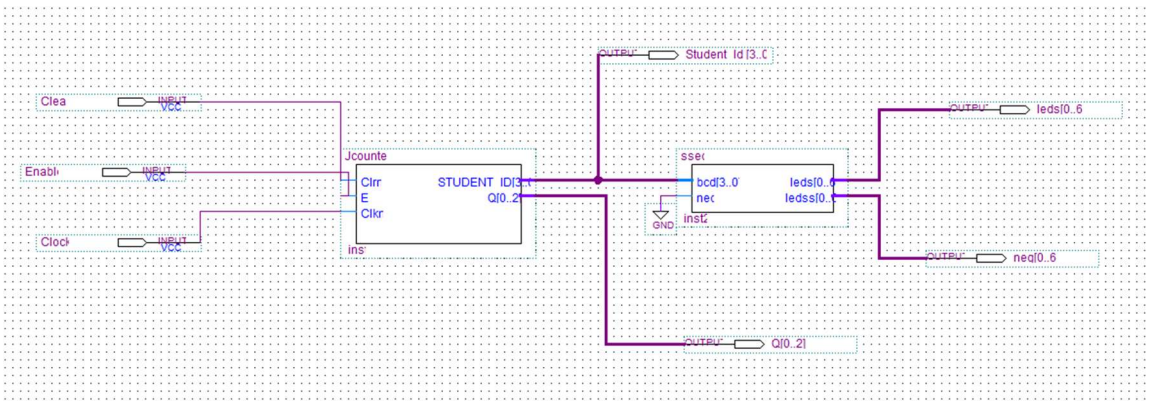
```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY Jcounter IS

PORT (Clrn, E, Clkn : IN STD_LOGIC; --clrn is your reset button
   STUDENT_ID : out std_logic_vector(3 downto 0);
   Q : OUT STD_LOGIC_VECTOR (0 TO 2));
END Jcounter;

ARCHITECTURE Behavior OF Jcounter IS
signal Qreg : STD_LOGIC_VECTOR (0 TO 2);
BEGIN
   PROCESS (Clrn, Clkn)
      BEGIN
         IF Clrn = '0' THEN
            Qreg <= "000";
         ELSIF (Clkn'EVENT AND Clkn = '0') THEN
         IF E = '1' THEN  -- complete your Jcounter flip-flop outputs here
            Qreg(1) <= Qreg(0);
            Qreg(2) <= Qreg(1);
            Qreg(0) <= not Qreg(2);
         ELSE
            Qreg <= Qreg;
         END IF;
      END IF;
      -- STUDENT_ID variable represents the last 6 digits of your student ID hence d4 is
      --the fourth digit of your --student ID in four bits, d5 is the fifth and so on.
      --For example, for Student ID 500435429, --d4 is 0100, d5 is 0011 and so on

   CASE Qreg IS

      WHEN "000" => STUDENT_ID <= "0000"; --d1
      WHEN "100" => STUDENT_ID <= "0001"; --d2
      WHEN "110" => STUDENT_ID <= "0001"; --d3
      WHEN "111" => STUDENT_ID <= "1000"; --d4
      WHEN "011" => STUDENT_ID <= "0101"; --d5
      WHEN "001" => STUDENT_ID <= "0010"; --d6

      WHEN OTHERS => STUDENT_ID <= "----";
      END CASE;
   END PROCESS;
Q <= Qreg;
END Behavior;
```

VHDL code for 7-segment display:

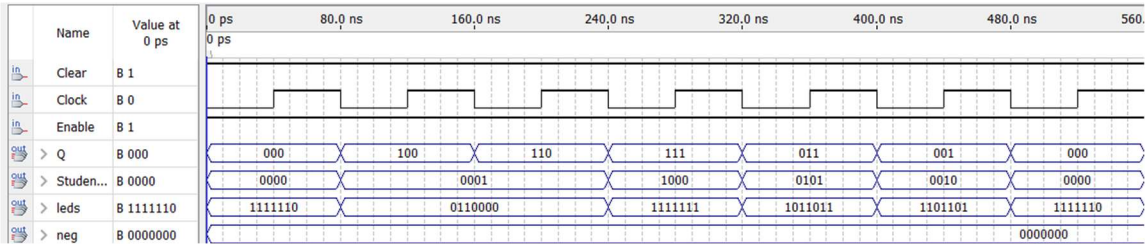
```
1   LIBRARY ieee ;
2   USE ieee.std_logic_1164.all ;
3
4   ENTITY sseg IS
5       PORT ( bcd : IN STD_LOGIC_VECTOR(3 DOWNTO 0) ;
6           neg : IN STD_LOGIC ;
7         leds : OUT STD_LOGIC_VECTOR(0 TO 6);
8         ledss: OUT STD_LOGIC_VECTOR(0 TO 6) ) ;
9   END sseg ;
10
11  ARCHITECTURE Behavior OF sseg IS
12  BEGIN
13      PROCESS ( bcd )
14      BEGIN
15          CASE bcd IS -- abcdefg
16              WHEN "0000" => leds <= "1111110";
17              WHEN "0001" => leds <= "0110000";
18              WHEN "0010" => leds <= "1101101";
19              WHEN "0011" => leds <= "1111001";
20              WHEN "0100" => leds <= "0110011";
21              WHEN "0101" => leds <= "1011011";
22              WHEN "0110" => leds <= "1011111";
23              WHEN "0111" => leds <= "1110000";
24              WHEN "1000" => leds <= "1111111";
25              WHEN "1001" => leds <= "1110011";
26
27              WHEN "1010"    => leds <= "1110111"; --a
28              WHEN "1011"    => leds <= "0011111"; --b
29              WHEN "1100"    => leds <= "1001110"; --c
30              WHEN "1101"    => leds <= "0111101"; --d
31              WHEN "1110"    => leds <= "1101111"; --e
32              WHEN "1111"    => leds <= "1000111"; --f
33
34          END CASE ;
35      END PROCESS ;
```

```
34          END CASE ;
35      END PROCESS ;
36
37  PROCESS (neg)
38      BEGIN
39      IF (neg = '1') THEN
40      ledss <= "0000001";
41
42      ELSE
43      ledss <= "0000000";
44
45      END IF;
46      END PROCESS;
47  END Behavior ;
```

Circuit connecting Johnson Counter with 7-segment display:



Waveform of the inputs and the outputs:



References

Brown, S. D., & Vranesic, Z. G. (2009). *Fundamentals of Digital Logic with VHDL Design*. New York, United States: McGraw-Hill Education.