RYERSON UNIVERSITY

Ryerson University

Department of Electrical & Computer Engineering

ELE 404

Amplifier Design Project

Introduction

The purpose of this project is to design, simulate, analyze, implement, and test a single-supply, multistage, inverting, transistor amplifier which fulfills a set of specifications.

For this project, **the pre-lab shall be treated as your formal design report and therefore must be much more detailed than usual** (please see **Evaluation** heading on the next page of this document). **The report shall be submitted to the TA by the deadline.** As with the previous labs, **the report is an individual assignment**.

Specifications

- Power supply: $+\mathbf{10}\boldsymbol{V}$ relative to the ground;
- Quiescent current drawn from the power supply: ***no larger than*** $\mathbf{10}\ \boldsymbol{mA}$**;**
- No-load voltage gain (at 1 kHz): $|\boldsymbol{A_{vo}}| = \mathbf{50}\ (\pm\ \mathbf{10}\%)$**;**
- Maximum no-load output voltage swing (at 1 kHz): ***no smaller than 8 V peak to peak;***
- Loaded voltage gain (at 1 kHz and with $R_L = 1\ k\Omega$): ***no smaller than*** $\mathbf{90}\%$ ***of the no-load voltage gain;***
- Maximum loaded output voltage swing (at 1 kHz and $R_L = 1\ k\Omega$): ***no smaller than 4 V peak to peak;***
- Input resistance (at 1 kHz): ***no smaller than*** $\mathbf{20}\ \boldsymbol{k\Omega}$;
- Amplifier type: ***inverting or non-inverting;***
- Frequency response: ***20 Hz to 50 kHz (*** $-\mathbf{3}\boldsymbol{dB}$ ***response);***
- Type of transistors: ***BJT;***
- Number of transistors (stages): ***no more than 3***;
- Resistances permitted: ***values smaller than*** $\mathbf{220}\ \boldsymbol{k\Omega}$ ***from the E24 series***;
- Capacitors permitted: $\mathbf{0.1}\ \boldsymbol{\mu F}$**,** $\mathbf{1.0}\ \boldsymbol{\mu F}$**,** $\mathbf{2.2}\ \boldsymbol{\mu F}$**,** $\mathbf{4.7}\ \boldsymbol{\mu F}$**,** $\mathbf{10}\ \boldsymbol{\mu F}$**,** $\mathbf{47}\ \boldsymbol{\mu F}$**,** $\mathbf{100}\ \boldsymbol{\mu F}$**,** $\mathbf{220}\ \boldsymbol{\mu F}$**;**
- Other components (BJTs, diodes, Zener diodes, etc.): ***only from your ELE404 lab kit.***

Notes:

- The output voltage must be free from distortions (clipping, etc.) in all test conditions.
- The source resistance, R_s, must be 600 Ω for all tests.

The designed amplifier must be AC-coupled for the load and the signal source, but the coupling between its intermediate stages may be of AC or DC type as per the designer's choice. There are no restrictions in terms of using NPN or PNP transistors.

Note that there is no right or wrong design, as long as the aforementioned specifications are met.

Report Content and Length

Including the cover page, the report is limited to 15 pages. In his/her report, the designer must:

1. Identify and justify the types of the constituting amplification stages, which when cascaded will meet the given design requirements (e.g., a CC stage followed by a CE stage, etc., and why…).
2. Present manual calculations for, and explain in sufficient details, his/her selection of the resistance and capacitance values.
3. Simulate the designed amplifier by Multisim (or any other circuit simulation software) and demonstrate that the design indeed meets the requirements and that its simulated performance is in a reasonable agreement with those predicted through manual calculations.

Evaluation (Read Carefully)

Your report shall be evaluated on the following:

1. Description of the circuit and its choice of configuration (e.g., a CC stage followed by a CE stage, etc., and why…)
2. Manual calculations for the resistance and capacitance values, bias voltages and currents, etc.
3. Detailed simulations of the design, using the circuit elements having come out of the manual calculations of item 2, clearly testing of the amplifier on its adherence to the design specifications (describe each test and provide all the corresponding waveforms).
4. Explanation of discrepancies, if any, between the simulation results and your manual calculation results, and provision of reasons for the discrepancies (to the best of your knowledge).
5. Organization and grammatical structure of the report.