Ryerson University Faculty of Science

**Department of Physics**

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| Course Number | *COE 328* |
| Course Title | *Digital Circuits* |
| Semester/Year | *Fall 2021* |
| Instructor | *Dr. Reza Sedaghat* |
| TA Name | *Sajjad Rostami Sani* |

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| Lab/Tutorial Report No. | *4* |

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| Report Title | *Lab 4* |

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| Section No. | *03* |
| Submission Date | *15-11-2021* |
| Due Date | *15-11-2021* |

| Student Name | Student ID | Signature* |
|---|---|---|
| Ahmad El-Gohary | 501011852 |  |

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## ***Objective***

The objective of this lab was to build a 4:1 multiplexer circuit using 3 2:1 multiplexer circuit and to build a 3:8 decoder circuit using 2 2:4 decoders.

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## ***Procedure***

Part 1:

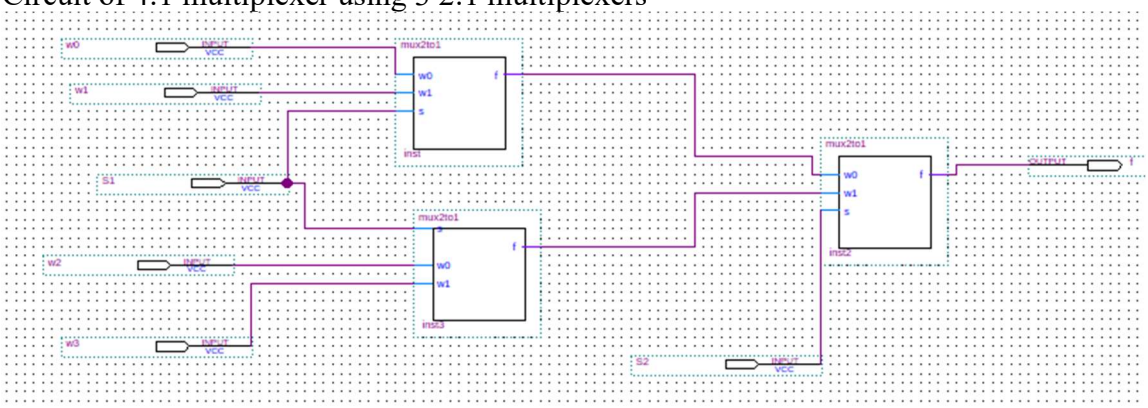
VHDL code for 2:1 multiplexer

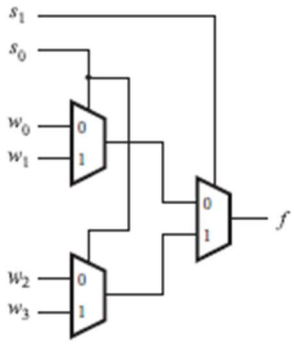
```
1   LIBRARY ieee ;
2   USE ieee.std_logic_1164.all ;
3   ENTITY mux2to1 IS
4   PORT ( w0, w1, s : IN STD_LOGIC ;
5         f : OUT STD_LOGIC ) ;
6   END mux2to1 ;
7   ARCHITECTURE Behavior OF mux2to1 IS
8   BEGIN
9   WITH s SELECT
10  f<= w0 WHEN '0',
11        w1 WHEN OTHERS;
12
13
14  END Behavior ;
```

VHDL code for 4:1

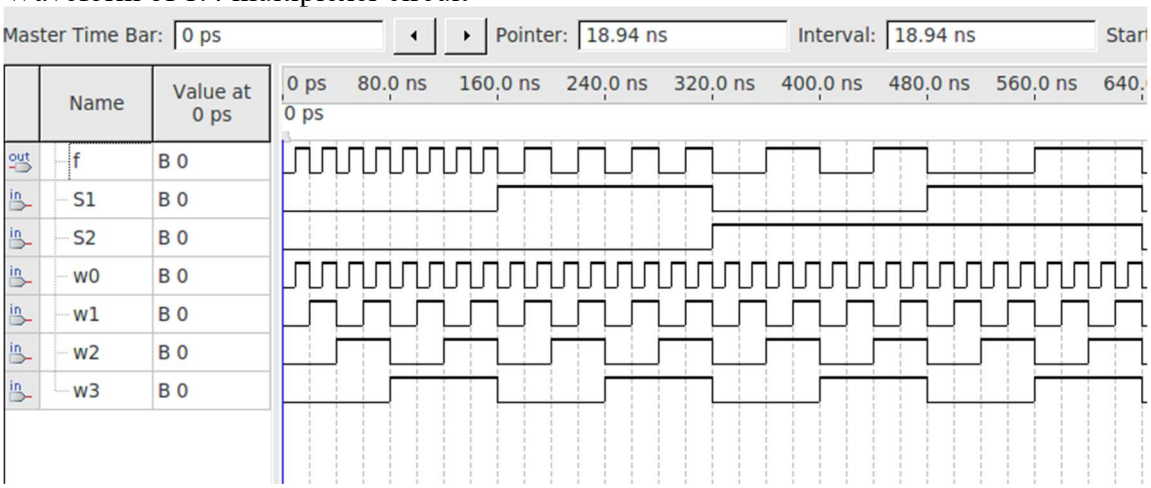
```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3
4   ENTITY mux4to1 IS
5   PORT (w0, w1, w2, w3 : IN STD_LOGIC;
6         s : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
7         f : OUT STD_LOGIC);
8   END mux4to1;
9
10  ARCHITECTURE Behavior OF mux4to1 IS
11  BEGIN
12  WITH s SELECT
13  f<= w0 WHEN "00",
14        w1 WHEN "01",
15        w2 WHEN "10",
16        w3 WHEN OTHERS;
17  END Behavior;
18
19  LIBRARY ieee;
20  USE ieee.std_logic_1164.all;
21  PACKAGE mux4to1_package IS
22  COMPONENT mux4to1
23  PORT (w0, w1, w2, w3 : IN STD_LOGIC;
24  s : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
25  f : OUT STD_LOGIC);
26  END COMPONENT;
27  END mux4to1_package;
```

Circuit of 4:1 multiplexer using 3 2:1 multiplexers




Waveform of 1:4 multiplexer circuit

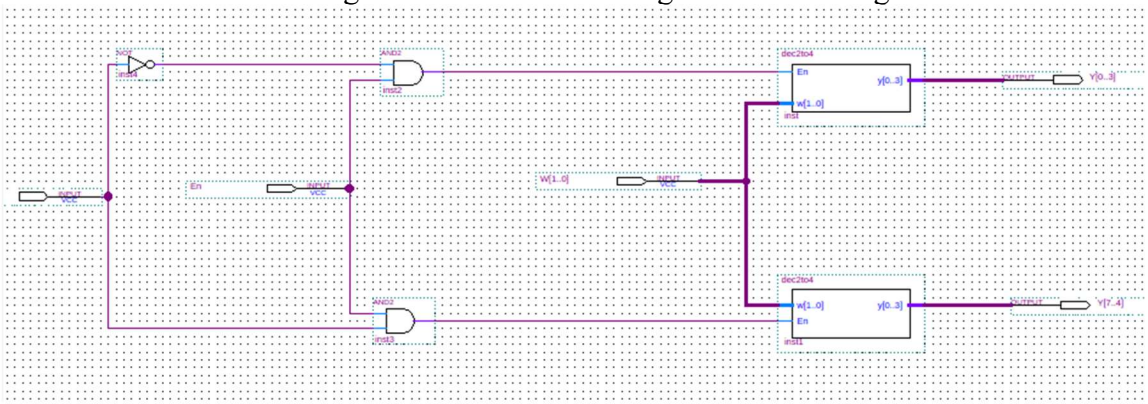


Part 2:

VHDL code for 2:4 decoder

```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3
4   ENTITY dec2to4 IS
5   PORT (w : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
6   En : IN STD_LOGIC;
7   y : OUT STD_LOGIC_VECTOR(0 TO 3));
8   END dec2to4;
9
10  ARCHITECTURE Behavior OF dec2to4 IS
11  SIGNAL Enw : STD_LOGIC_VECTOR(2 DOWNTO 0);
12  BEGIN
13  Enw <= En & w;
14  WITH Enw SELECT
15  y<= "1000" WHEN "100",
16  "0100" WHEN "101",
17  "0010" WHEN "110",
18  "0001" WHEN "111",
19  "0000" WHEN OTHERS;
20  END Behavior;
```

Circuit of 3:8 decoder using 2 2:4 decoders a NOT gate and 2 AND gates



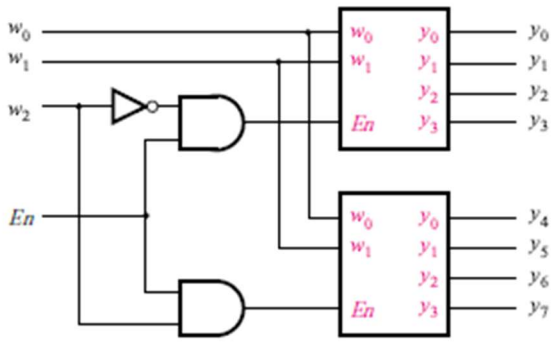
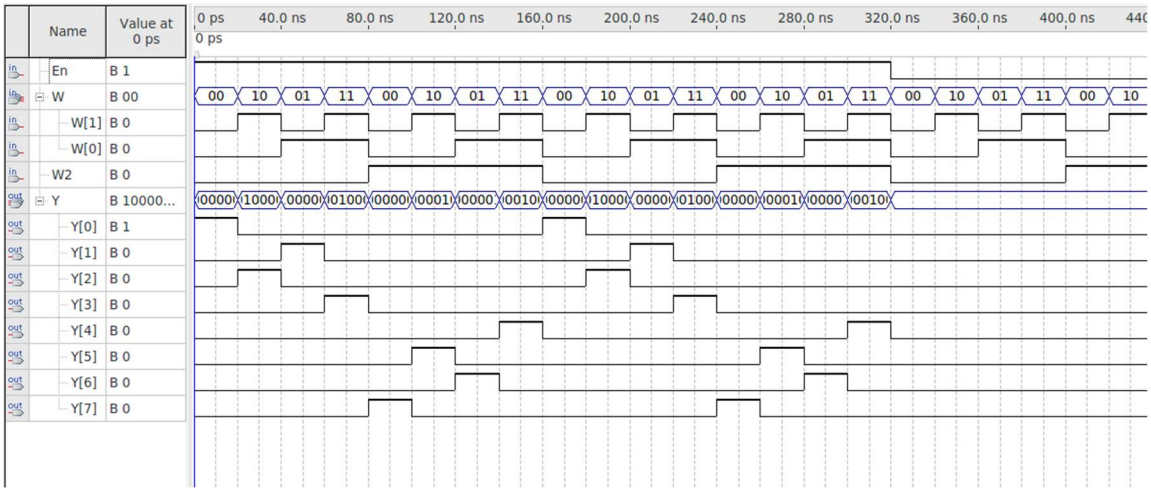



**Figure 6.17** A 3-to-8 decoder using two 2-to-4 decoders.

Waveform of 3:8 decoder circuit




## ***References***


Brown, S. D., & Vranesic, Z. G. (2009). *Fundamentals of Digital Logic with VHDL Design*. New York, United States: McGraw-Hill Education.