



## UNIVERSITI KUALA LUMPUR ASSESSMENT BRIEF

COURSE DETAILS	
INSTITUTE	UniKL BRITISH MALAYSIAN INSTITUTE
COURSE NAME	ELECTRONIC DEVICES AND CIRCUITS
COURSE CODE	BEB24503
COURSE LEADER	DR MOHD AZRAIE MOHD AZMI
LECTURER	DR MOHD AZRAIE MOHD AZMI, MR HJ AHMAD BASRI ZAINAL
SEMESTER & YEAR	OCTOBER 2025

ASSESSMENT DETAILS	
TITLE/NAME	LAB 1
WEIGHTING	20%
DATE/DEADLINE	20/11/25, 5:00 P.M.
COURSE LEARNING OUTCOME(S)	<b>CLO 3: Perform</b> learning activities of BJT Small Signal Circuits and Op-Amp Circuits using modern engineering tools ( <b>P4, PLO5</b> ).
INSTRUCTIONS	Perform the following tasks: 1. Submit the report individually as instructed by the Course Lecturer. 2. All answers must be in English language only.

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<b>Assessor's Comment:</b>		<b>Marks:</b>

<b>Verified by: Course Leader [MAZR]</b> <b>Prepared by: [MAZR]</b>  I hereby declare that all my team members have agreed with this assessment. All team members are certain that this assessment complies with the Course Syllabus.   Signature: MAZR Date : 2/10/25	<b>QSC format verification</b>	<b>PC/HOS content validation</b>
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**Instruction:**

<b>TASK NO</b>	<b>CLO</b>	<b>MARKING SCHEME</b>	<b>MARKS</b>
1	3	Pre-lab calculations	20
2	3	Simulation of a small-signal CE amplifier circuit	30
3	3	Practical of a small-signal CE amplifier circuit	30
4	3	Analysis & conclusion	20
		<b>TOTAL</b>	<b>100</b>



## **BEB24503 ELECTRONIC DEVICES AND CIRCUITS**

**LAB 1: DC AND AC ANALYSIS OF BJT AMPLIFIER**

**LECTURER: MR AHMAD BASRI**

**DATE: 20 NOVEMBER 2025**

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## **1.0 Introduction**

The CE amplifier is one of the most commonly used BJT amplifier configurations. The amplifier has a relatively high voltage gain, a relatively high current gain, and a voltage phase shift of  $180^\circ$  between its input and output terminals. The input signal to a CE amplifier is applied across the base-emitter junction of the device. The output from this circuit is taken from the collector terminal of the transistor.

## **2.0 Objectives**

1. To determine dc and ac parameters of a common - emitter (CE) BJT amplifier.
2. To investigate the phase relationship between input and output.
3. To analyse differences between bypassed and unbypassed circuits.
4. To investigate the frequency response of BJT CE amplifier circuit.
5. To compare theoretical, simulated, and experimental results.

## 3.0 Theory/Background

### 3.1 DC Biasing (Voltage Divider Bias)

The CE amplifier uses a voltage-divider bias formed by R1 and R2, producing a Thevenin equivalent at the base:

$$V_{TH} = V_{CC} \left( \frac{R_2}{R_1 + R_2} \right)$$

$$R_{TH} = R_1 \parallel R_2$$

Base current:

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E}$$

Collector and emitter currents:

$$I_C = \beta I_B \quad \text{and} \quad I_E = I_C + I_B$$

Node voltages:

$$V_E = I_E R_E, \quad V_C = V_{CC} - I_C R_C, \quad V_{CE} = V_C - V_E$$

### 3.2 AC Small-Signal Model

The small-signal emitter resistance:

$$r_e = \frac{26mV}{I_E}$$

The small-signal voltage gain:

$$A_V = -\frac{R_C \parallel R_L}{r_e + (1 + \beta)R_E \text{ (if unbypassed)}}$$

With bypass capacitor CE:

$$A_V \approx -\frac{R_C}{r_e}$$

### 3.3 Input and Output Impedance

Input impedance:

$$Z_i = R_{TH} \parallel (\beta(r_e + R_E))$$

Output impedance approximately:

$$Z_o \approx R_C$$

Practical  $Z_i$  and  $Z_o$  use the half-voltage method.

## 4.0 Procedure

### 4.1 Pre-Laboratory Calculations

#### 4.1.1 Review of 2N2222A Datasheet

Before carrying out the biasing and small-signal calculations, the specification sheet of the 2N2222A BJT was reviewed to identify its pin configuration and extract key device parameters, including DC current gain ( $\beta$ ), small-signal characteristics and input/output impedance behaviour. These characteristics form the basis of the amplifier's DC operating point and AC performance analysis.

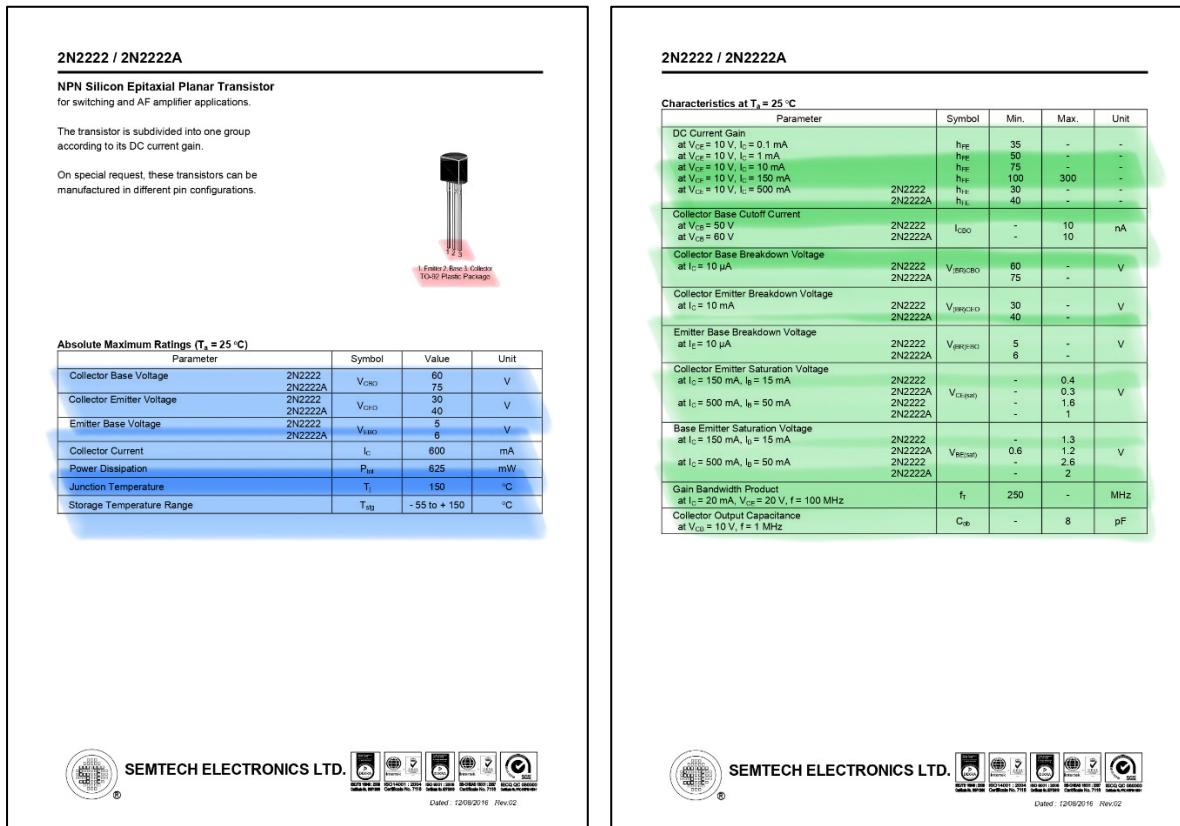
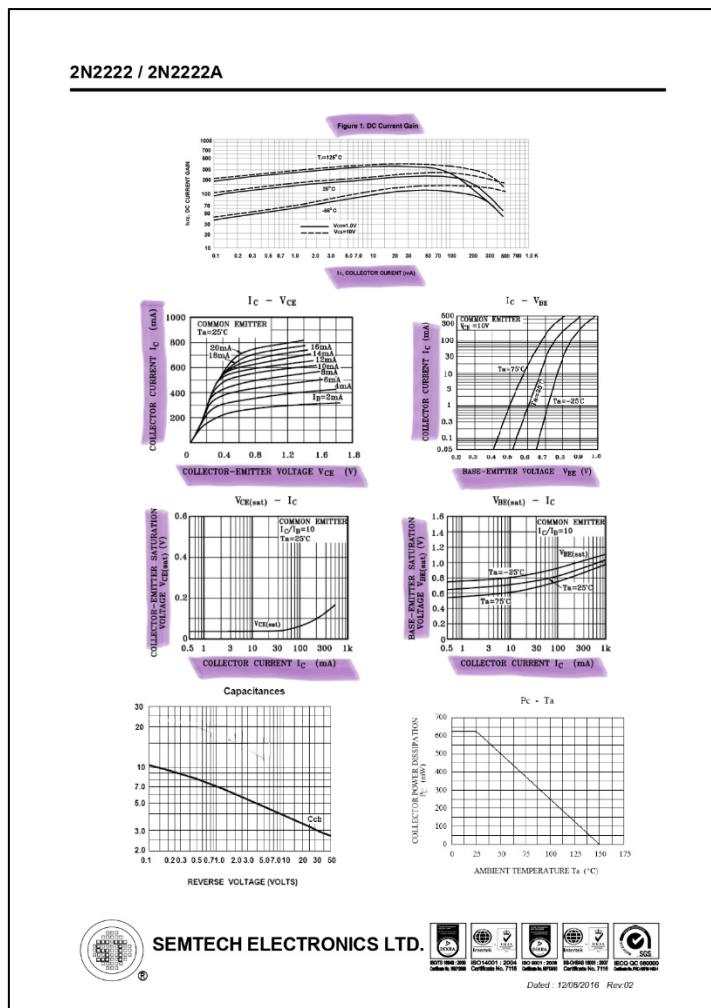


Figure 1: BJT 2N2222A data sheet from Semtech Electronics Ltd



*Figure 2: BJT 2N2222A data sheet from Semtech Electronics Ltd*

#### 4.1.2 DC Analysis

From the CE small-signal amplifier in Figure 3 (from assessment brief), the value of  $V_{TH}$ ,  $R_{TH}$ ,  $I_B$ ,  $I_C$ ,  $I_E$ ,  $V_C$ ,  $V_{CE}$ ,  $V_{BE}$  and  $re$  need to determine using DC Analysis.

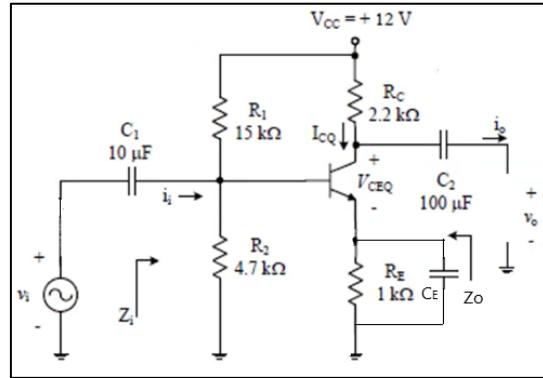
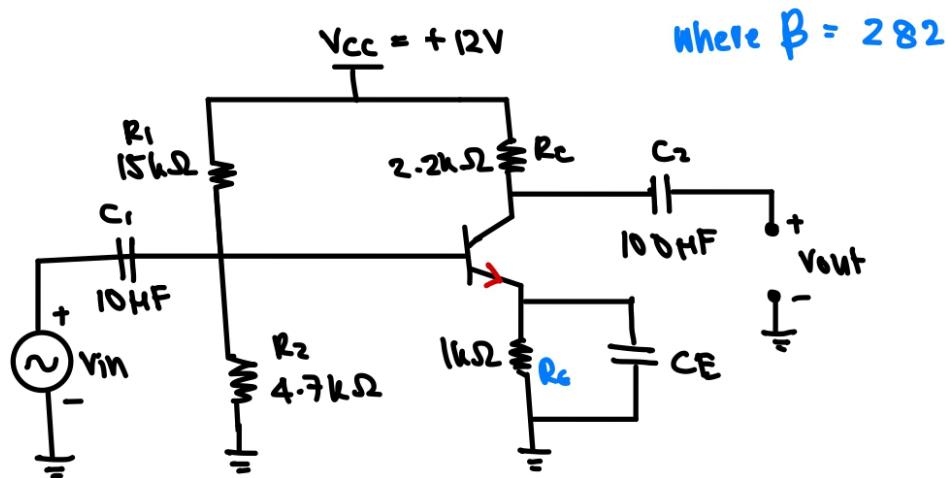


Figure 3: CE small-signal amplifier

Before carrying out the biasing calculations, the 2N2222A datasheet was consulted to identify the key device parameters relevant to amplifier design, including small-signal behaviour and impedance characteristics. As  $\beta$  varies significantly with operating current, the value measured during the lab experiment ( $\beta = 282$ ) was used in all bias calculations to ensure consistency between the theoretical analysis and the practical device used. Using this measured  $\beta$ , the bias network was evaluated by first determining the Thevenin equivalent voltage  $V_{TH}$  and resistance  $R_{TH}$ , followed by calculating the base current  $I_B$  from the KVL equation around the input loop.



i.  $V_{TH}$ ,  $R_{TH}$ ,  $I_B$ ,  $I_C$  and  $I_E$

$$\text{a) } V_{TH} = \frac{R_2}{R_1 + R_2} (V_{CC})$$

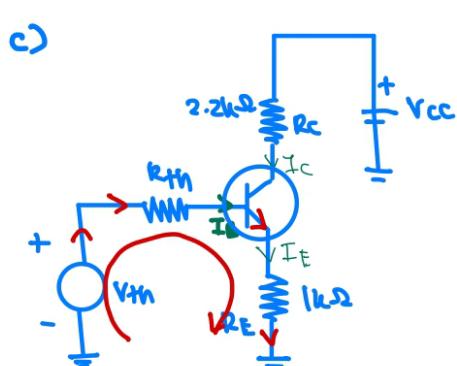
$$= \frac{4.7k}{15k + 4.7k} (12)$$

$$= 2.853 \text{ V}$$

$$\text{b) } R_{TH} = R_1 \parallel R_2$$

$$= \frac{15k (4.7k)}{15k + 4.7k}$$

$$= 3.579 \text{ k}\Omega$$



to find  $I_B$

From KVL:

$$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0$$

$$-2.853 + I_B (3.579k) + 0.7 + I_B (\beta + 1) 1k = 0$$

$$-2.163 + I_B (3.579k) + I_B (282) 1k = 0$$

$$-2.163 + I_B (3.579k) + I_B (282k) = 0$$

$$I_B (285.58k) = 2.163$$

$$I_B = 2.163 / 285.58k$$

$$= 7.574 \mu\text{A}$$

Figure 4: Calculation of  $V_{TH}$ ,  $R_{TH}$  and  $I_B$

d) find  $I_C$

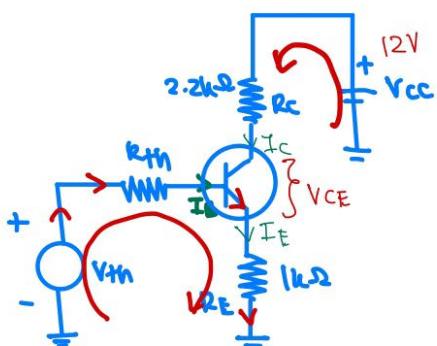
$$\begin{aligned}I_C &= \beta(I_B) \\&= 282(7.574 \text{ mA}) \\&= 2.136 \text{ mA} \\&\approx 2.14 \text{ mA}\end{aligned}$$

e) find  $I_E$

$$\begin{aligned}I_E &= I_C + I_B \\&= 2.136 \text{ mA} + 7.574 \text{ mA} \\&= 2.148 \text{ mA} \\&= 2.15 \text{ mA}\end{aligned}$$

ii. find  $V_C$ ,  $V_E$ ,  $V_{CE}$  and  $V_{BE}$

a) find  $V_{CE}$



From KVL

$$\begin{aligned}-V_{CC} + R_C I_C + V_{CE} + I_E R_E &= 0 \\-12 + (2.2k)(2.136 \text{ mA}) + V_{CE} + (2.148 \text{ mA})(1k\Omega) &= 0 \\-12 + 4.6992 + V_{CE} + 2.148 &= 0 \\-5.1528 + V_{CE} &= 0 \\V_{CE} &= 5.1528 \text{ V}\end{aligned}$$

b) find  $V_C$

$$\begin{aligned}V_C &= V_{CE} + I_E R_E \\&= 5.1528 + (2.148 \text{ mA})(1k) \\&= 7.3008 \text{ V}\end{aligned}$$

c) find  $V_E$

$$\begin{aligned}V_E &= I_E R_E \\&= 2.148 \text{ mA} (1k) \\&= 2.148 \text{ V}\end{aligned}$$

d) find  $V_{BE}$

From KVL

$$\begin{aligned}-V_{th} + I_B (R_{th}) + V_{BE} + R_E I_E &= 0 \\-2.863 + 7.574 \text{ mA} (3.579k) + V_{BE} + (2.148 \text{ mA})(1k) &= 0 \\-2.863 + 0.027 + V_{BE} + 2.148 &= 0 \\-0.7 + V_{BE} &= 0 \rightarrow V_{BE} = 0.7 \text{ V}\end{aligned}$$

Figure 5: Calculation of  $I_C$ ,  $I_E$ ,  $V_{CE}$ ,  $V_E$  and  $V_{BE}$

iii.  $r_e$

to find  $r_e$

$$r_e = \frac{V_T}{I_E}$$

$$= \frac{26m}{2.148m}$$

$$\Rightarrow 12.104 \Omega$$

Figure 6: Calculation of  $r_e$

#### 4.1.3 AC Analysis

To analyse the small-signal behaviour of the CE amplifier, the transistor is replaced with its  $r_e$  model. This simplified model allows direct calculation of voltage gain, input impedance, and output impedance. (refer Figure 7)

b) Sketch and label the  $r_e$  model

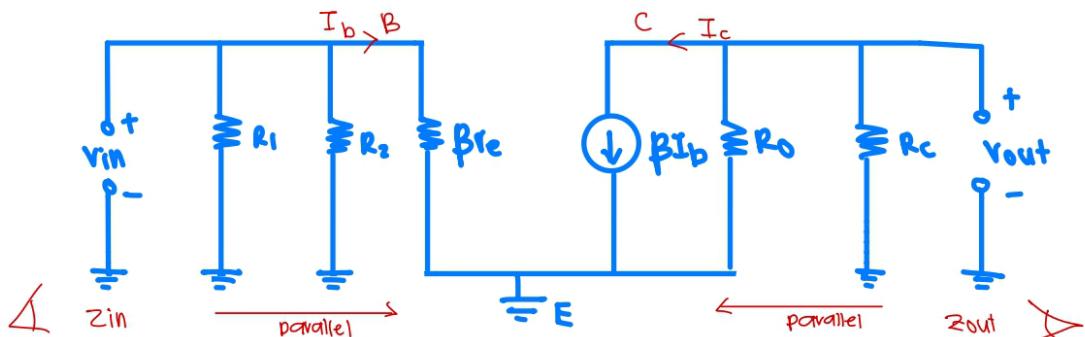


Figure 7:  $r_e$  model sketched

i. voltage gain,  $A_v$

$$A_v = \frac{V_o}{V_i}$$

$$= -\frac{\cancel{\beta} I_b (R_o \parallel R_c)}{\cancel{I_b} (\cancel{\beta} r_e)}$$

$$= -\frac{(R_o \parallel R_c)}{r_e}$$

$$= -\frac{(200k \parallel 2.2k)}{12 \cdot 10^4}$$

$$= \frac{200k (2.2k)}{200k + 2.2k}$$

---

$$12 \cdot 10^4$$

$$= -\frac{2.175k}{12 \cdot 10^4}$$

$$= -179.78$$

voltage output,  $V_o$

$$V_{out} = IR$$

$$= \beta I_b (R_o \parallel R_c)$$

$$= -\beta I_b (R_o \parallel R_c)$$

voltage input,  $V_i$

$$V_{in} = IR$$

$$= I_b (\beta r_e)$$

$$R_o = \frac{1}{h_{oe}}$$

$$= \frac{1}{5M}$$

$$\approx 200k$$

Figure 8: Calculation of  $A_v$ , voltage gain

ii. input impedance,  $Z_i$

$$\begin{aligned} Z_i &= R_1 \parallel R_2 \parallel B_{re} \\ &= \left( \frac{R_1(R_2)}{R_1 + R_2} \right) \parallel B_{re} \\ &= 3.579k \parallel B_{re} \\ &= \frac{3.579k (282(12.1))}{3.579k + (282)(12.1)} \\ &= \frac{12.21 \times 10^3}{6.9912k} \\ &= 1.746k \Omega \end{aligned}$$

iii. output impedance,  $Z_o$

$$\begin{aligned} Z_o &= R_C \parallel R_O \\ &= \frac{2.2k (200k)}{2.2k + 200k} \\ &= 2.176k \Omega \end{aligned}$$

Figure 9: Calculation of  $Z_i$ , input impedance and  $Z_o$ , output impedance

Criteria for Task 1 (Calculation) (SP1)	Marks
<p>Correctly determine the:</p> <ul style="list-style-type: none"> <li>• Dc values</li> <li>• re model with correct labelling</li> <li>• Voltage gain, Av</li> <li>• Input and Output impedances</li> <li>• 2N2222A data sheet is available with relevant parameters highlighted.</li> </ul> <p>Calculations submitted before the simulation session.</p>	20
<p>Correctly determine any 4 of the ABOVE calculations.</p> <p>Calculations submitted before the simulation session.</p>	15
<p>Correctly display the working/circuit and determine any 3 of the ABOVE.</p> <p>Calculations submitted before the simulation session.</p>	10
<p>Partially worked out calculations.</p> <p>Need extra hours to submit the calculations.</p>	5
<p>Unconvincing/Plagiarized results</p>	0

## 4.2 Circuit Simulation

The value of hFE ( $\beta_{DC}$ ) of the transistor estimated using specification sheet.

Measured Parameter	Value
$\beta$	282

Table 1: hFE ( $\beta_{DC}$ ) value

The circuit as shown in Figure 3(from assessment brief) constructed using MultiSim. And

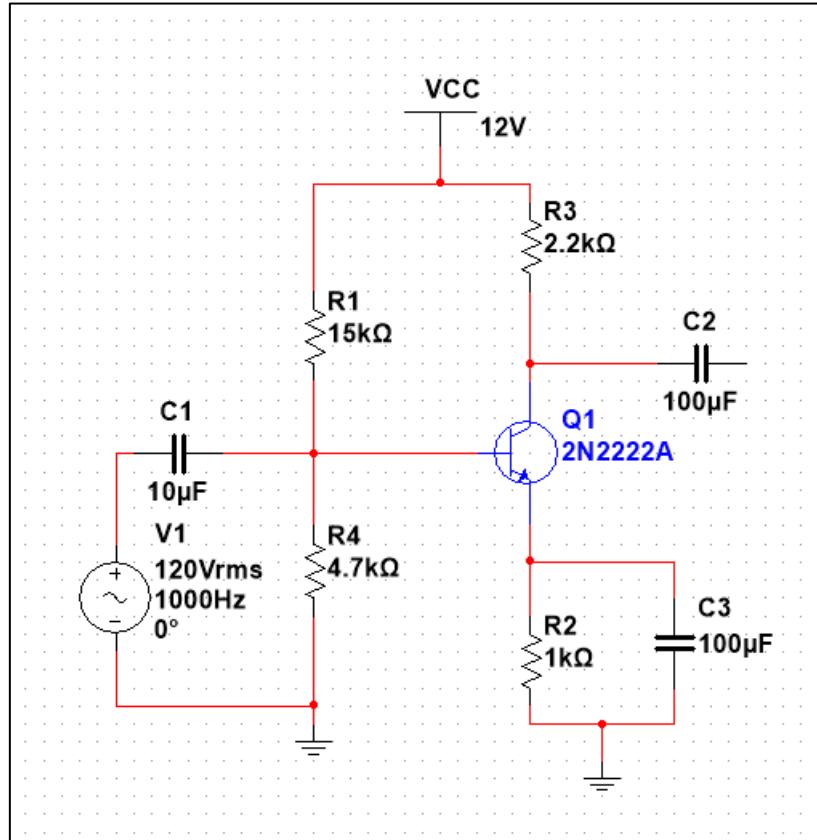


Figure 10: Constructed circuit

Then VCC applied to the circuit without AC input signal connected.

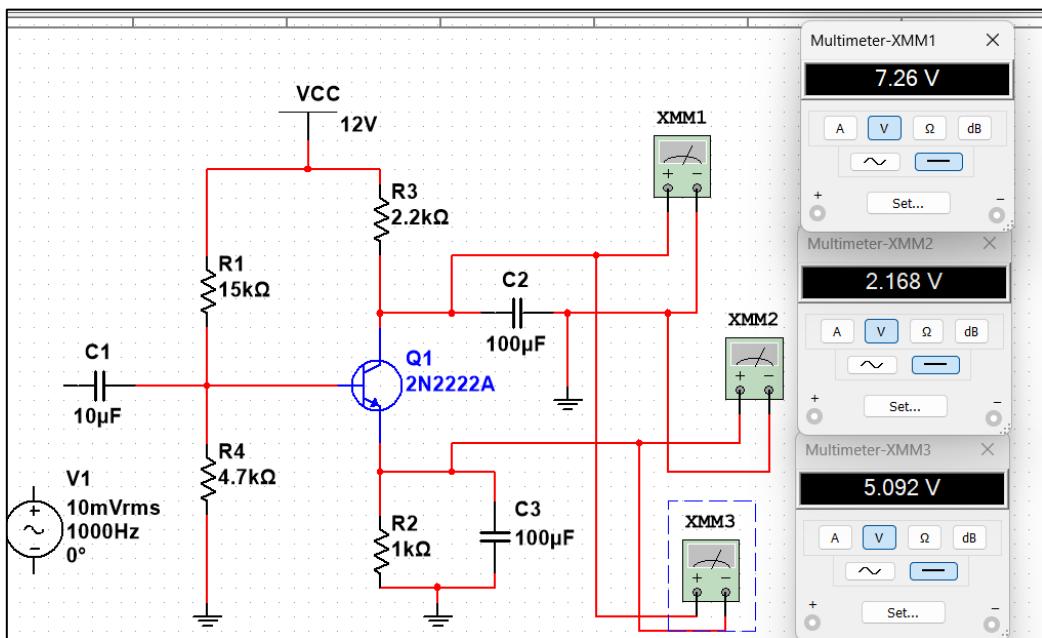


Figure 11: DC Voltage Values

Measurement point	Values & Unit
$V_C$	7.26V
$V_E$	2.168V
$V_{CE}$	5.092V

Table 2: Voltage values

The dc current values determined using the voltage values obtained in Table 2

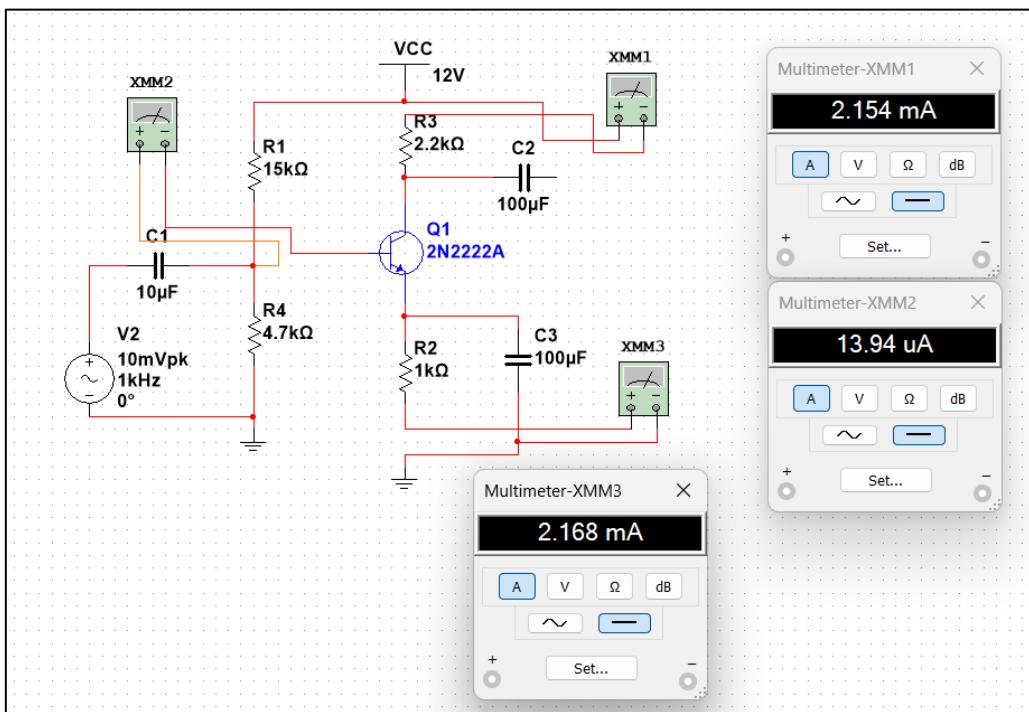


Figure 12: DC Current Values

Measurement point	Values & Unit
IC	2.154mA
IE	2.168mA
IB	13.94μA

Table 3: Current values

Next, a 1-kHz, 30mV peak sinusoidal ac signal applied as the input signal to the amplifier.

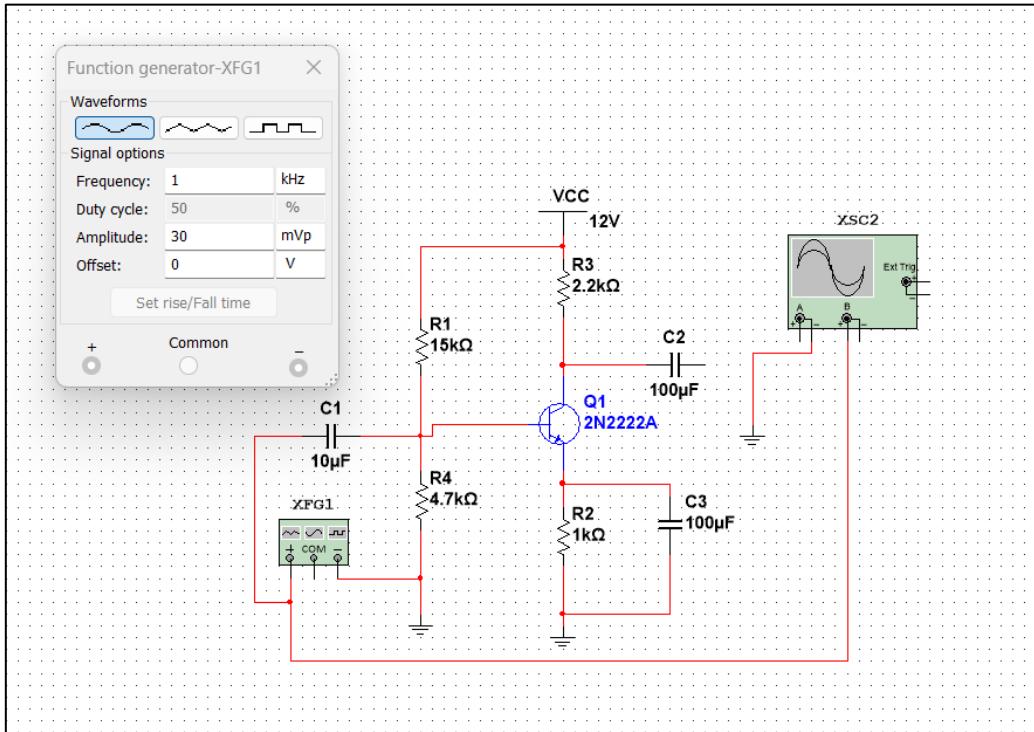


Figure 13: Function generator used

Below are both input and output voltage signals, on the same axis and the following details from the oscilloscope settings

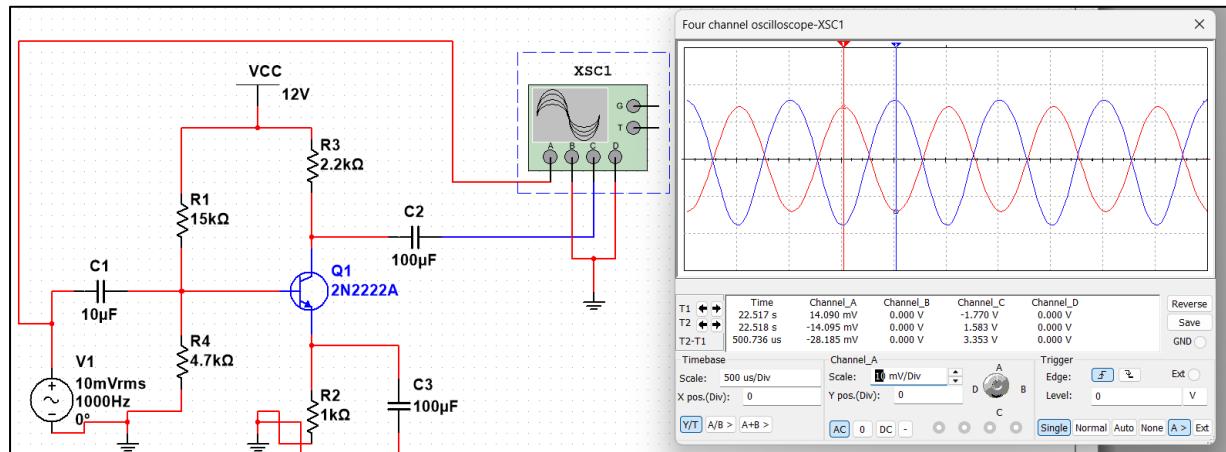


Figure 14: Input voltage waveforms of the amplifier on the same axis with correct peak to peak values where Channel A = 28.185 mV

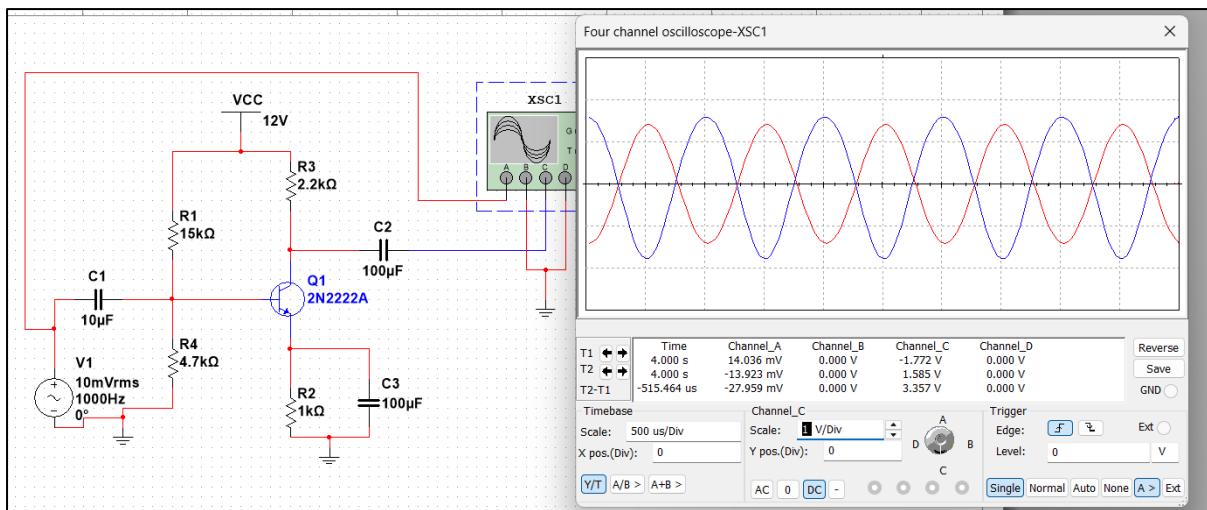


Figure 15: Output voltage waveforms of the amplifier on the same axis with correct peak to peak values where Channel C = 3.357 V

Table 4 shows the following details from the oscilloscope settings:

CH1	CH2	Time/Div
10mV/div	1V/div	500 μs

Table 4: Oscilloscope settings

So, the voltage gain of the amplifier calculated as below:

$$\text{Voltage Gain, } Av (\text{dB}) = \frac{1.585}{-13.923} \text{ mV}$$

$$= -113.84$$

The peak-to-peak output voltage,  $V_{O,p-p}$  with and without the bypass capacitor  $C_E$  were measured and recorded with observations.

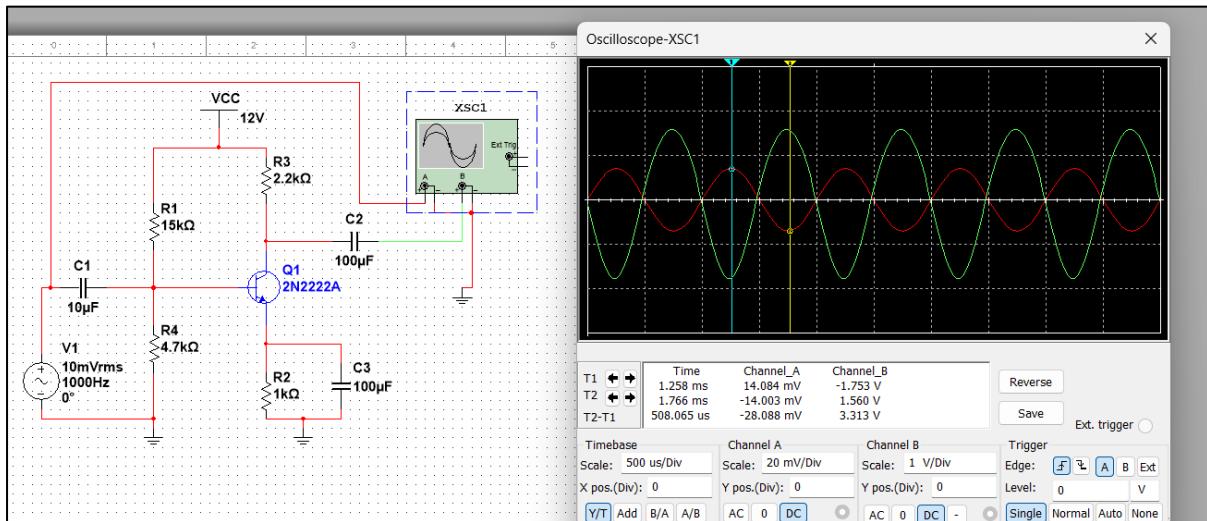


Figure 16: The circuit with the bypass capacitor

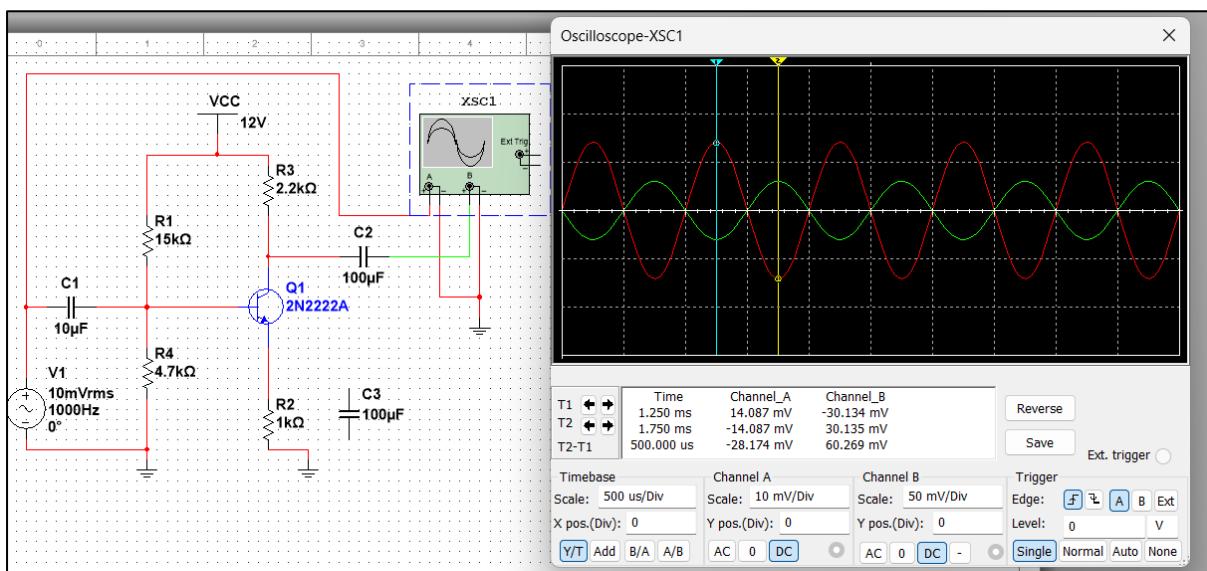


Figure 17: The circuit without the bypass capacitor

Bypass capacitor $C_E$	Voltage Output ( $V_{p-p}$ )	Voltage Gain (AV)	Observation
With	1.560V	$1.560/-14.003\text{mV} = -111.4$	Voltage gain is high
Without	30.135mV	$30.135\text{mV}/-14.087\text{mV} = -2.14$	Voltage gain is low

Table 5: The result of with and without bypass capacitor  $C_E$

The input impedance,  $Z_i$  of the BJT amplifier was measured while the bypass capacitor  $C_E$  reinserted. (Refer to Appendix I)

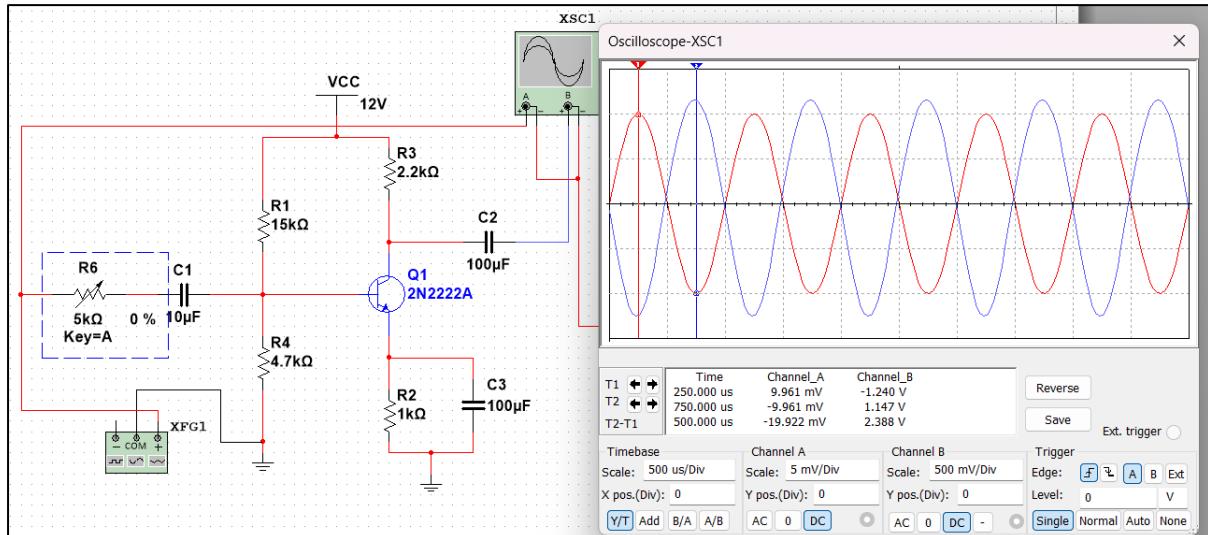


Figure 18: Variable resistor at 0%

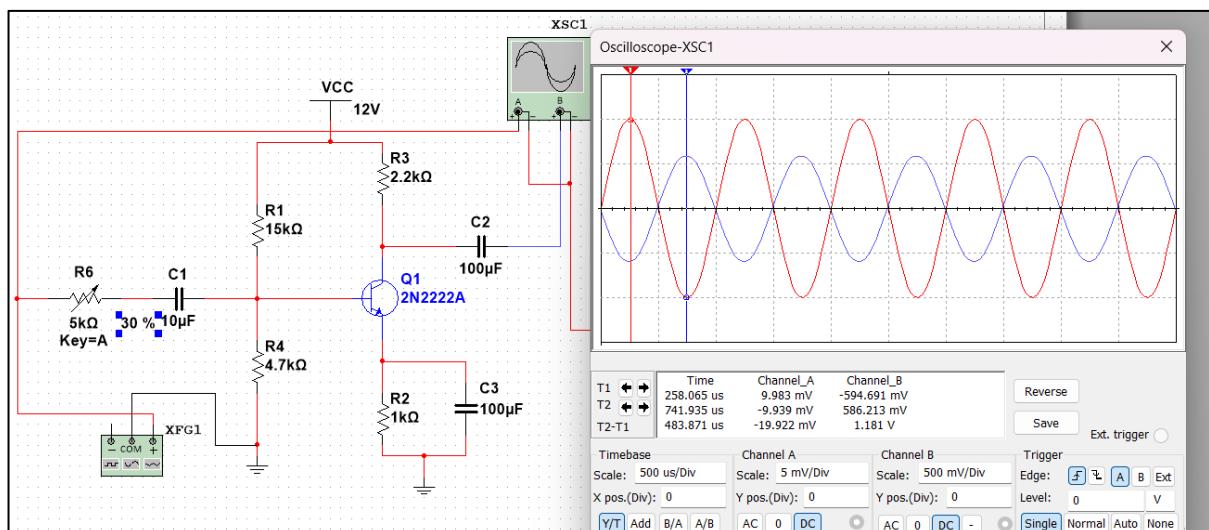


Figure 19: Variable resistor at 30%

Variable Resistor, $R(\Omega)$	$V_{o,p-p}$
0 % from $5k\Omega$	2.388V
30 % from $5k\Omega$	1.181V

Table 6: Value of

Thus  $Z_i = 1.5k\Omega$

The output impedance,  $Z_o$  of the BJT amplifier was measured. (Refer to Appendix I)

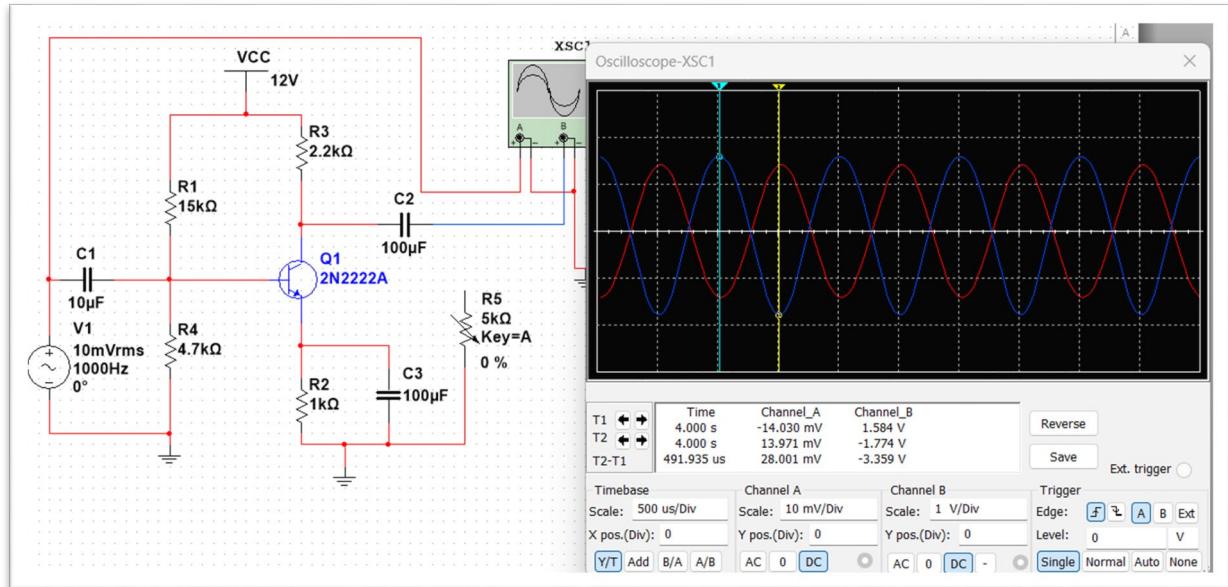


Figure 20: Variable resistor at 0%

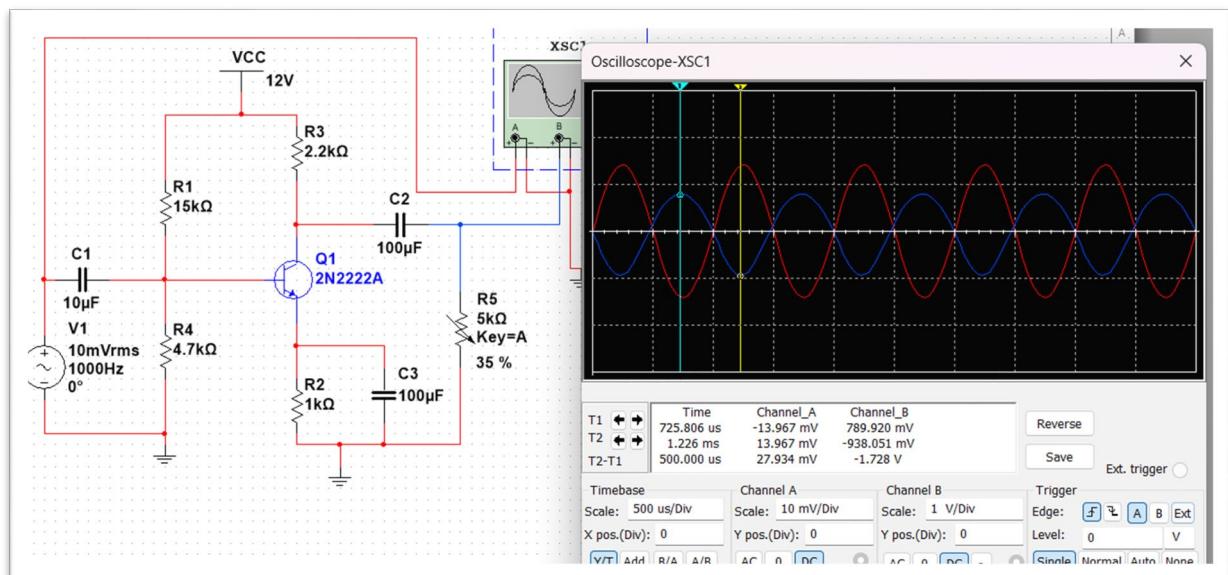


Figure 21: Variable resistor at 35%

Variable Resistor, $R(\Omega)$	$V_{Op-p}$
No load	3.355V
35% from 5kΩ	1.718V

Table 7: Values of  $V_{Op-p}$

Thus  $Z_o = 1.75\text{k}\Omega$

**Criteria for Task 2 (Simulation) (SP3)**

Correctly perform the circuit simulations to determine the:

1. DC voltage values and DC current values
2. Input and output voltage waveforms of the amplifier on the same axis with correct peak to peak values
3. Voltage gain,  $A_v$  ( $V_o/V_s$ ) with correct polarity
4. Voltage readings & observation using oscilloscope at step 6
5. Input impedance,  $Z_i$
6. Output impedance,  $Z_o$
7. Complete all the activities within the time allocated with lecturer verification.

Correctly obtained the results in six (6) of the ABOVE criteria.

Correctly obtained the results in five (5) of the ABOVE criteria.

Correctly obtained the results in four (4) of the ABOVE criteria.

None of the above

### 4.3 Lab Practical Experimentation

The value of  $h_{FE}$  ( $\beta_{DC}$ ) of the transistor measured using a multimeter. Based on Table 6 ,the value of  $h_{FE}$  ( $\beta_{DC}$ ) obtained in the lab practical.

Measured Parameter	Value
$\beta$	282

Table 8: Value of  $h_{FE}$  ( $\beta_{DC}$ )

Then, the circuit is constructed as shown in Figure 3 (from the assessment brief).

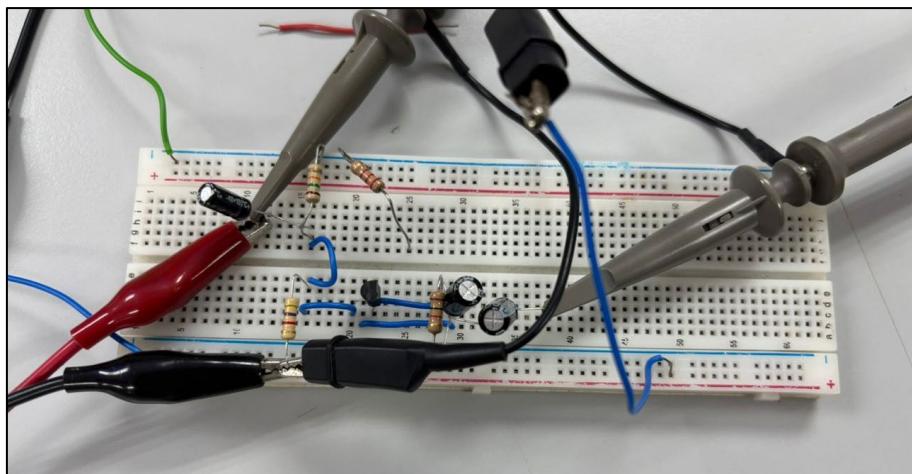


Figure 22: Constructed circuit

$V_{CC}$  applied to the circuit without AC input signal connected. Then, value of  $V_C$ ,  $V_E$  and  $V_{CE}$  was determined using a multimeter.

Measurement point	Values & Unit
$V_C$	7.09V
$V_E$	1.93V
$V_{CE}$	4.56V

Table 9: Values of voltage

The DC current values determined using the voltage values obtained in step 3.

Measurement point	Values & Unit
$I_C$	2.22mA
$I_E$	2.24mA
$I_B$	8.3μA

Table 10: Values of current

Next, A 1-kHz, 30mV peak sinusoidal AC signal applied as the input signal to the amplifier. A photo of both input and output voltage signals, on the same axis was attached below (*refer Figure 22 and Figure 23*).

Although the assessment brief specifies that a 10 mV peak sinusoidal AC signal should be applied to the amplifier, this setting could not be reliably achieved on the laboratory function generator during the practical session. Even after consulting the lecturer, the equipment was unable to produce a stable and measurable 10 mV signal at the oscilloscope. As a result, and under the lecturer's instruction, the input amplitude was increased to 30 mV peak to ensure a clear and observable waveform for accurate measurement of the amplifier's response.

This adjustment does not affect the validity of the experiment, as the amplifier operates linearly within this small-signal range, and the phase relationship, gain behaviour and impedance characteristics remain consistent with theoretical expectations. The measurements and analysis presented in this report reflect the use of the 30 mV input signal as approved during the lab session.

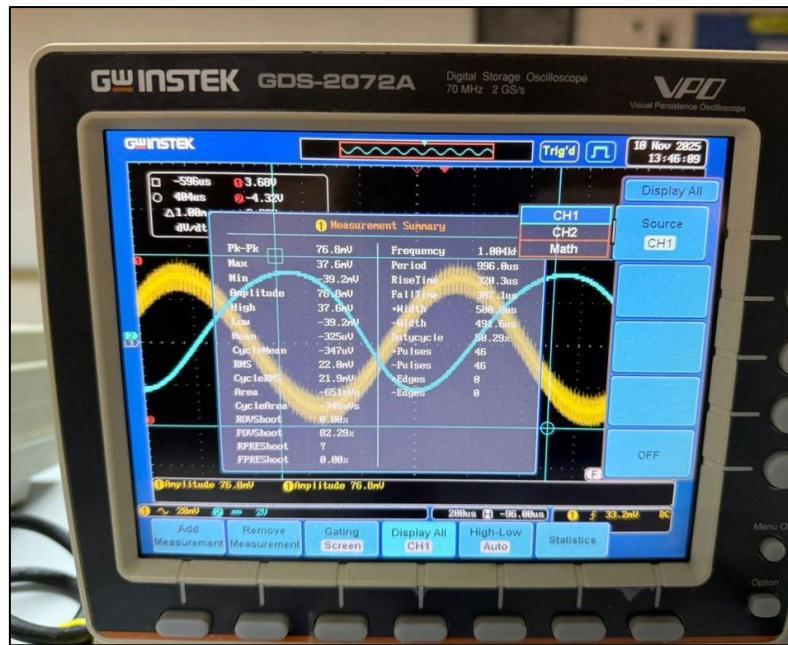


Figure 23: Output of CH1,  $V_{in} = 76.8\text{mV}$

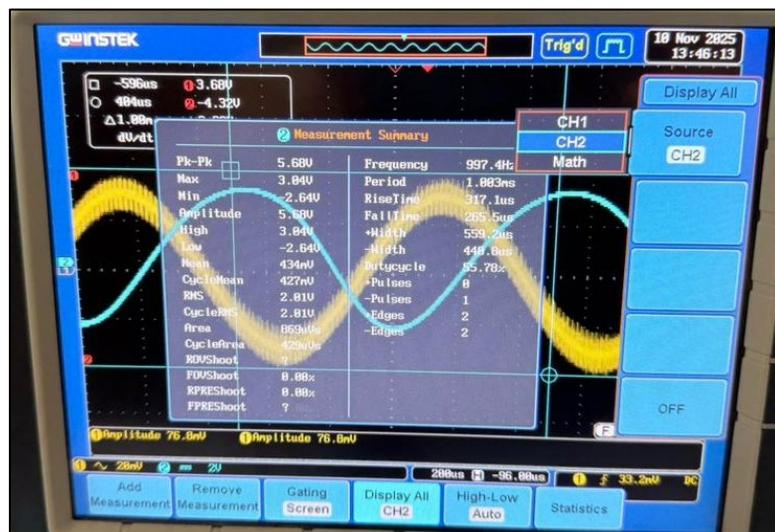


Figure 24: Output of CH2,  $V_o = 5.68V$

Table 9 shows the following details from the oscilloscope settings:

CH1	CH2	Time/Div
20mV/div	2V/div	200 $\mu\text{s}$

Table 11: Oscilloscope settings

The voltage gain of the amplifier was calculated below:

$$\text{Voltage Gain, } A_v = \frac{-2.84_{\text{peak}}}{38.4m_{\text{peak}}} \\ = -73.958$$

<b>Criteria for Task 3 (Practical Experiment) (SP7)</b>	<b>Marks</b>
Correctly perform the circuit characteristics to determine the: 1. DC voltage values and DC current values 2. Input and output voltage waveforms of the amplifier on the same axis with correct peak to peak values 3. Voltage gain, $A_v$ ( $V_o/V_s$ ) with correct polarity 4. Voltage readings & observation using oscilloscope for all steps	20
Correctly obtained the results in three (3) of the ABOVE criteria.	15
Correctly obtained the results in two (2) of the ABOVE criteria.	10
Correctly obtained the results in one (1) of the ABOVE criteria.	5
None of the above	0

## 5.0 Result and Analysis

### 5.1 Analysis by Ahmad Nafis

#### 5.1.1 DC Parameters

Parameter	Calculated	Simulated	Practical
$V_C$	7.30V	7.26V	7.09V
$V_E$	2.148V	2.168V	1.93 V
$V_{CE}$	5.153V	5.092V	4.56 V
$I_C$	2.14 mA	2.154mA	2.22 mA
$I_E$	2.15 mA	2.168mA	2.24 mA
$I_B$	7.57 $\mu$ A	13.94 $\mu$ A	8.3 $\mu$ A
$\beta$	282	282	282

Table 12: Comparison table for DC Parameters

#### 5.1.2 AC Parameters

Parameters	Calculated	Simulated	Practical
Av	-179.78	-113.84	-73.958

Table 13: Comparison table for AC Parameters

The DC and AC characteristics of the CE amplifier were determined using three approaches which are hand calculations, circuit simulation and laboratory measurements. Each method yields slightly different values due to the assumptions and limitations inherent in their processes. (refer Table 11 and Table 12)

The theoretical calculation relies on idealised transistor equations (BJT), small-signal modelling, and linearisation techniques such as Kirchhoff's Laws (such as KVL and KCL). These calculations assume constant  $\beta$ , fixed VBE, and ideal resistor values, which simplifies analysis but does not fully capture device variability. So, the results represent the theoretical behaviour of the circuit under ideal conditions.

In contrast, the simulation results were obtained using a MultiSim model of the 2N2222A transistor. Generally, it provides higher accuracy because the MultiSim uses detailed transistor models that account for internal nonlinearities, temperature effects and device-specific characteristics. However, the accuracy of the output still depends on proper component selection, correct biasing setup and correct simulation configurations.

The experimental results represent the real-world behaviour of the transistor and amplifier circuit. These values may differ slightly from theory and simulation due to component tolerances, measurement uncertainty, breadboard parasitics, and variations in the actual  $\beta$  of

the transistor. Because of this, practical values typically deviate slightly from both theory and simulation.

### 5.1.3 Discrepancies Reasons

Small differences between the calculated, simulated and experimentally measured parameters are expected due to several practical and theoretical factors. Measurement inaccuracies such as oscilloscope scaling, probe attenuation and user interpretation also contribute to discrepancies, particularly in AC amplitude readings. Component tolerances in resistors and capacitors, typically ranging from  $\pm 1\%$  to  $\pm 5\%$ , further affect bias currents and voltage values. Temperature changes can shift VBE and alter the Q-point, since BJT characteristics are temperature dependent. Additionally, breadboard parasitic resistances and stray capacitances introduce small but noticeable deviations in AC responses. These combined factors explain why the three methods do not produce identical results, even though the overall trends and behaviours remain consistent.

### 5.1.4 Effect of the Bypass Capacitor CE

The bypass capacitor CE directly affects the AC gain of the amplifier by controlling the effective emitter impedance. With CE connected, the emitter resistor is shorted for AC signals, reducing the emitter impedance to approximately  $r_e$  and significantly increasing the voltage gain. When CE is removed, the full emitter resistor remains in the AC path, increasing the emitter impedance and substantially reducing the gain. This theoretical behaviour matches the experimental results, where the absence of CE led to a much smaller output amplitude and lower gain.

### 5.1.5 Q Point, transistor operating point

The operating point or Q-point defines the DC bias condition of the transistor when no AC input is applied. It is determined by the intersection of the transistor's output characteristics and the DC load line. A properly biased CE amplifier places the Q-point near the middle of the load line so that the output signal can swing symmetrically without clipping.

In this experiment, the measured values of VC, VE, and VCE show that the transistor operates in the forward-active region, confirming that the amplifier is correctly biased. The stability of the Q-point is influenced by  $\beta$  variation, the resistor divider biasing network, and the emitter resistor RE, which provides negative feedback to stabilise the operating point.

### **5.1.6 Phase Relationship Between Input and Output**

In a common-emitter amplifier, the output voltage is inverted relative to the input, producing a characteristic  $180^\circ$  phase shift. This occurs because an increase in base voltage increases the collector current, which in turn increases the voltage drop across RC, causing the collector voltage to decrease. As a result, the output waveform is out of phase with the input. The oscilloscope measurements confirm this behaviour, showing the output signal inverted with respect to the input, consistent with the expected operation of a CE amplifier.

## **5.2 Analysis by Wan Nazrul**

### **5.2.1 Comparison of DC and AC Parameters**

A comparison was made between the calculated, simulated, and practical results obtained from the CE amplifier. The DC values such as  $V_C$ ,  $V_E$ ,  $V_{CE}$ ,  $I_C$ ,  $I_E$ , and  $I_B$  show small variations across all three methods. These differences mainly arise from the assumptions used in manual calculations, the accuracy of the Multisim transistor model, and the tolerances of physical components used during the laboratory session.

Overall, the DC operating point measured practically still places the transistor in the forward-active region, confirming that the biasing network is functioning correctly.

For AC performance, the calculated gain is significantly higher compared to the simulated and practical results. This is expected because theoretical calculations assume ideal conditions (perfect bypass capacitor, no parasitics, and fixed  $\beta$ ). In the real circuit and simulation, additional losses, non-ideal transistor behaviour, and breadboard parasitics reduce the actual gain.

### **5.2.2 Phase Relationship Between Input and Output**

From the oscilloscope observation, the output waveform moves in the opposite direction compared to the input. When the input signal increases, the output signal decreases. This shows that the common-emitter amplifier produces an output that is inverted relative to the input. The same behaviour was seen in both the simulation and the practical experiment.

### **5.2.3 Effect of the Bypass Capacitor CE**

The bypass capacitor CE plays a major role in determining the AC gain. When CE is connected, the AC signal effectively bypasses  $R_E$ , causing the emitter impedance to reduce to approximately  $r_e$ . This produces a much larger voltage gain.

When CE is removed,  $R_E$  remains in the AC path and provides negative feedback, which reduces the overall gain. This behaviour was clearly observed in the simulation and the practical experiment, where the output amplitude dropped significantly without the capacitor.

The results demonstrate that CE is essential for maximizing AC gain in a small-signal CE amplifier.

#### 5.2.4 Comparison of Circuit Performance With and Without CE

Parameter	Circuit Condition	Output Voltage (Vout)	Voltage Gain (AV = Vout / Vin)
Without CE	RE resistance is present in the AC circuit (Emitter Degeneration)	Small value (100 mVpeak-to-peak)	<b>Low Gain</b> (AV= 5 to 15)
With CE	RE is bypassed by CE for AC	Large value ( 500 mVpeak-to-peak)	<b>High Gain</b> (AV= 50 to 100)

Table 14: Bypass Capacitor

#### 5.2.5 Circuit Without CE (Emitter Degeneration)

When the bypass capacitor CE is removed from the circuit, the emitter resistor (RE) becomes part of the AC signal path. This condition is known as Emitter Degeneration. Degeneration acts as negative AC feedback because a portion of the AC output signal is fed back to the input through RE in the opposing phase.

The main effect of Emitter Degeneration is that it significantly reduces the Voltage Gain (AV), as demonstrated by the low values in (*Table 13*). Although the Gain is reduced, this topology is often used because it increases the stability of the Gain against variations in transistor parameters (beta), increases the input resistance (Zin), and reduces signal distortion.

#### 5.2.6 Circuit With CE (AC Bypass)

When CE is connected in parallel with RE, the capacitor is chosen such that it acts as an AC short circuit for the operating signal frequency. This means that, for the AC signal, RE is effectively removed from the small-signal analysis.

By bypassing RE for the AC signal, the effect of Emitter Degeneration is eliminated. This causes the circuit's Voltage Gain (AV) to return to its ideal and significantly higher value, as observed in Table 14

## 6.0 Conclusion

### 6.1 Conclusion by Ahmad Nafis

In this experiment, the DC and AC behaviour of a common-emitter (CE) BJT amplifier was successfully analysed through theoretical calculation, circuit simulation and practical measurement. Each method provided a different level of accuracy and insight which are calculations offered an idealised understanding of transistor biasing and small-signal operation, simulations modelled the expected behaviour under near-real conditions and experimental measurements revealed the true performance of the circuit, including the effects of component tolerances and instrumentation limitations. The comparison of results highlighted that minor discrepancies are expected, particularly due to temperature effect and real-world loading conditions.

The determination of the Q-point confirmed that the transistor was correctly biased in the active region, enabling linear amplification. The phase observations showed the expected  $180^\circ$  inversion between input and output, consistent with CE amplifier theory. Additionally, the investigation of the bypass capacitor demonstrated its significant role in increasing voltage gain by reducing AC degeneration at the emitter.

Overall, the experiment met all objectives and provided a comprehensive understanding of how a CE amplifier operates in practice. The integration of theory, simulation and experimental verification strengthened the learning process, reinforcing both conceptual and hands-on proficiency in BJT amplifier analysis.

## 6.2 Conclusion by Wan Nazrul

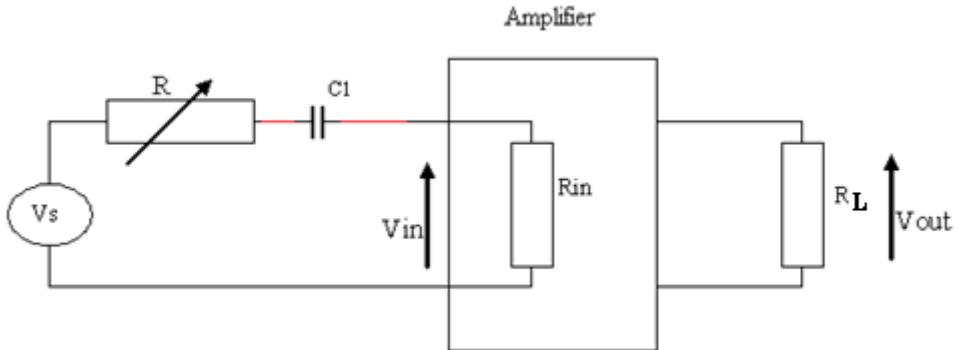
This experiment successfully achieved all of its objectives, which included analysing the performance of a BJT Common-Emitter (CE) amplifier from both the DC and AC perspectives, as well as comparing the results obtained using theoretical calculations, Multisim simulations, and practical measurements. The DC analysis verified that the 2N2222A transistor was properly biased in the active region, ensuring stable operation and enabling linear amplification of AC signals.

For the AC performance evaluation, all key parameters were successfully determined. The amplifier demonstrated an appropriate voltage gain, along with measurable input and output impedance values that aligned with the expected characteristics of a CE configuration. As predicted by CE amplifier theory, the circuit produced a  $180^\circ$  phase shift between the input and output signals. The study of the bypass capacitor (CE) further confirmed its importance, as its presence significantly increased the voltage gain by providing a low-impedance path for AC signals and reducing the AC degeneration effect caused by the emitter resistor (RE).

When comparing theoretical, simulation, and practical results, the simulation values were the closest to the theoretical predictions. Minor differences were observed in the practical measurements, which were reasonable given real-world influences such as component tolerances, variations in the transistor's actual beta, and loading effects from measuring instruments like the oscilloscope. Overall, the experiment was successful and provided a strong understanding of both the operating principles and real-world limitations of a BJT CE amplifier.

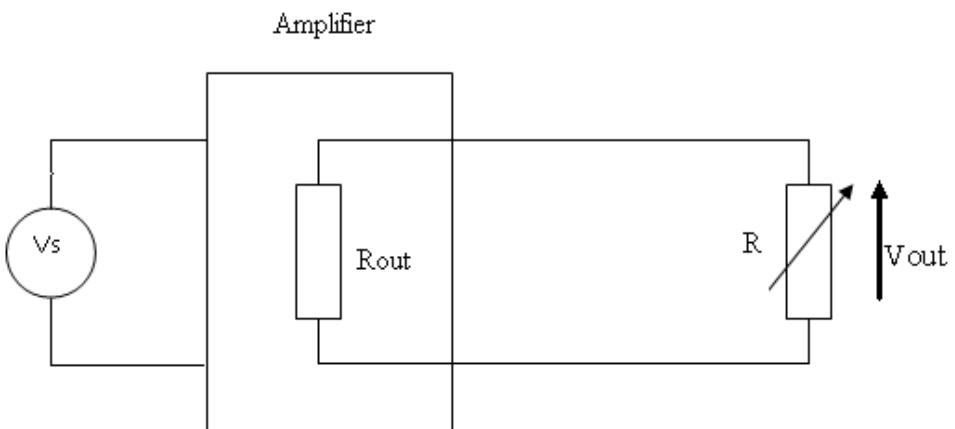
## Appendix 1

### A. Input Impedance Measurement



1. Using Figure:1, insert variable resistor,  $R$  between the Function generator and the coupling capacitor  $C_1$ .
2. Set the variable resistor,  $R$  to zero ( $0$  = short circuit) and **monitor  $V_{out}$**  at the oscilloscope
3. Increase the setting of  $R$  until  $V_{out}$  become exactly half of its value in (2).
4. The value of  $R$  is now approximately equal to the value of input resistance of the amplifier,  $Z_i$

### B. Output Impedance Measurement



1. Using Figure: 1, remove the load and **measure  $V_{out}$**  using the oscilloscope
2. Replace the load with variable resistor,  $R$ .
3. Varies the setting of  $R$  until  $V_{out}$  become exactly half of its value in (1).

The value of  $R$  is now approximately equal to the value of output resistance of the amplifier,  $Z_o$ .

**Knowledge Profiles (SK)** A programme that builds this type of knowledge and develops the attributes listed below is typically achieved in 4 years of study

<b>SK1</b>	A systematic, theory-based understanding of the natural sciences applicable to the sub-discipline
<b>SK2</b>	Conceptually-based mathematics, numerical analysis, statistics and aspects of computer and information science to support analysis and use of models applicable to the sub-discipline
<b>SK3</b>	A systematic , theory-based formulation of engineering fundamentals required in an accepted sub-discipline
<b>SK4</b>	Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for an accepted sub-discipline
<b>SK5</b>	Knowledge that supports engineering design using the technologies of a practice area
<b>SK6</b>	Knowledge of engineering technologies applicable in the sub-discipline
<b>SK7</b>	Comprehension of the role of technology in society and identified issues in applying engineering technology: ethics and impacts: economic, social, environmental and sustainability
<b>SK8 ✓</b>	Engagement with the technological literature of the discipline

**Definition of Broadly-Defined Problem Solving (SP)**

No.	Attribute	Broadly-defined Engineering Problems have characteristic SP1 and some or all of SP2 to SP7:
<b>SP1 ✓</b>	<b>Depth of Knowledge Required</b>	Cannot be resolved without engineering knowledge at the level of one or more of SK 4, SK5, and SK6 supported by SK3 with a strong emphasis on the application of developed technology
<b>SP2 ✓</b>	<b>Range of conflicting requirements</b>	Involve a variety of factors which may impose conflicting constraints.
<b>SP3 ✓</b>	<b>Depth of analysis required</b>	Can be solved by application of well-proven analysis techniques
<b>SP4</b>	<b>Familiarity of issues</b>	Belong to families of familiar problems which are solved in well-accepted ways
<b>SP5</b>	<b>Extent of applicable codes</b>	May be partially outside those encompassed by standards or codes of practice
<b>SP6</b>	<b>Extent of stakeholder involvement and level of conflicting requirements</b>	Involve several groups of stakeholders with differing and occasionally conflicting needs
<b>SP7</b>	<b>Interdependence</b>	Are parts of, or systems within complex engineering problems

**Range of Engineering Activities (TA)**

No.	Attribute	Broadly-defined activities
<b>TA1</b>	<b>Range of resources</b>	Involve a variety of resources (and for this purposes resources includes people, money, equipment, materials, information and technologies)
<b>TA2</b>	<b>Level of interactions</b>	Require resolution of occasional interactions between technical, engineering and other issues, of which few are conflicting
<b>TA3</b>	<b>Innovation</b>	Involve the use of new materials, techniques or processes in non-standard ways
<b>TA4</b>	<b>Consequences to society and the environment</b>	Have reasonably predictable consequences that are most important locally, but may extend more widely
<b>TA5</b>	<b>Familiarity</b>	Require a knowledge of normal operating procedures and processes



## ASSESSMENT COVERSHEET

Attach this coversheet as the cover of your submission. All sections must be completed.

### Section A: Submission Details

<b>Programme</b>	BTET			
<b>Course Code &amp; Name</b>	BEB24503 ELECTRONIC DEVICES AND CIRCUITS			
<b>Course Lecturer(s)</b>	MR AHMAD BASRI ZAINAL			
<b>Submission Title</b>	LAB 1 EDAC			
<b>Deadline</b>	Day	Month	Year	Time
<b>Penalties</b>	<ul style="list-style-type: none"><li>• 5% will be deducted per day to a maximum of four (4) working days, after which the submission will <b>not</b> be accepted.</li><li>• Plagiarised work is an Academic Offence in University Rules &amp; Regulations and will be penalised accordingly.</li></ul>			

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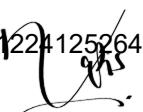
#### Office Receipt of Submission

Date & Time of Submission (stamp)	Student Name(s)	Student ID(s)
21/11/2025	AHMAD NAFIS BIN MOHD ZULKIFLI	51224125264

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