



AHMAD REZAEI

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RESEARCH INTERESTS

Hardware acceleration, Machine Learning, Pipelined processors design

EDUCATION

Bachelor of Science | *Major: Electrical Engineering, Minor: Electronics*

Sep. 2014 – Sep 2019

Shahid Bahonar University

Kerman, Iran

Score: 3.0/4.0

Dissertation: Developing Dynamic Bayesian networks for SET analysis in digital circuits

Supervisor: Prof. Ali Mahani

Secondary school and High-school

Sep. 2008 – May 2014

National Organization for Development of Exceptional Talents (NODET)

Sirjan, Iran

PUBLICATIONS

Rezaei, A., Mahani, A., (2021). Noise-based logic locking scheme against signal probability skew analysis. IET Computers & Digital Techniques. Accepted- in publication procedure. Article DOI: 10.1049/cdt2.12022

ACADEMIC EXPERIENCE

Researcher

January 2019 – present

Reliable and Smart System Laboratory

SBUK

- Conducting research on secure digital circuits, and hardware design and implementation of machine learning models.

Laboratory Assistant

September 2019 – January 2021

Digital System Design II lab.

SBUK

- Instructing students on design, synthesis, and implementation of MIPS processors.
- Semesters: September 2019 – January 2020 and September 2020 – January 2021

Teacher Assistant

September 2019 – January 2020

Test and Testable Design Course

SBUK

- Atalanta software workshop

PROJECTS AND RESEARCH

Hardware Implementation of Mauler ML network on Kintex-7 FPGA device | *C++, HLS*

Ongoing

Reliable and Smart Systems Lab.

Basecaller's Accuracy Enhancement using attention based LSTM network | *Tensorflow 2*

Ongoing

Reliable and Smart Systems Lab.

Design and implementation of Piplined MIPS processor on Spartan-6 FPGA device | *Verilog, Assembly*

Computer Architecture Course, Digital System II lab.

Test pattern generation using Synopsys TetraMAX software

April 2019

Test and Testable Design course

Reliability analysis of extra-stage butterfly network | *SHARPE*

September 2019

Fault Diagnosis and Tolerance course

Designing hardware for tanh/sinh activation function based on CORDIC algorithm

May 2018

Digital System Design(FPGA, ASIC) course

HONORS AND AWARDS

C++ programming course Certificate of successful completion in Beginning C++ Programming-From Beginner to Beyond course by Frank J. Mitropoulos	April 2020
Xilinx Vivado HLS course Certificate of successful completion in FPGA Design with High Level Synthesis Tool(Vivado HLS) course by Digitronix Nepal	February 2020
Top 7 qualified for the second stage of Synopsys Olympiad 13Th Synopsys Microelectronic annual Olympiad in Iran	September 2018
Tuition Waiver Among top 5% of participants, Recieved full scholarship from SBUK	September 2014

VOLUNTARY WORKS

Baran Charity Sales Person in Booth	December 2017 SBUK
Executive team member Multiple fundraising events for orphans and poorly supervised children	July 2015 Sirjan, Iran

SKILLS

Languages: English (IELTS 7.5 score), German (C1 - to be taken soon), Persian (Native)
Programming: Python(Tensorflow 1&2, NumPy, Sklearn, Matplotlib, Pandas), C++/C, Verilog/VHDL, MATLAB, Assembly
Digital Design: Xilinx Vivado Design Suite and HLS, Design Compiler, Cadence SoC Encounter, Modelsim, ChipScope, Espresso Logic Minimizer, H-Spice, P-Spice
Test and Verification: Synopsys TetraMAX, ATALANTA
Microprocessors and Microcontrollers: IAR Embedded Workbench, Codevision, Atmel Studio, Arduino

REFERENCES

Prof. Ali Mahani PHD, Associate professor Head of EE Department Department of Electrical engineering Shahid Bahonar university of Kerman Kerman, Iran http://academicstaff.uk.ac.ir/en/amahani ☎ +98 34 31322518 ✉ Amahani@uk.ac.ir ✉ mahani.akh@gmail.com	Prof. Hossein Nezamabadipour Professor of Elec. Eng. Department of Electrical Engineering Shahid Bahonar university of Kerman Kerman, Iran http://academicstaff.uk.ac.ir/en/nezam ☎ +98 34 31322510 ✉ nezam@uk.ac.ir ✉ nezam.h@yahoo.com
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