



# AHMAD REZAEI

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## RESEARCH INTERESTS

Hardware acceleration, Machine Learning, Computer Architecture

## EDUCATION

<b>Bachelor of Science</b>   <i>Major: Electrical Engineering, Minor: Electronics</i> Shahid Bahonar University Score: 3.0/4.0 Dissertation: Developing Dynamic Bayesian networks for SET analysis in digital circuits Supervisor: Prof. Ali Mahani	Sep. 2014 – Sep 2019 Kerman, Iran
<b>Secondary school and High-school</b> National Organization for Development of Exceptional Talents (NODET Special School)	Sep. 2008 – May 2014 Sirjan, Iran

## PUBLICATIONS

Rezaei, A., Mahani, A., (2020). Noise-based logic locking scheme against signal probability skew analysis. IET Computers & Digital Techniques. Accepted- in publication procedure. Article DOI: 10.1049/cdt2.12022

## ACADEMIC EXPERIENCE

<b>Researcher</b> Reliable and Smart System Laboratory <ul style="list-style-type: none"><li>Conducting research on secure digital circuits, and hardware design and implementation of machine learning models.</li></ul>	January 2019 – present SBUK
<b>Laboratory Assistant</b> Digital System Design II lab. <ul style="list-style-type: none"><li>Instructing students on design, synthesis, and implementation of MIPS processors.</li><li>Semesters: September 2019 – January 2020 and September 2020 – January 2021</li></ul>	September 2019 – January 2021 SBUK
<b>Teacher Assistant</b> Test and Testable Design Course <ul style="list-style-type: none"><li>Atalanta software workshop</li></ul>	September 2019 – January 2020 SBUK

## RESEARCH

<b>Hardware Implementation of Mauler ML network on Kintex-7 FPGA device</b>   <i>C++, HLS</i> Reliable and Smart Systems Lab.	Ongoing
<b>Basecaller's Accuracy Enhancement using attention based LSTM network</b>   <i>Tensorflow 2</i> Reliable and Smart Systems Lab.	Ongoing
<b>Design and implementation of Piplined MIPS processor on Spartan-6 FPGA device</b>   <i>Verilog, Assembly</i> Computer Architecture Course, Digital System II lab.	
<b>Test pattern generation using Synopsys TetraMAX software</b> Test and Testable Design course	April 2019
<b>Reliability analysis of extra-stage butterfly network</b>   <i>SHARPE</i> Fault Diagnosis and Tolerance course	September 2019
<b>Designing hardware for tanh/sinh activation function based on CORDIC algorithm</b> Digital System Design(FPGA, ASIC) course	May 2018

## HONORS AND AWARDS

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### **C++ programming course**

April 2020

Certificate of successful completion in Beginning C++ Programming-From Beginner to Beyond course by Frank J. Mitropoulos

### **Xilinx Vivado HLS course**

February 2020

Certificate of successful completion in FPGA Design with High Level Synthesis Tool(Vivado HLS) course by Digitronix Nepal

### **Top 7 qualified for the second stage of Synopsys Olympiad**

September 2018

13Th Synopsys Microelectronic annual Olympiad in Iran

### **Tuition Waiver**

September 2014

Among top 5% of participants, Recieved full scholarship from SBUK

## SKILLS

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**Languages:** English (IELTS 7.5 score), German (C1 - to be taken soon), Persian (Native)

**Programming:** Python(Tensorflow 1&2, NumPy, Scikit, Matplotlib, Pandas), C++/C, Verilog/VHDL, MATLAB, Assembly

**Digital Design:** Xilinx Vivado Design Suite and HLS, Design Compiler, Cadence SoC Encounter, Modelsim, ChipScope, Espresso Logic Minimizer, H-Spice, P-Spice

**Test and Verification:** Synopsys TetraMAX, ATALANTA

**Microprocessors and Microcontrollers:** IAR Embedded Workbench, Codevision, Atmel Studio, Arduino

## REFERENCES

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Head of EE Department  
Department of Electrical engineering  
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