Ahmad Rezaei

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Email
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Linkedin
Research Gate

Research Interests

Cross-layer acceleration, Machine Learning, Computer Architecture, Bioinformatics

Education

Bachelor of Science | ***Major: Electrical Engineering, Minor: Electronics*** Sep. 2014 – Sep 2019
Shahid Bahonar University Kerman, Iran
Score: 15,14/20
Dissertation: Developing Dynamic Bayesian networks for SET analysis in digital circuits
Supervisor: Prof. Ali Mahani

Secondary school and High-school Sep. 2008 – May 2014
National Organization for Development of Exceptional Talents (NODET Special School) Sirjan, Iran

Publications

Rezaei, A., & Mahani, A. (2021). Noise-based logic locking scheme against signal probability skew analysis. IET Computers & Digital Techniques.
Journal Paper DOI: 10.1049/cdt2.12022

Academic Experience

Researcher January 2019 – present
Reliable and Smart System Laboratory SBUK
- Conducting research on secure digital circuits, and hardware design and implementation of machine learning models.

Laboratory Assistant September 2019 – January 2021
Digital System Design II lab. SBUK
- Instructing students on design, synthesis, and implementation of MIPS processors.
- Semesters: September 2019 – January 2020 and September 2020 – January 2021

Teacher Assistant September 2019 – January 2020
Test and Testable Design Course SBUK
- Atalanta software workshop

Research & Academic Projects

Cross-layer acceleration of Mauler ML network on Kintex-7 FPGA device | ***C++, HLS*** Ongoing
Reliable and Smart Systems Lab.

Basecaller's Accuracy Enhancement using attention based LSTM network | ***Tensorflow 2*** Ongoing
Reliable and Smart Systems Lab.

Design and implementation of Piplined MIPS processor on Spartan-6 FPGA device| ***Verilog, Assembly***
Computer Architecture Course, Digital System II lab.

Test pattern generation using Synopsys TetraMAX software April 2019
Test and Testable Design course

Reliability analysis of extra-stage butterfly network | ***SHARPE*** September 2019
Fault Diagnosis and Tolerance course

Designing hardware for tanh/sinh activation function based on CORDIC algorithm May 2018
Digital System Design(FPGA, ASIC) course

Honors and Awards

C++ programming course April 2020
Certificate of successful completion in Beginning C++ Programming-From Beginner to Beyond course by Frank J. Mitropoulos

Xilinx Vivado HLS course February 2020
Certificate of successful completion in FPGA Design with High Level Synthesis Tool(Vivado HLS) course by Digitronix Nepal

Top 7 qualified for the second stage of Synopsys Olympiad September 2018
13Th Synopsys Microelectronic annual Olympiad in Iran

Tuition Waiver September 2014
Among top 5% of participants, Recieved full scholarship from SBUK

Skills

Languages: English (IELTS 7.5 score), German (C1 - to be taken soon), Persian (Native)

Programming: Python(Tensorflow 1&2, NumPy, Scikit, Matplotlib, Pandas), C++/C, Verilog/VHDL, MATLAB, Assembly

Digital Design: Xilinx Vivado Design Suite and HLS, Design Compiler, Cadencee SoC Encounter, Modelsim, ChipScope, Espresso Logic Minimizer, H-Spice, P-Spice

Test and Verification: Synopsys TetraMAX, ATALANTA

Microprocessors and Microcontrollers: IAR Embedded Workbench, Codevision, Atmel Studio, Arduino

References

Prof. Ali Mahani
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Prof. Hossein Nezamabadipour
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Department of Electrical Engineering
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