Homework 3 Written

The pdf you submit must look exactly like this with the answers and all supporting works shown on the the page with the question.

Last Name	First Name	Student ID
Waheed	Muhammad	912741425

Partner Last Name	Partner First Name	Partner Student ID
Magno	Mathew	913366789

available f.f = T
required f.f = JK

1. (5 points) Create a JK Flip-Flop using only a T Flip-Flop and basic logic gates.

Characteristics table for J-K

J	K	State Current	State Next
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Current State	T	Next State
0	0	0
0	1	1
1	0	1
1	1	0

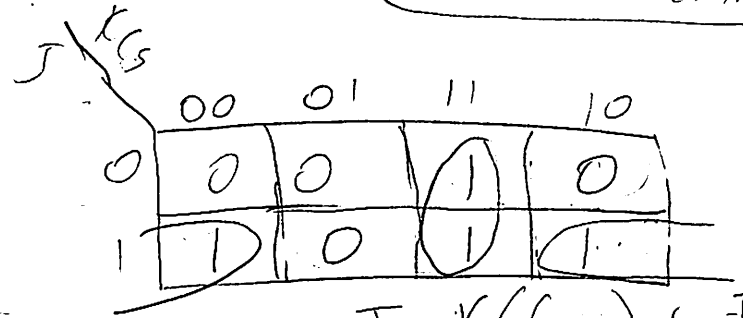
Excitation table for T

J	K	State Current	T
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

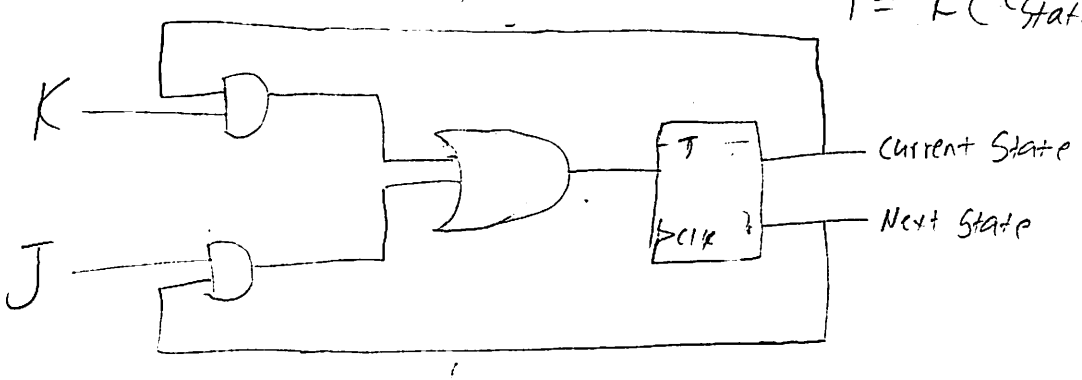
Excitation Table

Current State	Next State	T
0	0	0
0	1	1
1	0	1
1	1	0

Example

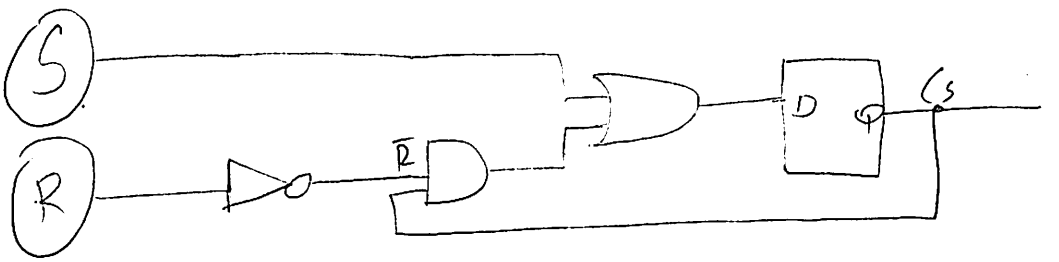


$T = K(C_{state}) + J(N_{state})$



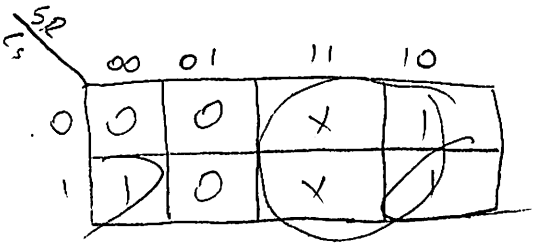
2. (5 points) Create an SR Flip-Flop using only a D Flip-Flop and basic logic gates.

$$D = (\overline{R} \cdot Q) + S$$



S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	X	-
1	1	X	X

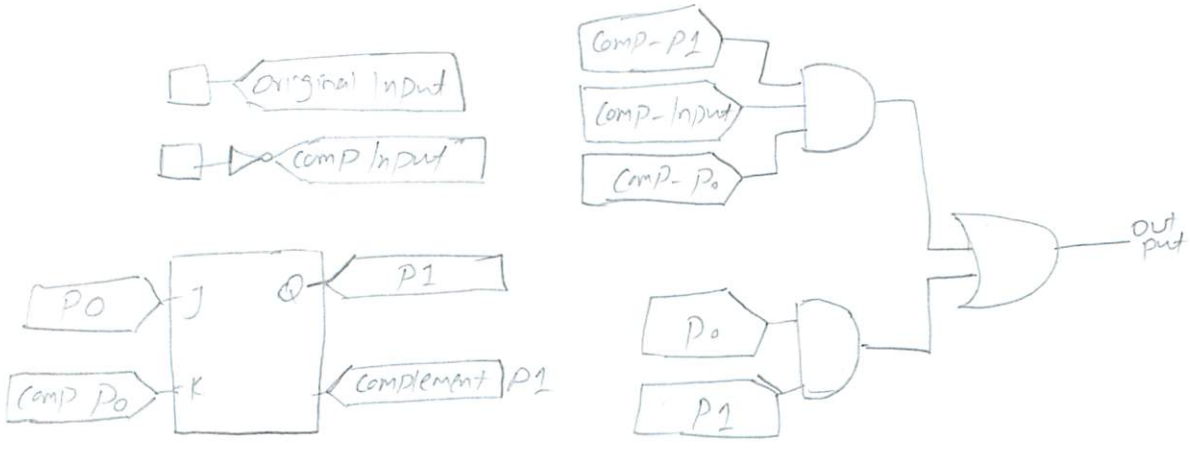
D
0
1
0
0
1
1
X
X

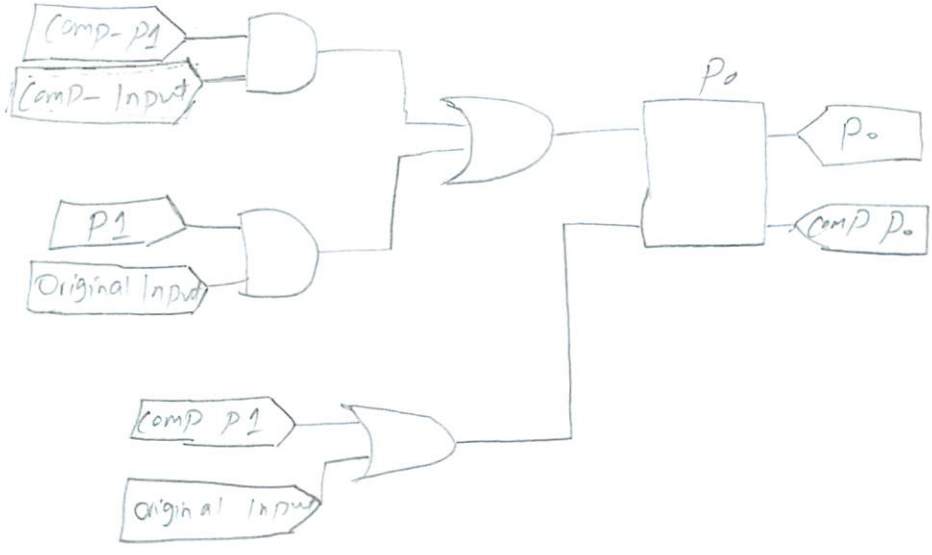


$D = SOP' = S + C_s \overline{R}$

3. (5 points) Implement the **simplest** circuit possible using **JK Flip-Flops** based on the following transition table.

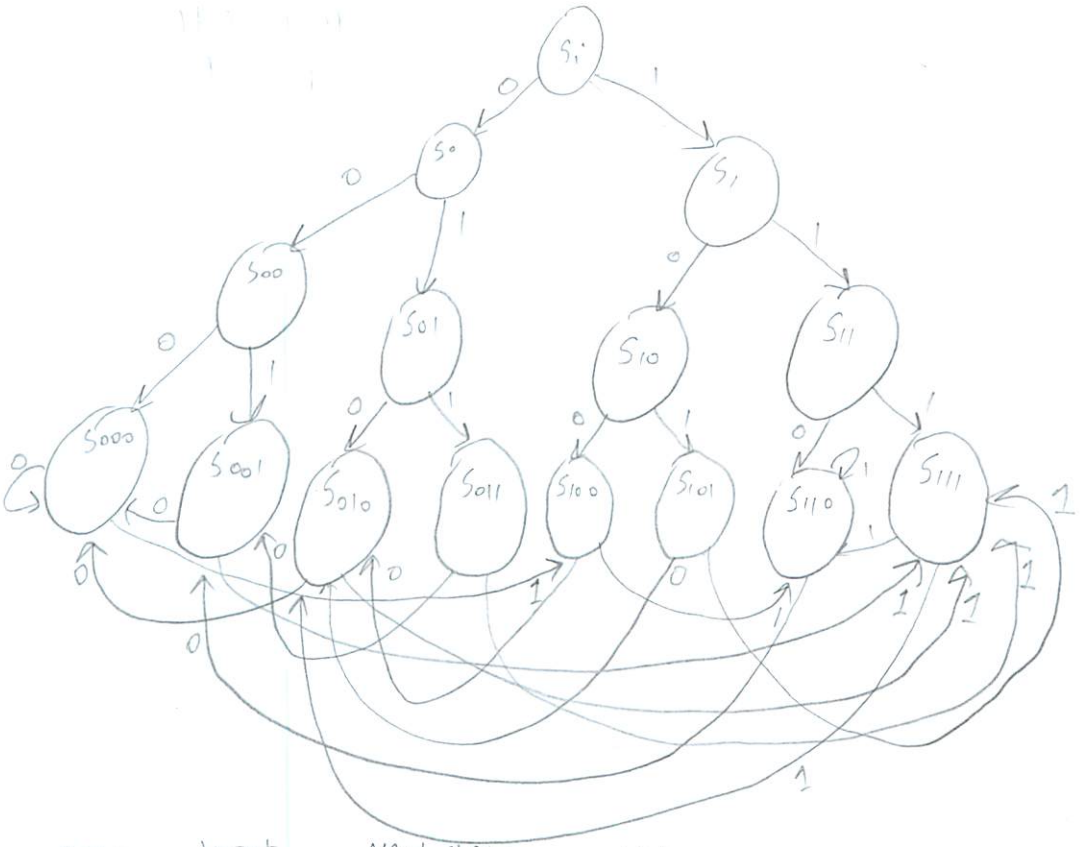
Current State/Encoding	Input	Next State	Output
00	0	11	1
00	1	10	0
01	D	00	0
10	0	10	0
10	1	11	0
11	0	01	1
11	1	00	1





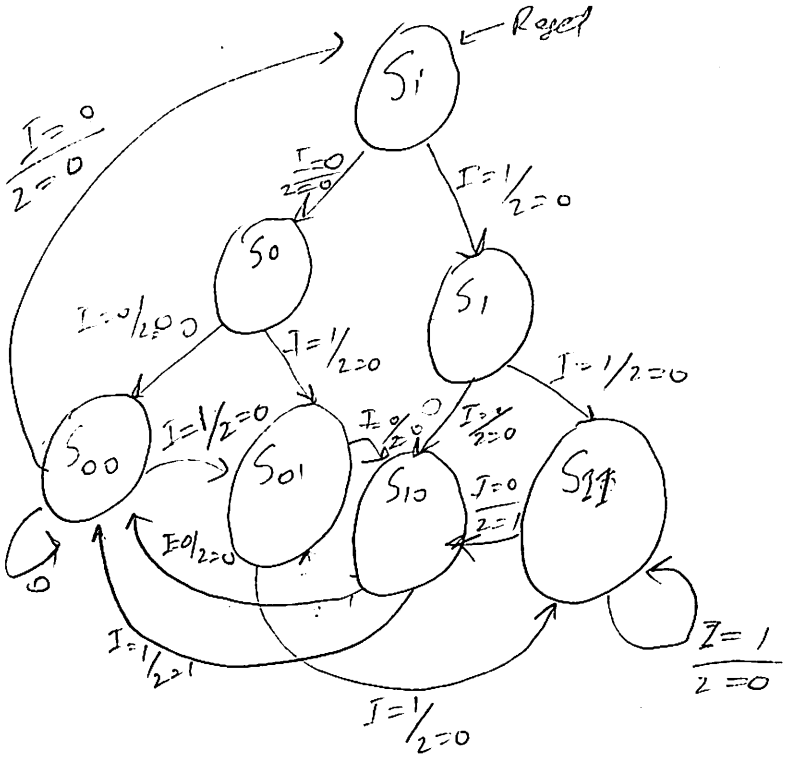
110 101

4. (5 points) Derive the **minimal** state table for a single input, single output **Moore** model FSM that outputs 1 whenever it detects either 110 or 101 in the input sequence. Overlapping sequences should be detected. For example if the input is 1101 then the output would be 00011 (Don't forget that the output of a Moore is delayed 1 clock cycle behind the input.



Current state	Input	Next state	output
000	0	000	0
000	1	100	0
100	0	010	0
100	1	110	0
110	0	001	0
110	1	110	0
010	0	000	0
010	1	111	0
011	0	001	0
011	1	111	0
001	0	000	1
001	1	111	1
111	0	010	1
111	1	110	1

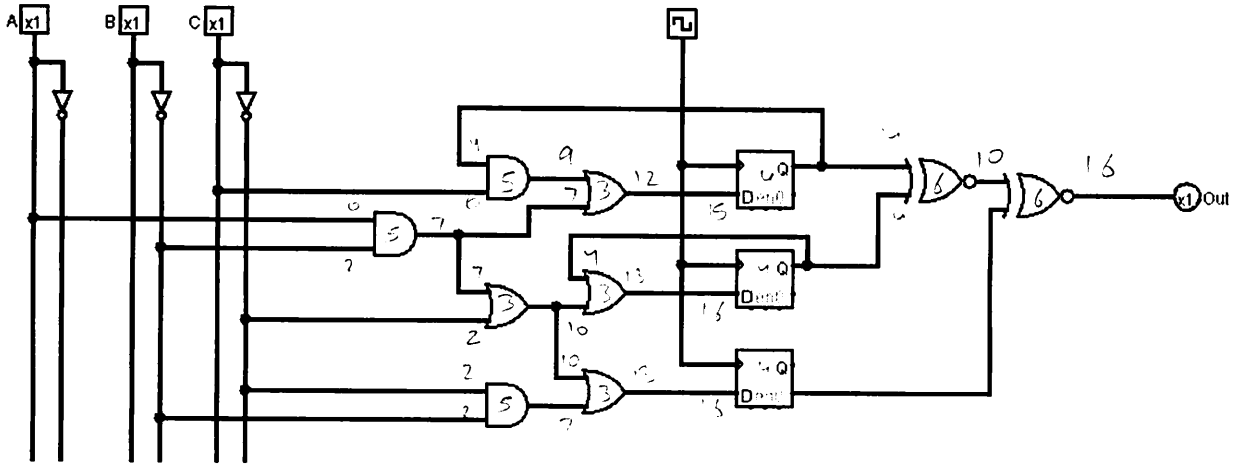
5. (5 points) Repeat number 4 but for a **Mealy** model FSM.



Current State	Input	Next State	Output
00	0	00	0
00	1	01	0
01	0	10	0
01	1	11	0
11	0	10	1
11	1	11	0
10	0	00	0
10	1	00	1

6. (5 points) Given the propagation delays contained in the table below and that the setup time for a D Flip-Flop is 3ns determine the length of the worst case path **and** the maximum clock frequency for the following circuit.

Gate	Propagation Delay
AND	5ns
OR	3ns
NOT	2ns
XNOR	6ns
D Flip-Flop	4ns



worst case = 16ns

max. clock freq. = $\frac{1}{16ns} = \frac{10^9}{16.}$ Hz