Homework 5
Points: 35

1. (3) Given that you have a Fully Associative cache of size 2^10 bytes with a line size of 16 bytes show how an Address of 29 bits would be partitioned.

Tag	Offset
28 - 4	3 - 0

2. (3) Given that you have Direct Mapped cache of size 2^12 bytes with a line size of 32 bytes show how an Address of 50 bits would be partitioned.

Tag	Set	Offset
49 - 12	11 - 5	4 - 0

3. (3)Given that you have a 5 way Set Associate cache of size 5242880 bytes with a line size of 64 bytes show how an Address of 64 bits would be partitioned.

Tag	Set	Offset
63 - 20	19 - 6	5 - 0

4. (3 per) Here is a string of hex address references given as byte addresses: 1, 2, 3, 1A, A,1B, 16, 14, 3, 12, 9, 23 ,3A, 5, 19, 1, 9
   1. Assuming a **direct mapped cache** with a **total size of 16 bytes** and a **line size that is 1 byte**. that is initially empty, label each reference in the list as a hit or miss and show the final contents of the cache tag bits for each line. If a line is not written to leave its tag bits blank. Compute the hit rate for this example.

Set	Tag
0	
1	0
2	1
3	2
4	1
5	0
6	1
7	
8	
9	0
10	3
11	1
12	
13	

14	
15	

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	M	M	M	M	M	M	M	H	M	M	M	M	M	M	H	M

    1. Hit rate = 2 / 17

2. Repeat 4.1 but for a **direct mapped cache** that is **16 bytes big** and has a **line size of 4 bytes.**

Set	Tag
0	0
1	0
2	0
3	

    1.

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	H	H	M	M	M	M	H	H	M	M	M	M	M	M	M	M

    2. Hit rate = 4/17

3. Repeat 4.1 but for a **two way set associative cache** that is **16 bytes big** and has a **line size of 1 byte**. Assume an **LRU replacement strategy** is used.
    1. The tags can be placed in either way

Set	Way 1	Way 2
0		
1	1	0
2	7	2
3	0	4
4	2	
5	0	
6	2	
7		

    2.

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	M	M	M	M	M	M	M	H	M	M	M	M	M	M	M	M

    3. Hit rate 1/17

4. Repeat 4.1 but for a **fully associative** cache that is **16 bytes big** and has a **line size of 1 byte**. Assume an **LRU replacement strategy** is used.
    1. 1, set so order doesn't matter.

Tag
1
2

3
1A
A
1B
16
14
12
9
23
3A
5
19

2.

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	M	M	M	M	M	M	M	H	M	M	M	M	M	M	H	H

3. Hit rate = 3/17

5. Repeat 4.1 but for a **fully associative** cache that is **16 bytes big** and has a **line size of 4 bytes**. Assume an **LRU replacement strategy** is used.

1. Since there is only 1 set tags can be in any order

2
6
1
0

2.

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	H	H	M	M	H	M	H	H	M	M	M	M	M	M	M	M

6. Hit rate = 5/17

5. (5) Consider a computer that has 2^{16} bytes of RAM and is using a Virtual Memory system whose virtual address is 32 bits long and is using a page size of 2^{10} bytes.

1. How many physical pages are there? $\frac{2^{16}}{2^{10}}=2^6$
2. How many virtual pages are there? $\frac{2^{32}}{2^{10}}=2^{22}$
3. How large is each entry in the page table (in bits)? $\log_2(2^6)=6\,bits$
4. How large is the page table for a single process (in bytes)? $6*2^{22}\,bits=6*2^{19}\,bytes$
5. Are there any problems with a page table that size? **It is larger than memory**

6. (6) Consider a computer that has 2^{18} bytes of RAM and is using a Virtual Memory system

with secondary page tables. The virtual address is 32 bits long and the page size is 2^{10} bytes. The size of the secondary pages is equal to the page size.

1. How many physical pages are there? $\frac{2^{18}}{2^{10}}=2^{8}$
2. How may virtual pages are there? $\frac{2^{32}}{2^{10}}=2^{22}$
3. How many secondary page tables are there? $\frac{2^{22}}{2^{10}}=2^{12}$
4. How large is each entry in the primary page table (in bytes)? 1 byte
5. How large is each entry in the secondary page table (in bytes)? 1 byte
6. How large is the primary page table (in bytes)? $2^{12}*1=2^{12}\mathit{bytes}$