5. Repeat 4.1 but for a **fully associative** cache that is **16 bytes big** and has a **line size of 4 bytes**. Assume an **LRU replacement strategy** is used.

Tag	0	1	2	6

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	H	H	M	M	H	M	H	H	M	M	M	M	M	M	M	M

Hit rate = $\frac{5}{17}$

4. Repeat 4.1 but for a **fully associative** cache that is **16 bytes big** and has a **line size of 1 byte.** Assume an **LRU replacement strategy** is used.

Tag	1	2	3	1A	A	1B	16	14	12	9	23	3A	5	19

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	M	M	M	M	M	M	M	H	M	M	M	M	M	M	H	H

Hit rate = $\frac{3}{17}$

3. Repeat 4.1 but for a **two way set associative cache** that is **16 bytes big** and has a **line size of 1 byte.** Assume an **LRU replacement strategy** is used.

Set	0	1	2	3	4	5	6	7
way1		1	7	0	2	0	2	
way2		0	2	4				

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5
M	M	M	M	M	M	M	M	H	M	M	M	M	M

19	1	9
M	M	M

Hit rate = $\frac{1}{17}$

2. Repeat 4.1 but for a **direct mapped cache** that is **16 bytes big** and has a **line size of 4 bytes**

Set	0	1	2	3
Tag	0	0	0	

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	H	H	M	M	M	M	H	H	M	M	M	M	M	M	M	M

Hit rate = $\frac{4}{17}$

4. (3 per) Here is a string of hex address references given as byte addresses: 1, 2, 3, 1A, A,1B, 16, 14, 3, 12, 9, 23 ,3A, 5, 19, 1, 9
   1. Assuming a **direct mapped cache** with a **total size of 16 bytes** and a **line size that is 1 byte**. that is initially empty, label each reference in the list as a hit or miss and show the final contents of the cache tag bits for each line. If a line is not written to leave its tag bits blank. Compute the hit rate for this example.

Set	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Tag		0	1	2	1	0	1			0	3	1					

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	M	M	M	M	M	M	M	H	M	M	M	M	M	M	H	M

Hit rate = $\frac{2}{17}$

3. (3)Given that you have a 5 way Set Associate cache of size 5242880 bytes with a line size of 64 bytes show how an Address of 64 bits would be partitioned.

The partition of an address of 64 bits will be:.

Tag	Set	offset
63-20	19-6	5-0

2. (3) Given that you have Direct Mapped cache of size 2^12 bytes with a line size of 32 bytes show how an Address of 50 bits would be partitioned.

The partition of an address of 50 bits will be:

Tag	Set	offset
49-12	11-5	4-0

1. (3) Given that you have a Fully Associative cache of size 2^10 bytes with a line size of 16 bytes show how an Address of 29 bits would be partitioned.

- The partition of an address of 29 bits will be:

Tag	offset
28-4	3-0

Homework 4 Written

Points: 35

The pdf you submit must look exactly like this with the answers and all supporting works shown on the the page with the question.

Last Name	First Name	Student ID
Waheed	Muhammad	912741428
Partner Last Name	**Partner First Name**	**Partner Student ID**
Magno	Mathew	913366789