



Zagazig University

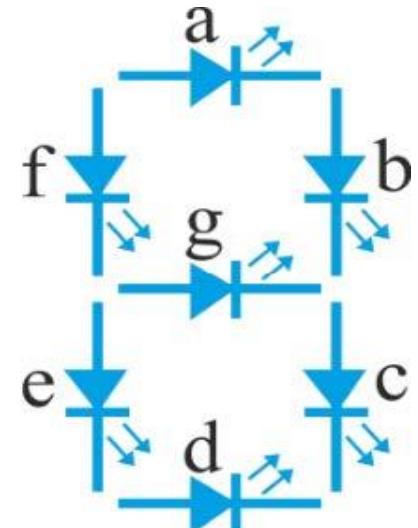
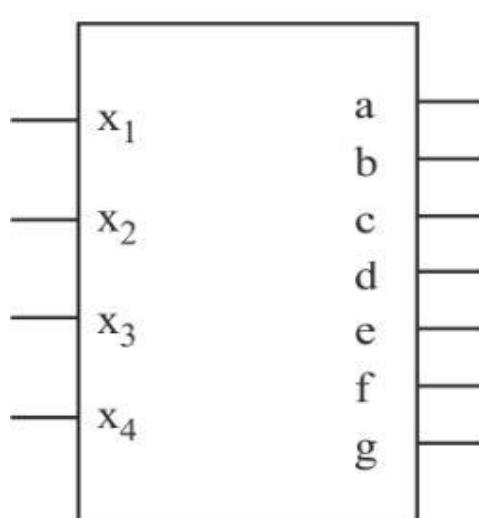
Faculty of Engineering

Electronics and Communications Dep.

5/15/2022

# Simple Binary Coded Decimal Decoder Implementation using CMOS technology\*\*

\*\*Custom design using Cadence virtuoso & (TCMC65nm)



## Team Members

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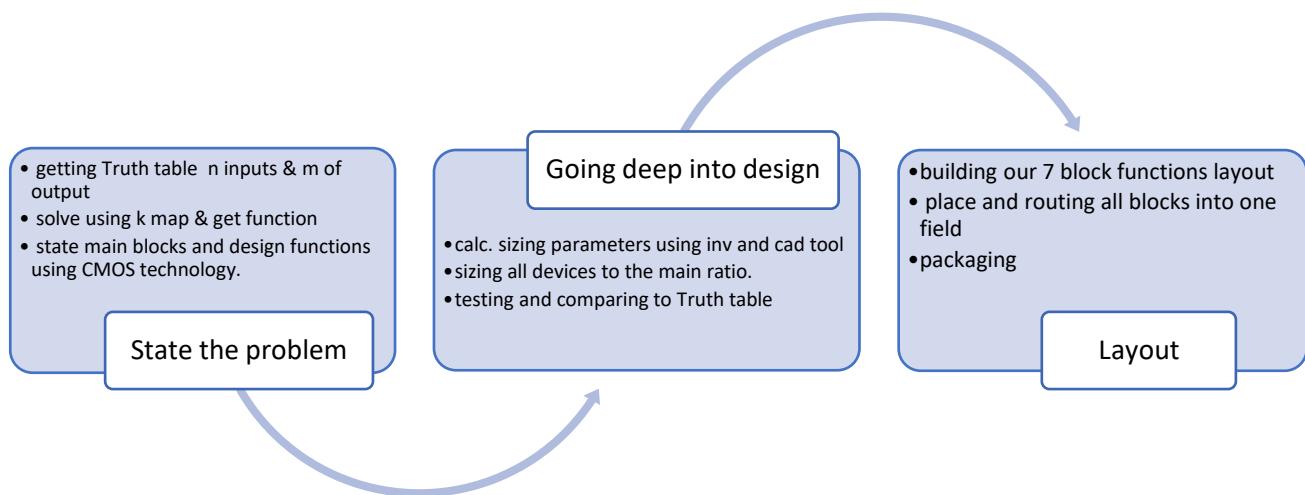
Digital IC Design Course

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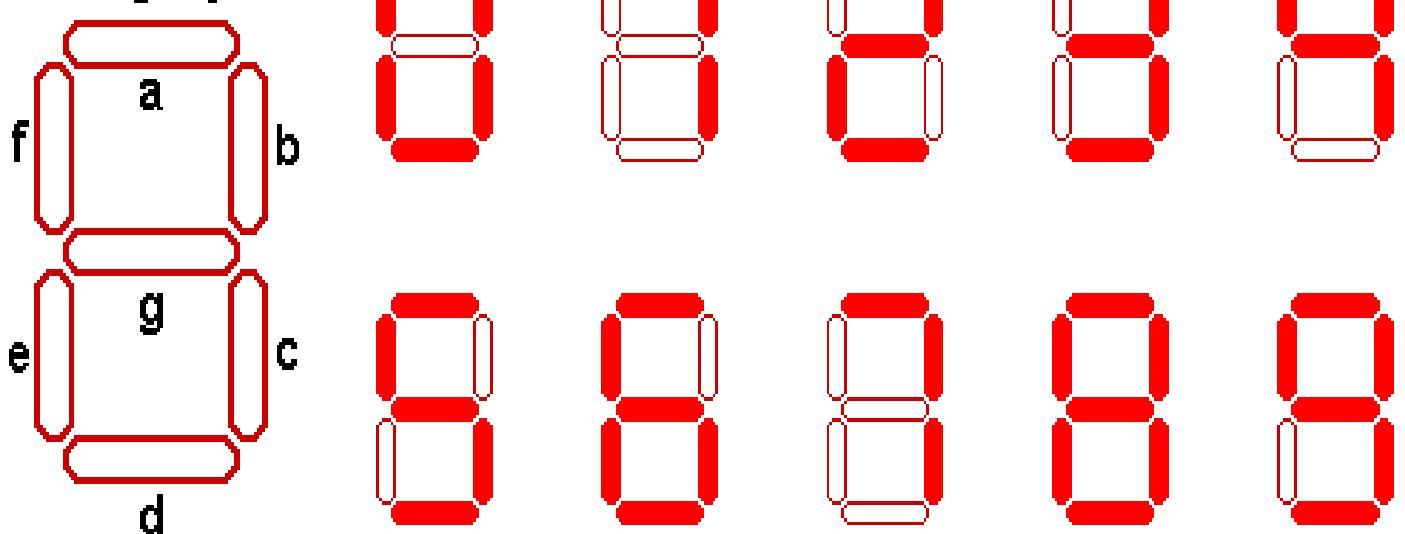
## ● Introduction:

What we are trying to do here is to implement binary coded decimal 4-bit input and 0-9 output, using CMOS technology ...

First, we may use the following flow diagram to brainstorm ideas behind the project :

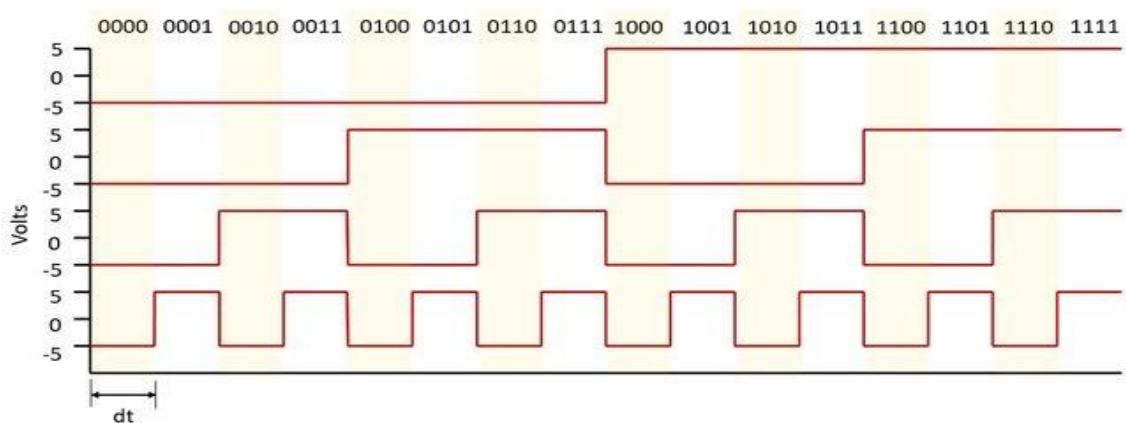


7-segment display



n	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X
15	1	1	1	1	X	X	X	X	X	X	X

● Input :



- Analysis & k-map:

a	b	c	d																																																																																																
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# note: we used x to denote to **don't care**.

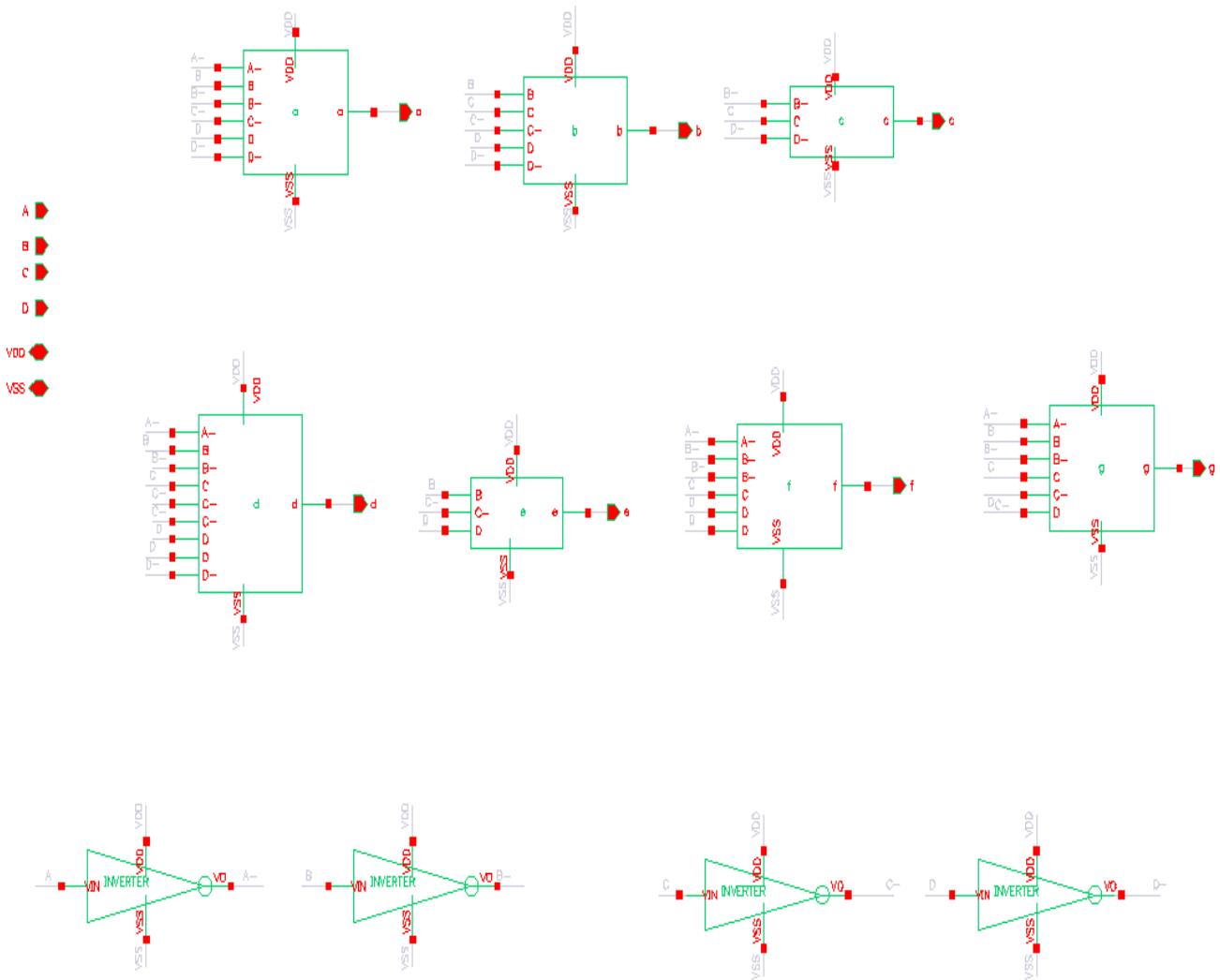
$$\begin{aligned}
 a' &= A'B'C'D + BC'D' \\
 b' &= B(C' + D').(C + D) \\
 c' &= B'CD' \\
 d' &= A'B'C'D + BCD + BC'D'
 \end{aligned}$$

$$\begin{aligned}
 e' &= D + BC' \\
 f' &= CB' + CD + A'B'D \\
 g' &= A'B'C' + BCD
 \end{aligned}$$

#CMOS transistors =  $76 + 4 * 2 = 84$  transistors

#Inverters

- Circuit diagram (cadence virtuoso):

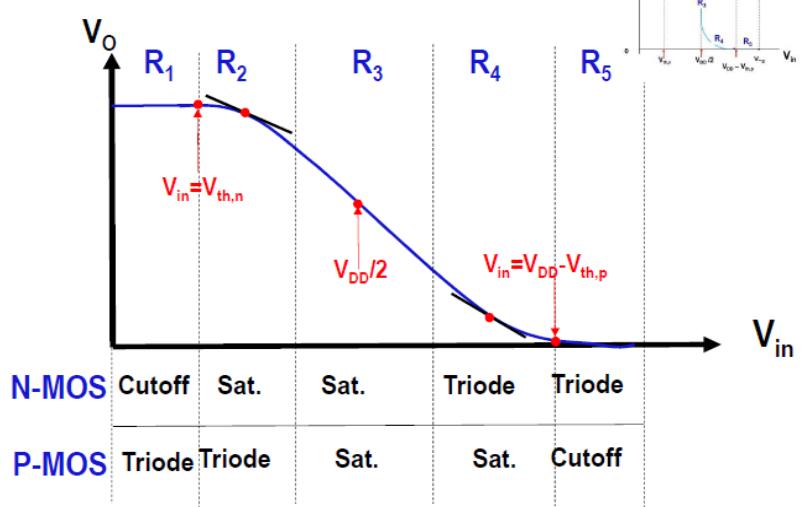
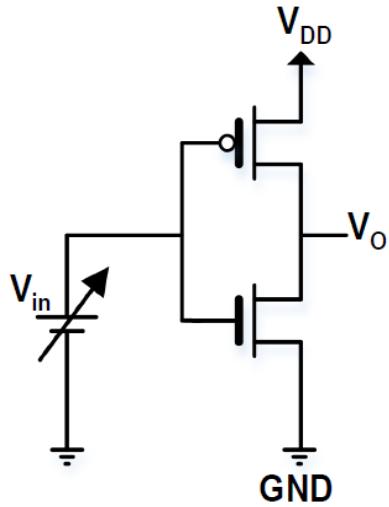


- Sizing:

- According to tech used (**tcmc65n**) we find minimum W/L ratio
- The main problem is that **Bn!=Bp** that makes the transfer from logic **1** to logic **0** (region3) taking more time than expected.
- So, we make W/L for nmos = 120n/60n and Lp=60n and sweep the value of **wp** in Vin-Vout Ch/s curve.
- We find wp at Vo=Vi=0.5vdd, that makes **Bn=Bp**

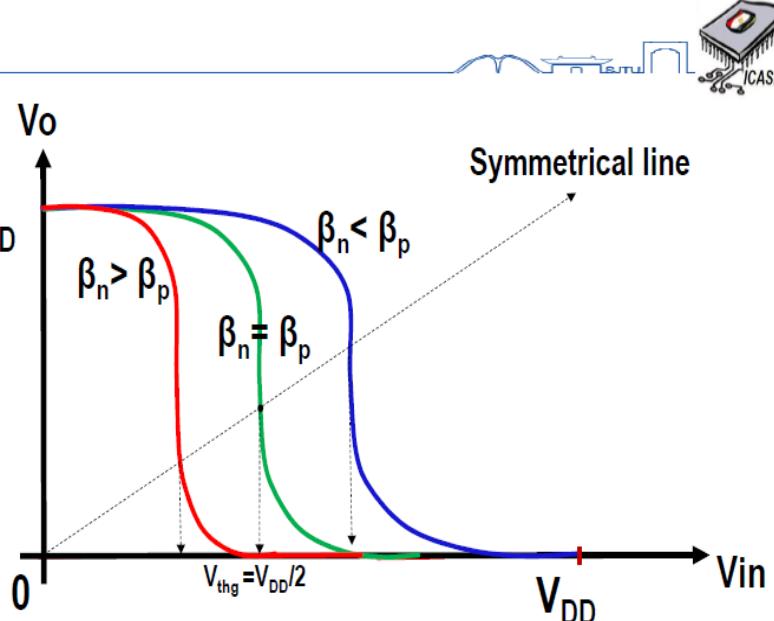
## DC Transfer Characteristics

### □ Static CMOS Inverter DC Characteristics

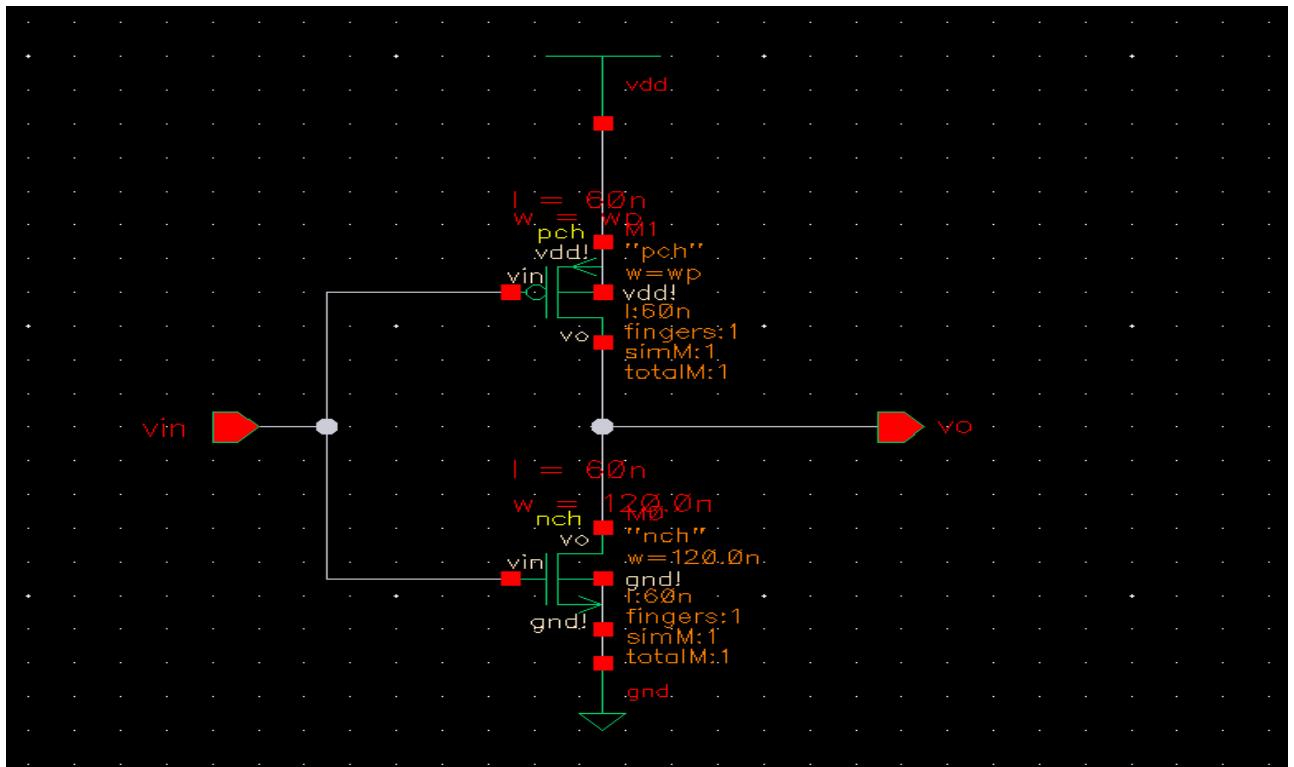


## Beta Ratio Effects :

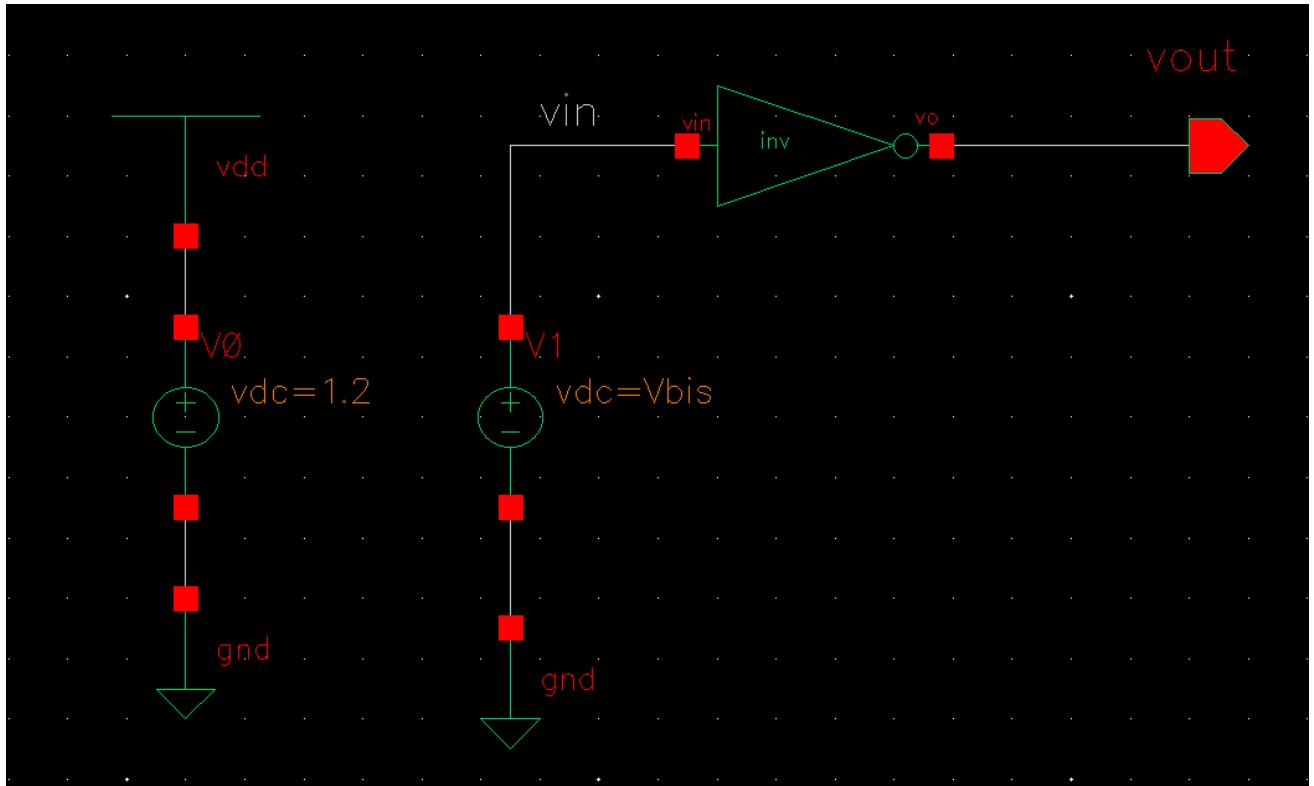
Case	Condition	$V_{thg}$
1	$\beta_n = \beta_p, V_{th,n} =  V_{th,p} $	$V_{thg} = V_{DD}/2$
2	$\beta_n > \beta_p, V_{th,n} =  V_{th,p} $	$V_{thg} < V_{DD}/2$
3	$\beta_n < \beta_p, V_{th,n} =  V_{th,p} $	$V_{thg} > V_{DD}/2$



- Using cadence tool to sweep & compute Wp:



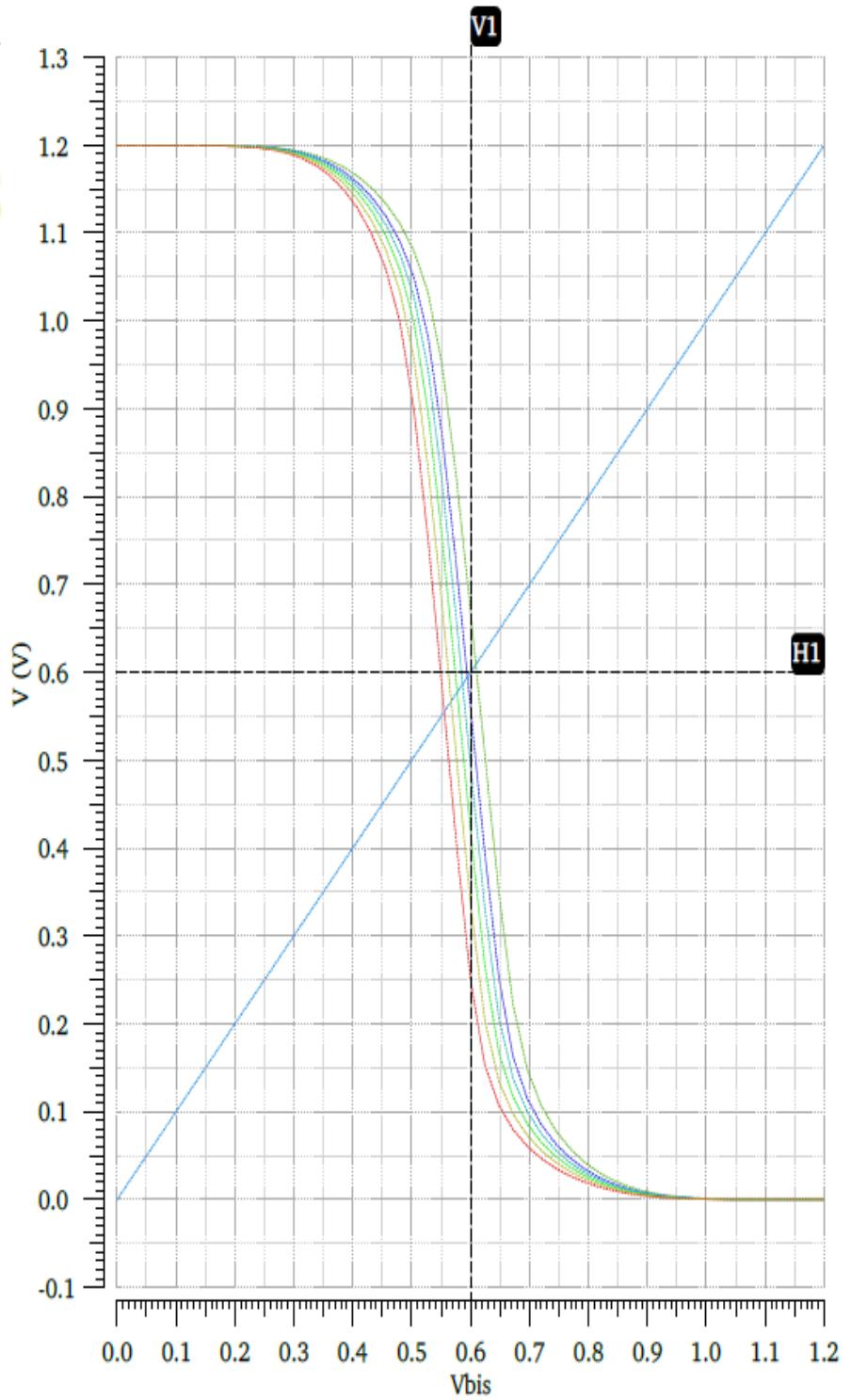
- Test bench:



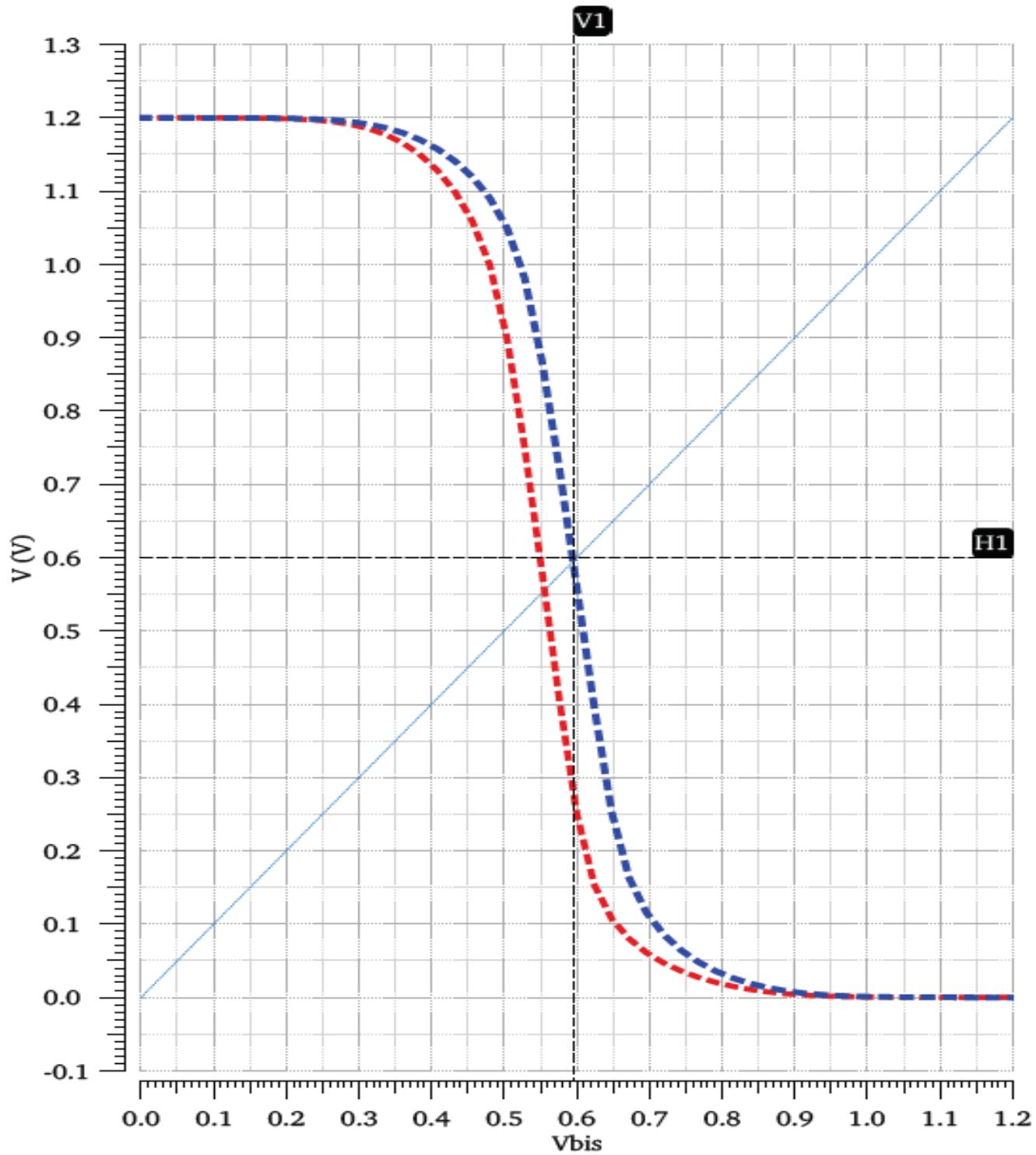
**DC Response****Sun May 22 07:15:57 2022**

Name	Vls	V1wp
/vout		
/vout	250.201mV	1.2e-07
/vout	336.778mV	1.5e-07
/vout	418.887mV	1.8e-07
/vout	492.935mV	2.1e-07
/vout	558.807mV	2.4e-07
/vout	669.186mV	3e-07
/vin	600.0mV	1.2e-07

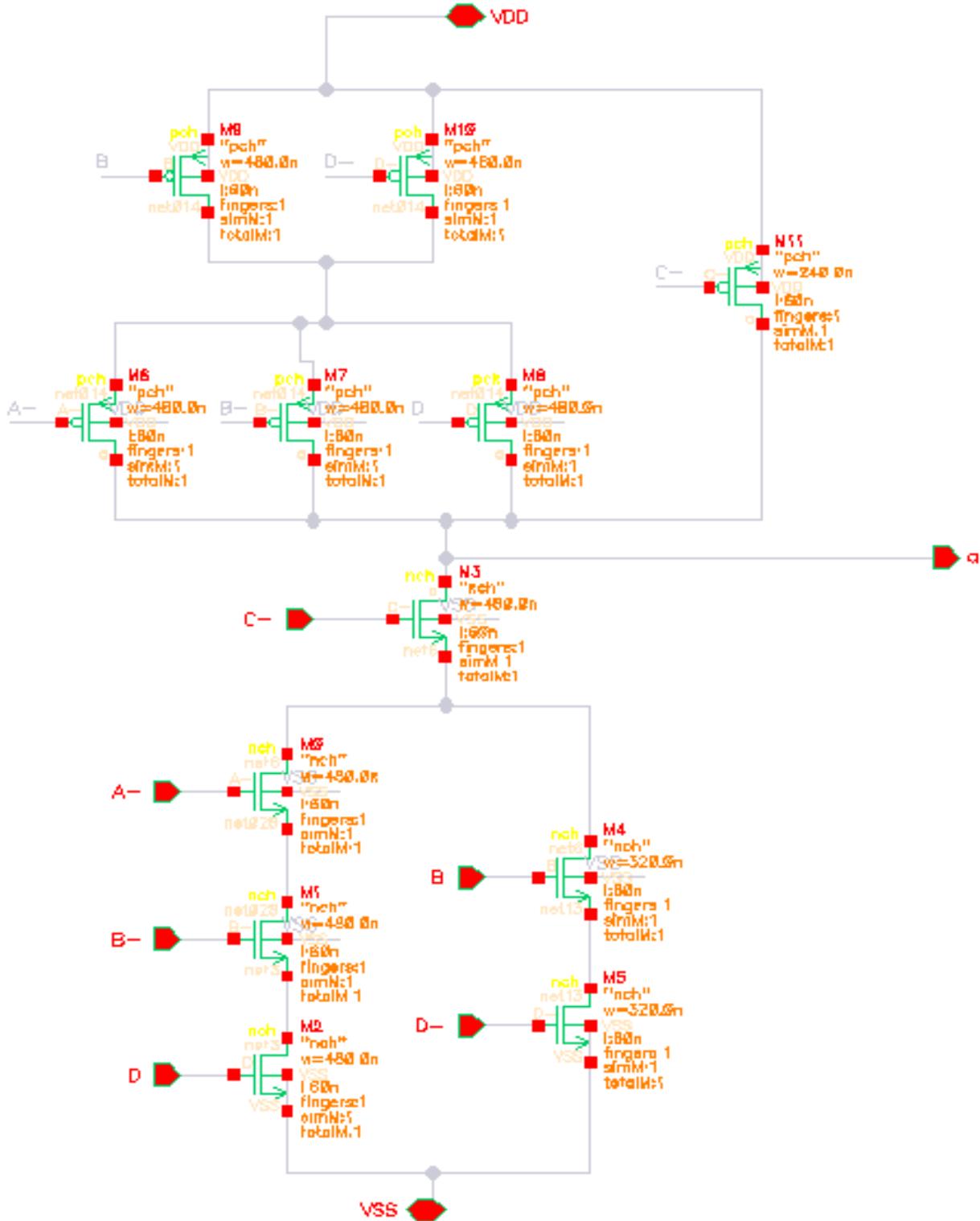
\*\* for  $B_n = B_p$ ,  
we take  $W_p = 2 * W_n$   
= 240nm

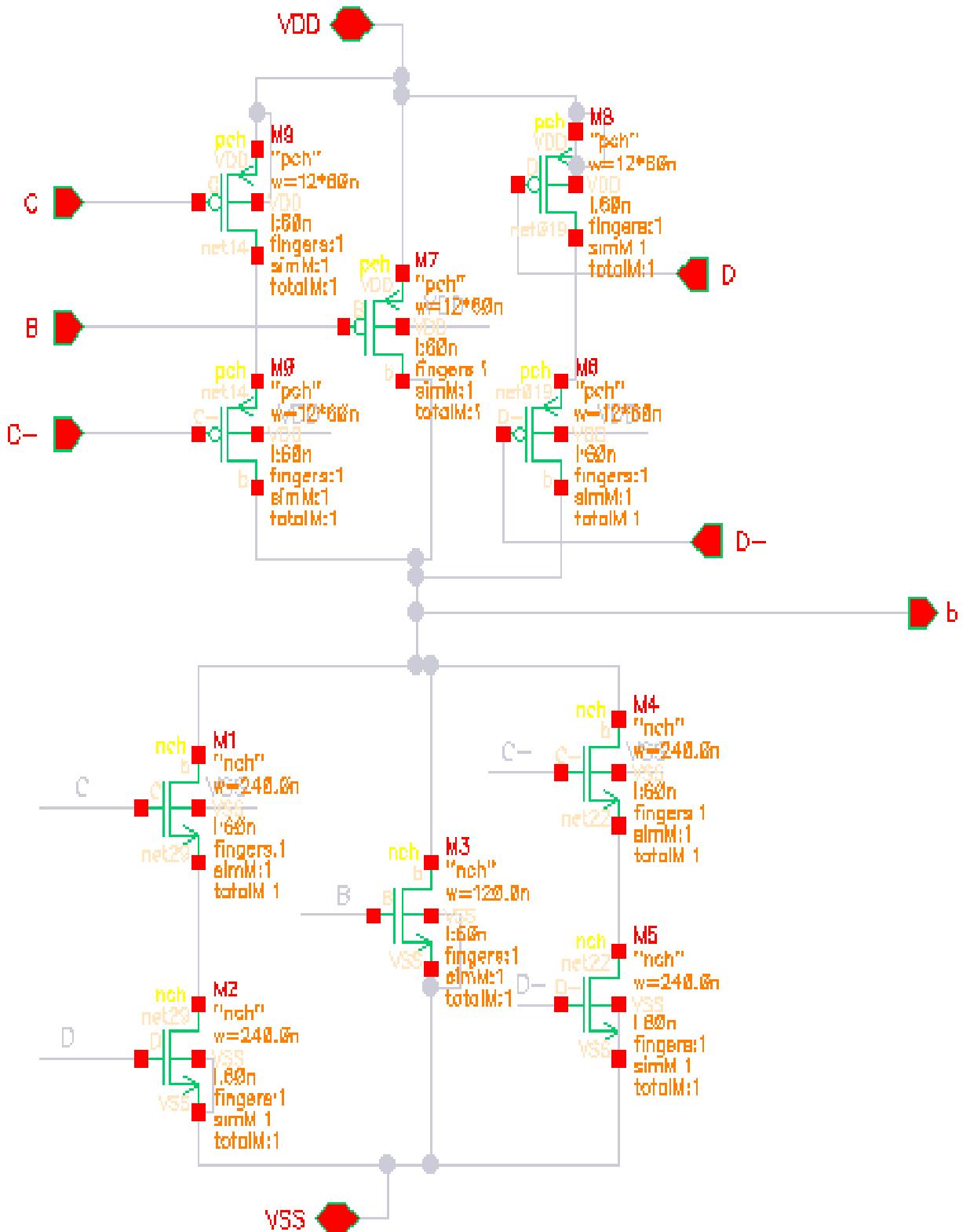


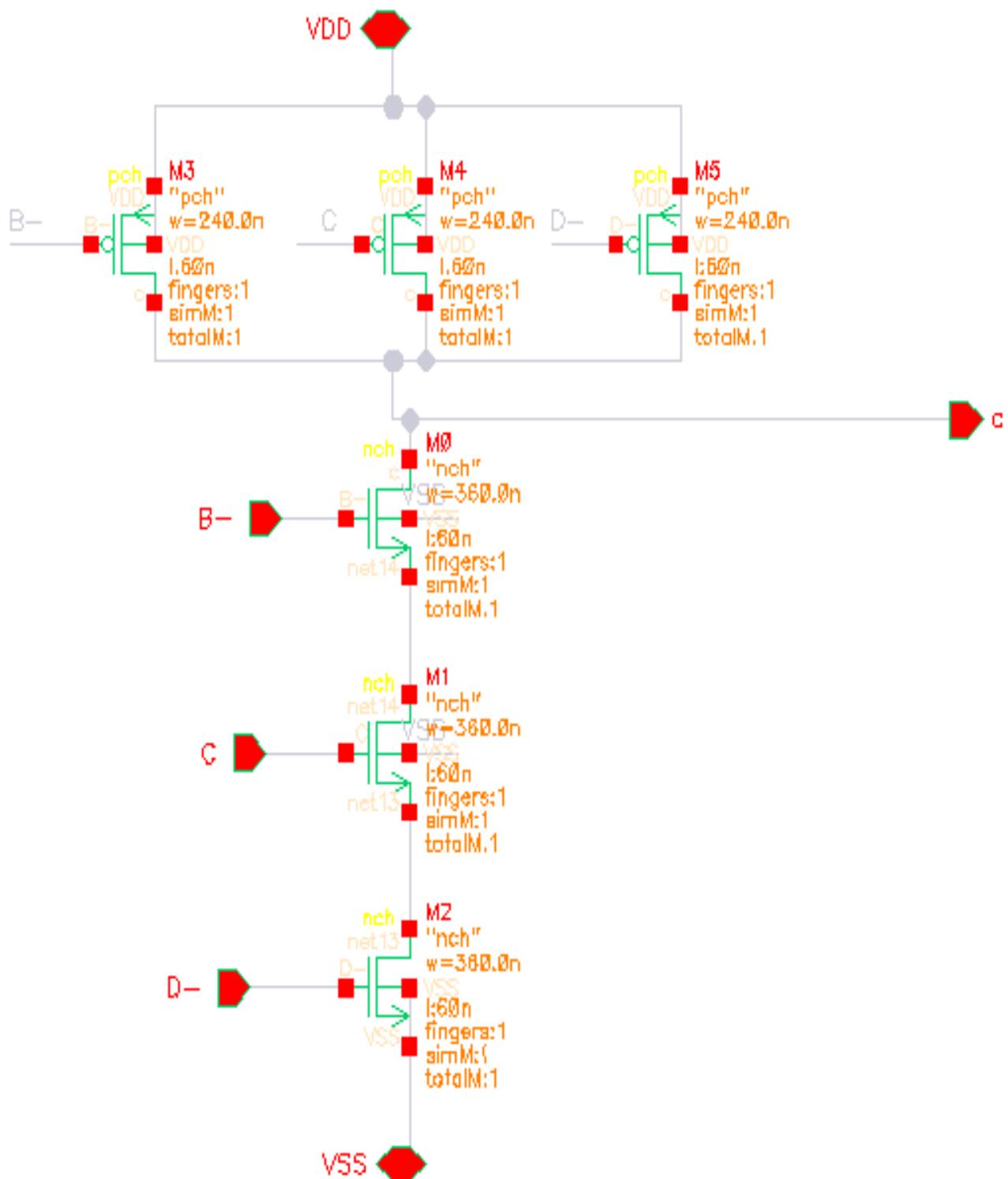
Wp=120n XX VS Wn=240n ✓✓

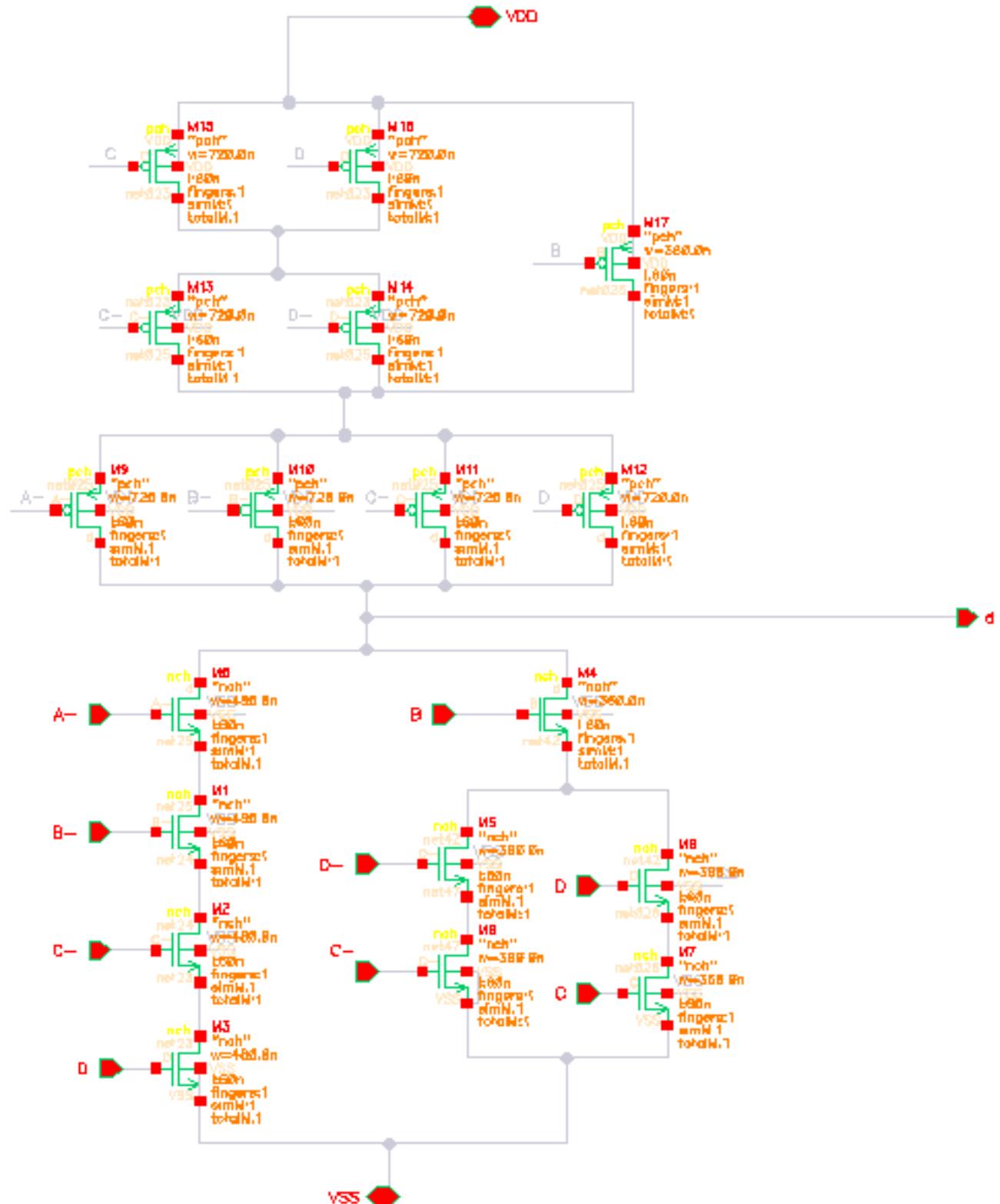


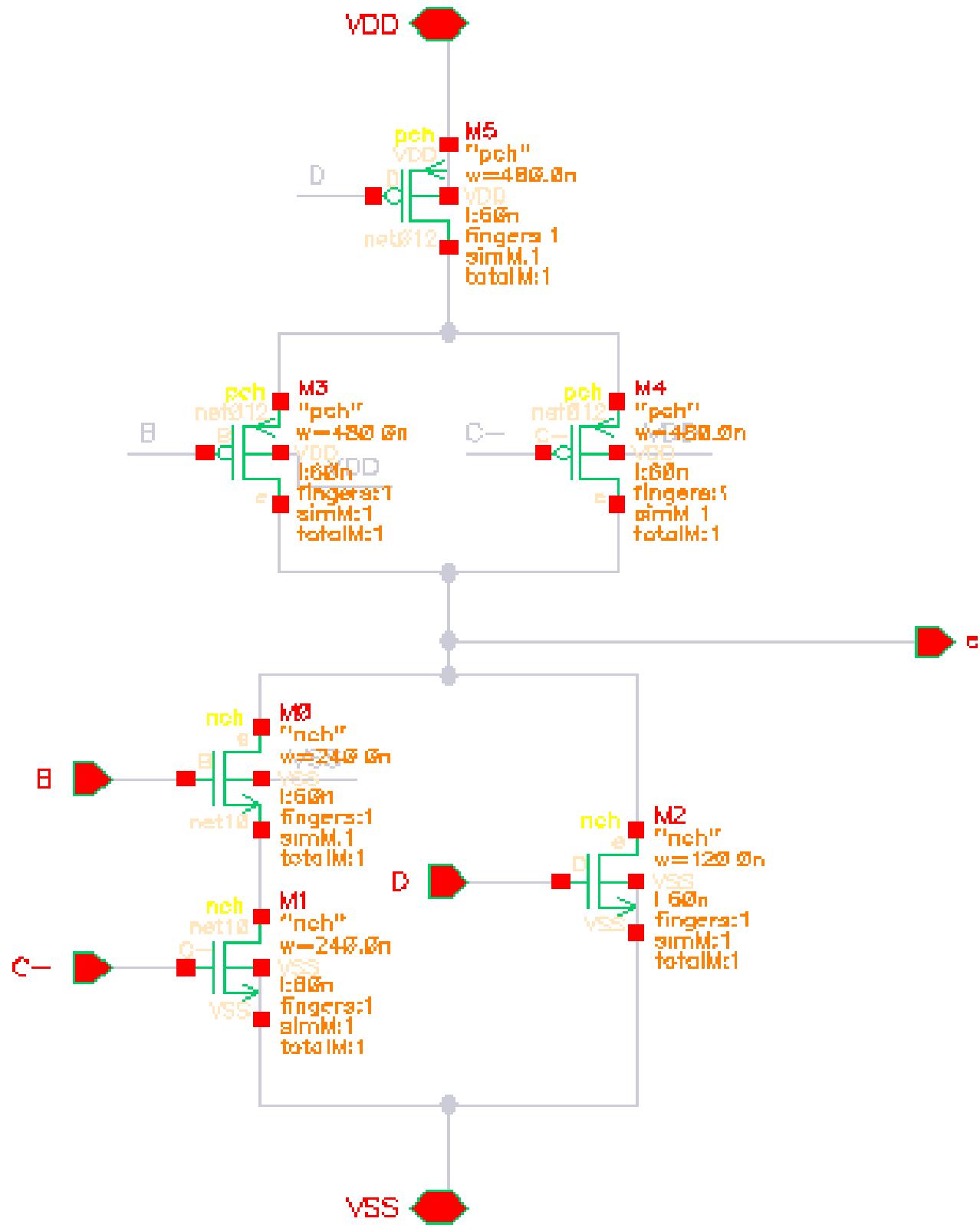
- Functions implementation after sizing:

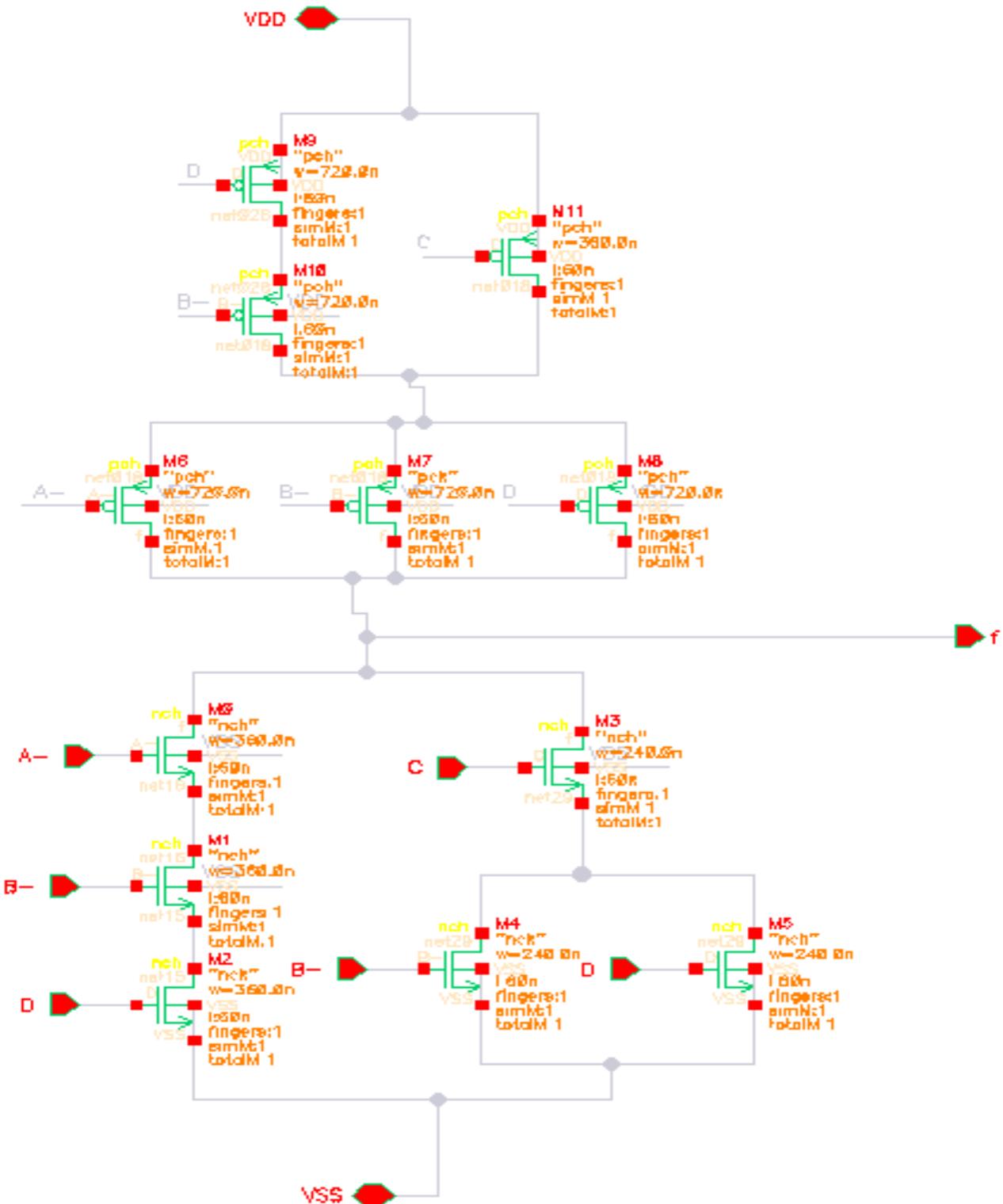


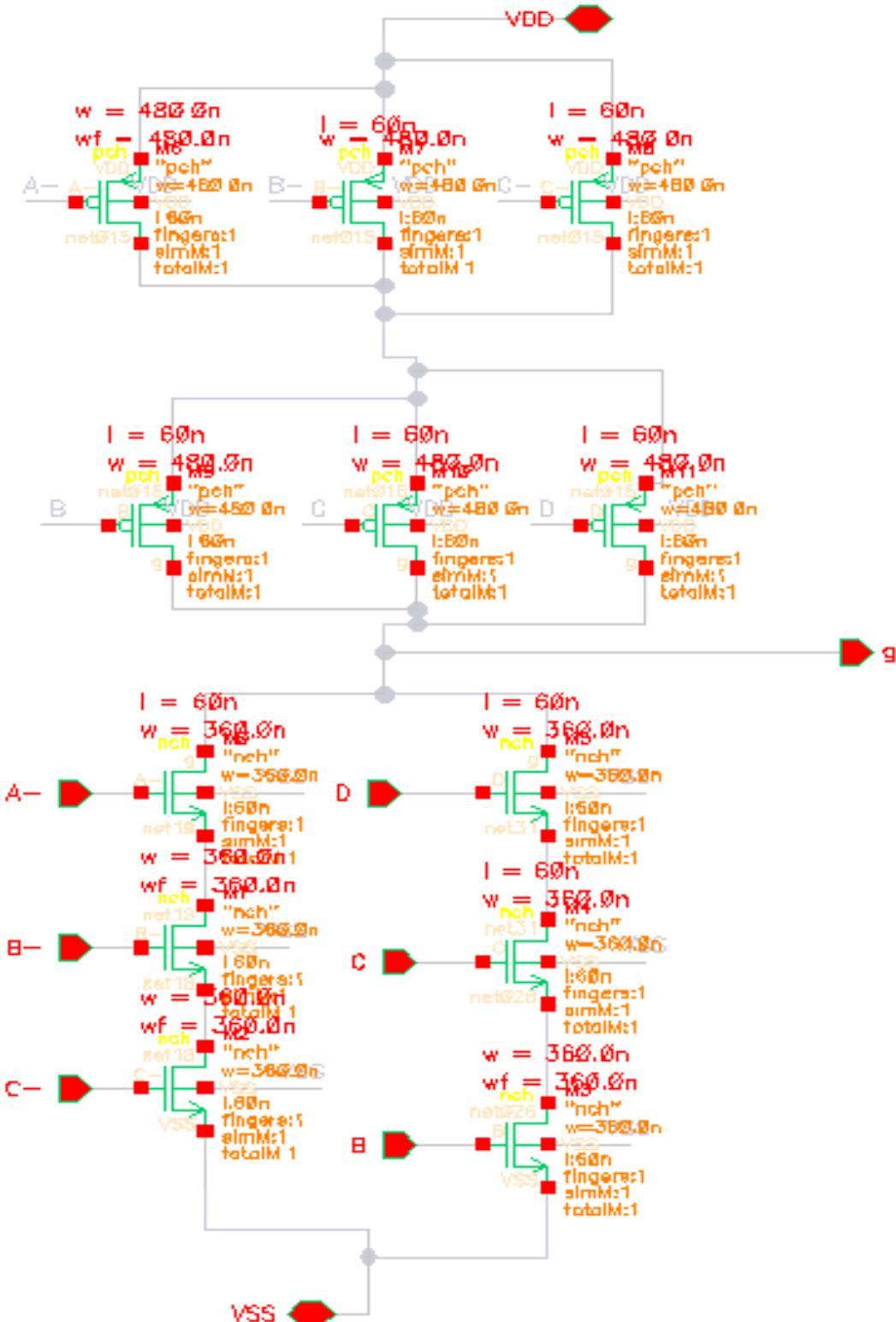










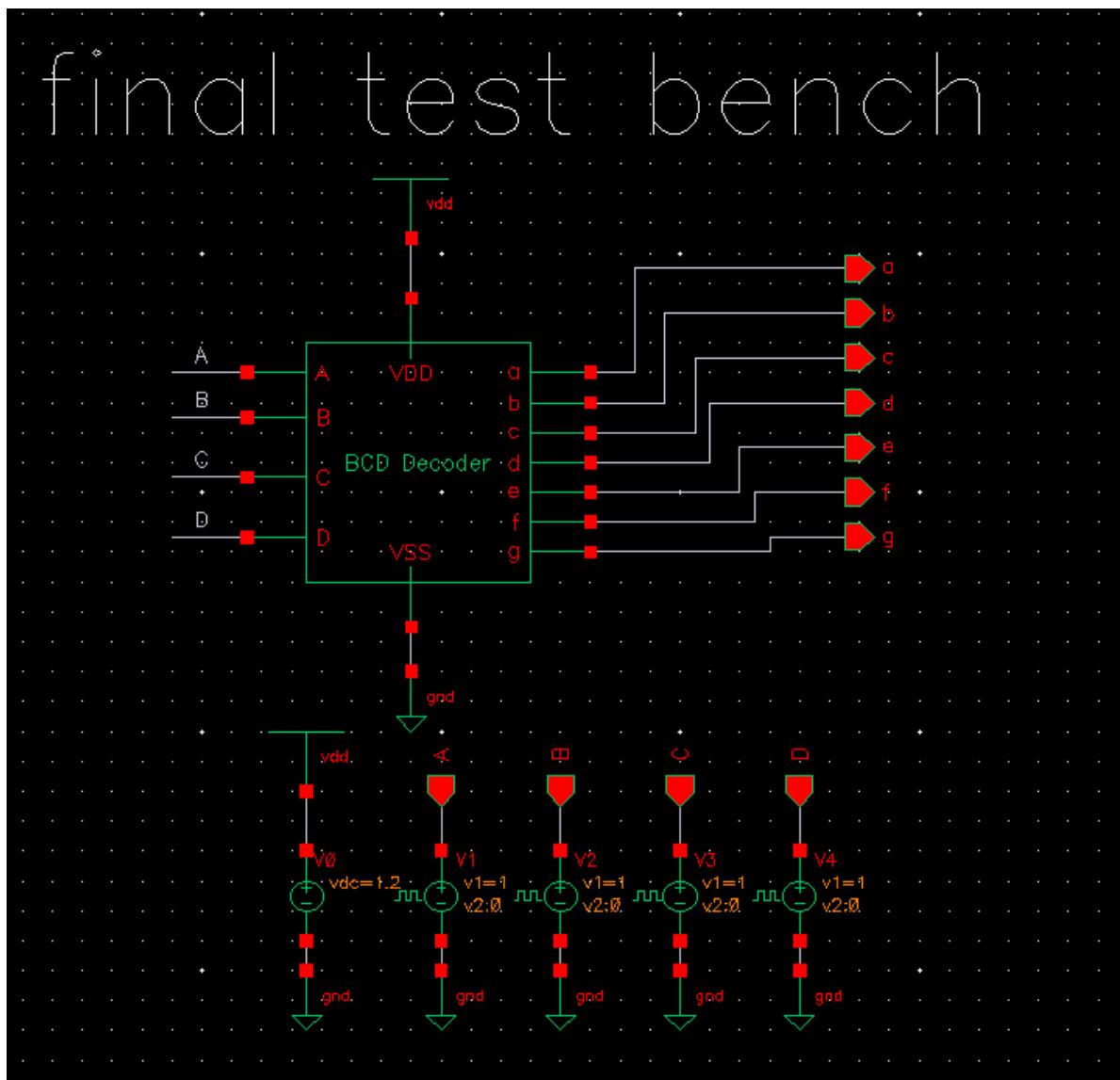


- **Final test bench:**

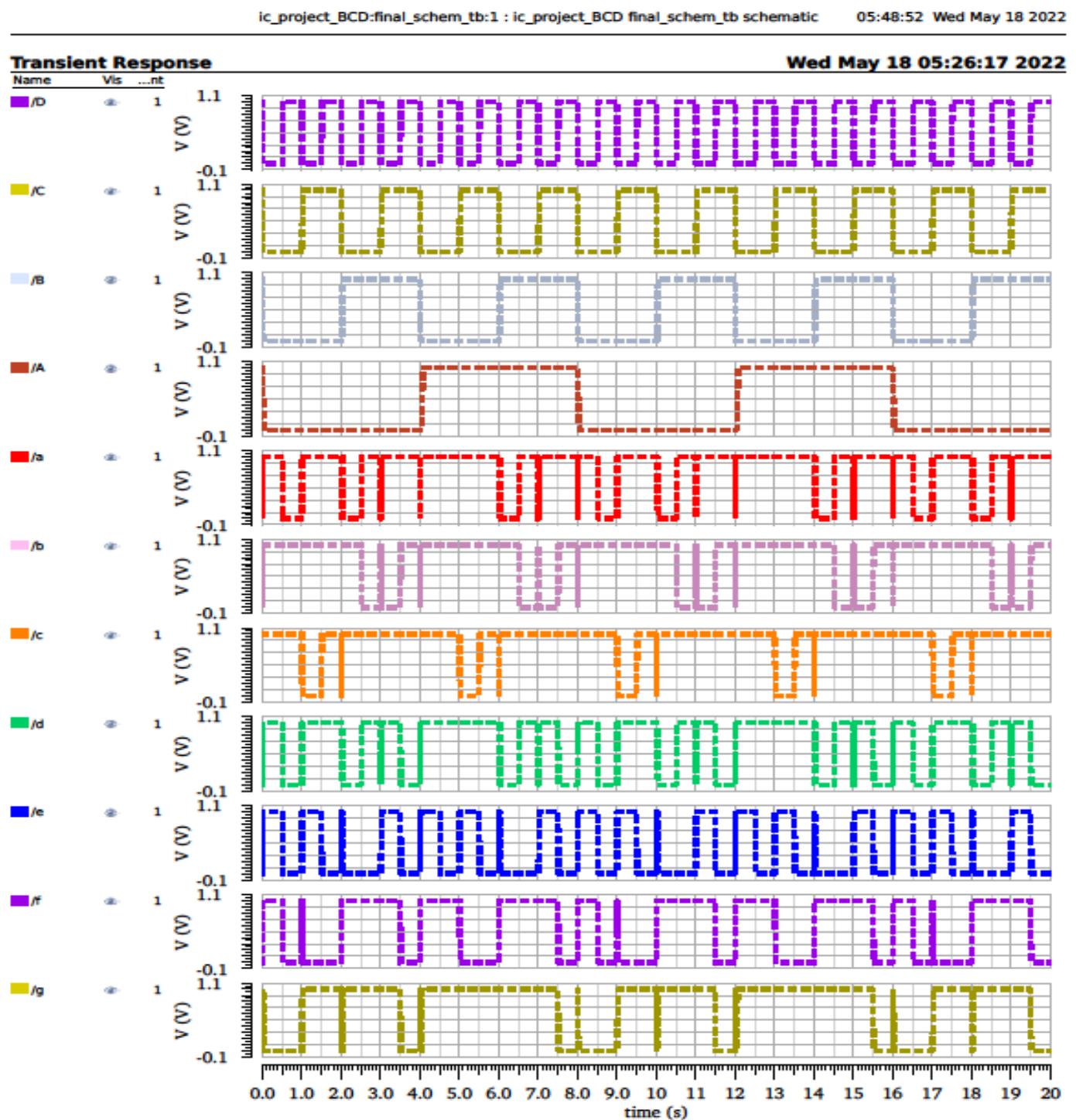
- Here we use

- $V_{dc} = 1.2V$  (according to technology used)
- $4 * V_{pulse}$ 
  - for D ( $v_1=0V ; v_2=1V$ ) -  $T_{pulse}=0.5$  sec  $T_{period} = 1$  sec
  - for C ( $v_1=0V ; v_2=1V$ ) -  $T_{pulse}=1$  sec  $T_{period} = 2$  sec
  - for B ( $v_1=0V ; v_2=1V$ ) -  $T_{pulse}=2$  sec  $T_{period} = 4$  sec
  - for A ( $v_1=0V ; v_2=1V$ ) -  $T_{pulse}=4$  sec  $T_{period} = 8$  sec

**Then RUN trans Simulation **20 seconds** & plot input verses the output!**

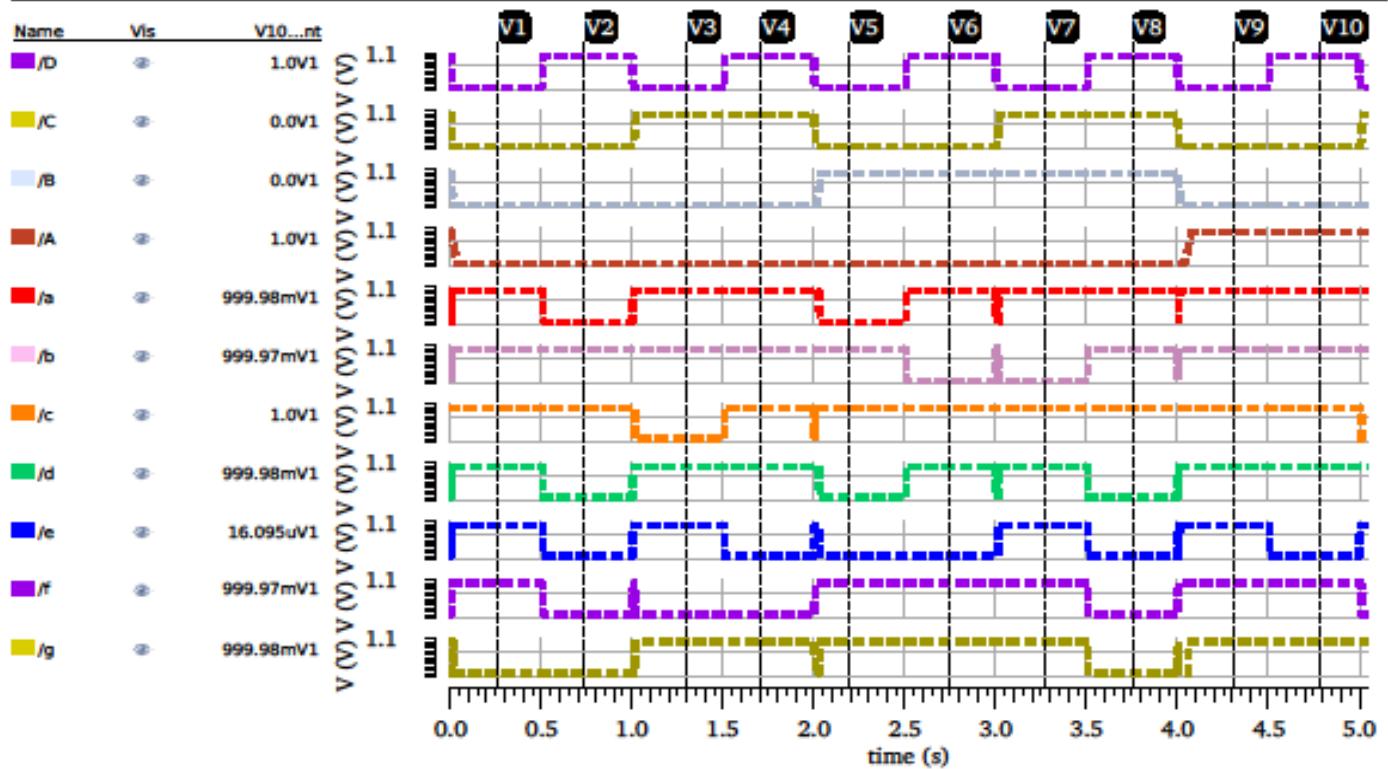


- **Run trans simulation for testing** : (CSV file s available on our drive)



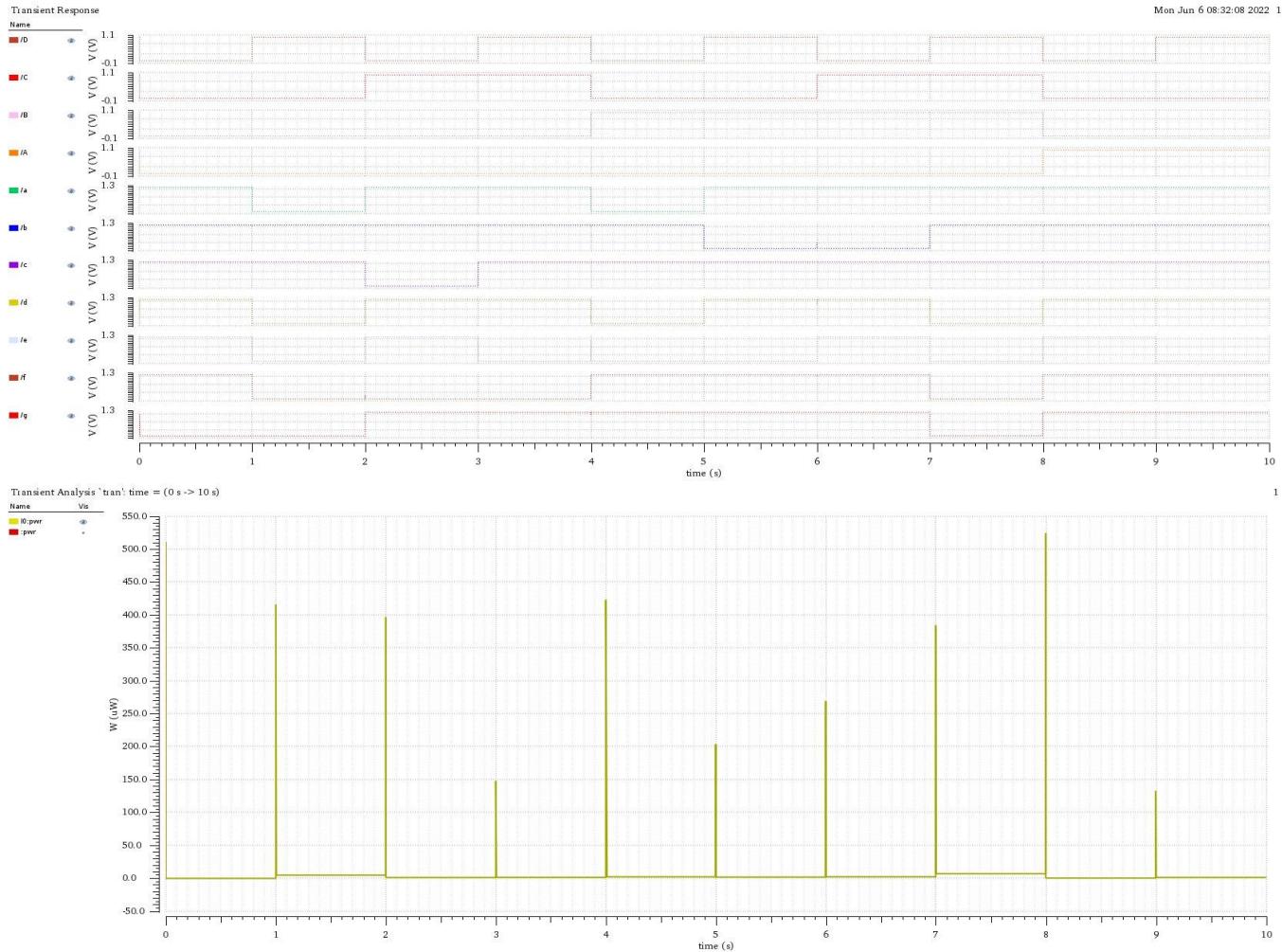
**Transient Response**

Wed May 18 05:26:17 2022

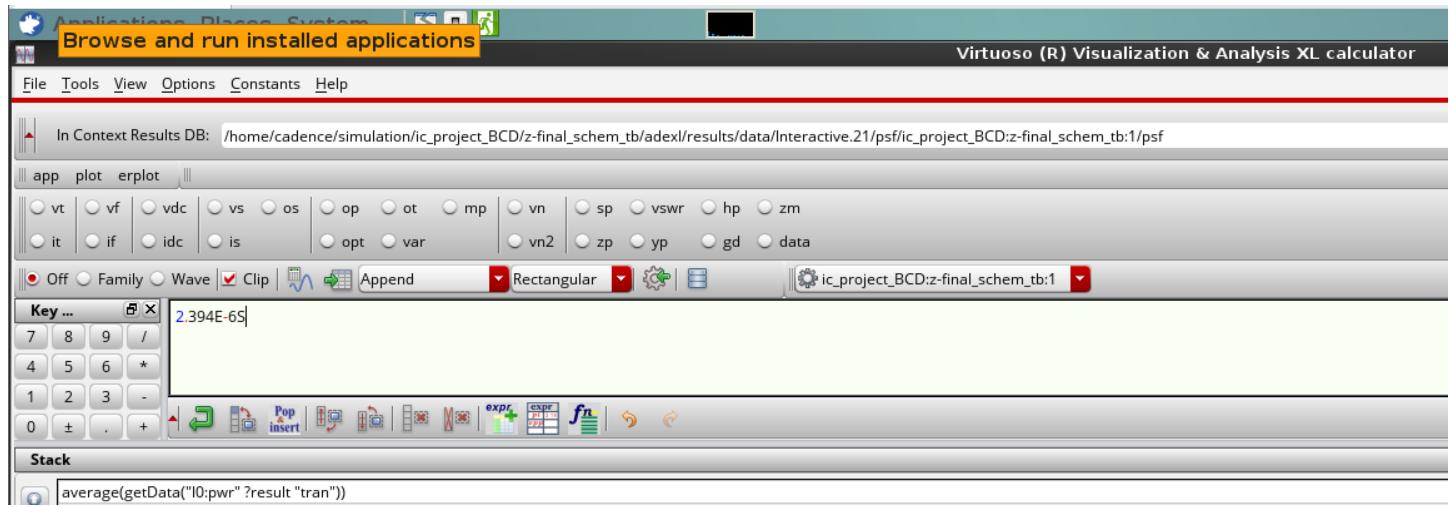
**Markers**

Design_Point	V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	
x /D		257.944ms	736.983ms	1.3s	1.70427s	2.19252s	2.73912s	3.27343s	3.75247s	4.31442s	4.78732s
/D	1	0.0V	1.0V	0.0V	1.0V	0.0V	1.0V	0.0V	1.0V	0.0V	1.0V
/C	1	0.0V	0.0V	1.0V	1.0V	0.0V	0.0V	1.0V	1.0V	0.0V	0.0V
/B	1	0.0V	0.0V	0.0V	0.0V	1.0V	1.0V	1.0V	1.0V	0.0V	0.0V
/A	1	0.0V	0.0V	0.0V	0.0V	0.0V	0.0V	0.0V	1.0V	1.0V	1.0V
/a	1	1.0V	74.95uV	1.0V	1.0V	53.75uV	1.0V	1.0V	1.0V	1.0V	1.0V
/b	1	1.0V	1.0V	1.0V	1.0V	1.0V	43.04uV	52.02uV	1.0V	1.0V	1.0V
/c	1	1.0V	1.0V	33.4uV	1.0V						
/d	1	1.0V	130.1uV	1.0V	1.0V	78.2uV	1.0V	1.0V	72.89uV	1.0V	1.0V
/e	1	1.0V	16.01uV	1.0V	14.13uV	38.72uV	4.645uV	1.0V	19.99uV	1.0V	16.09uV
/f	1	1.0V	95.17uV	53.17uV	9.411uV	1.0V	1.0V	1.0V	46.09uV	1.0V	1.0V
/g	1	61.34uV	61.37uV	1.0V	1.0V	1.0V	1.0V	55.26uV	1.0V	1.0V	

## Total power consumption:

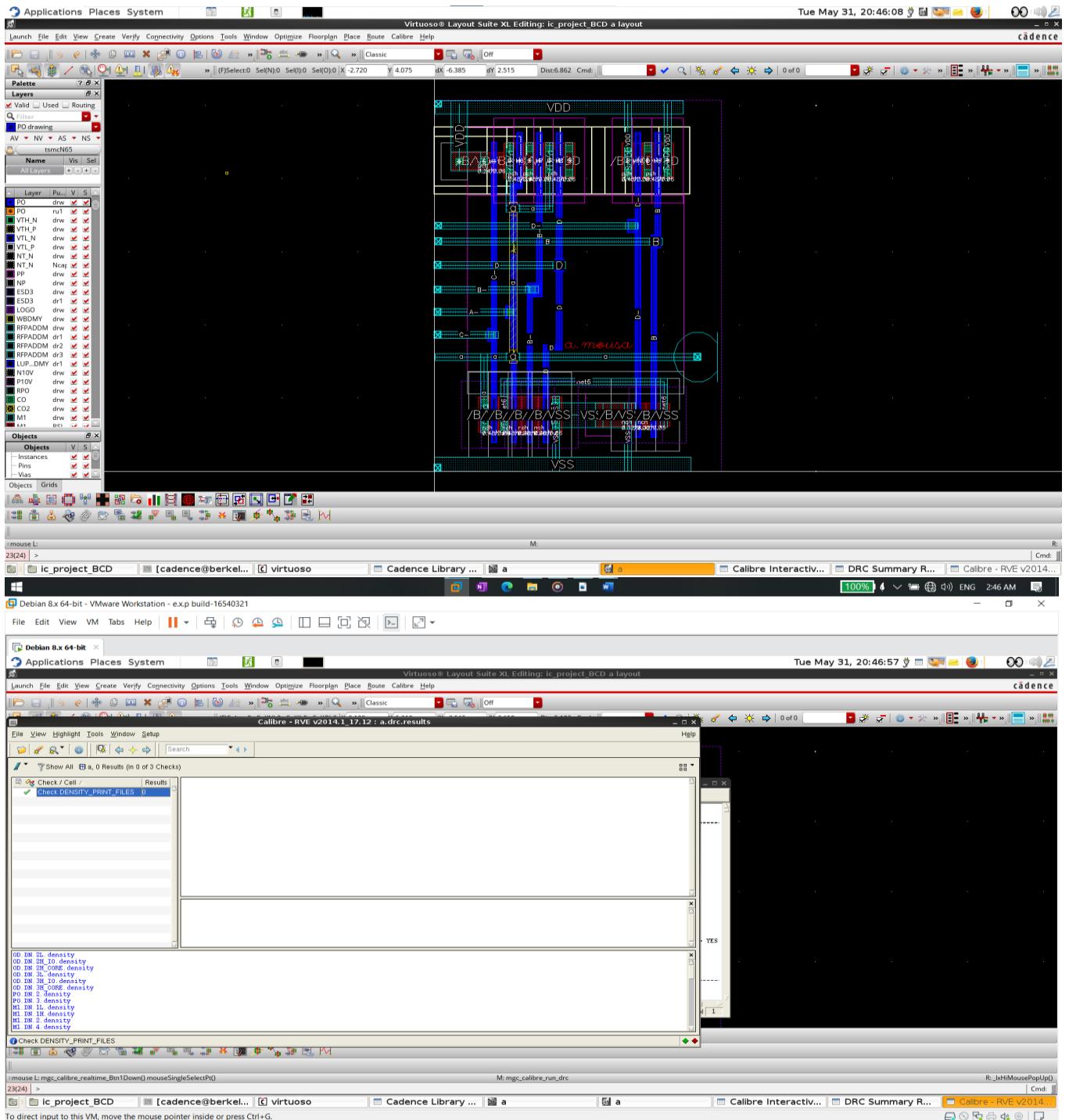


## Average:

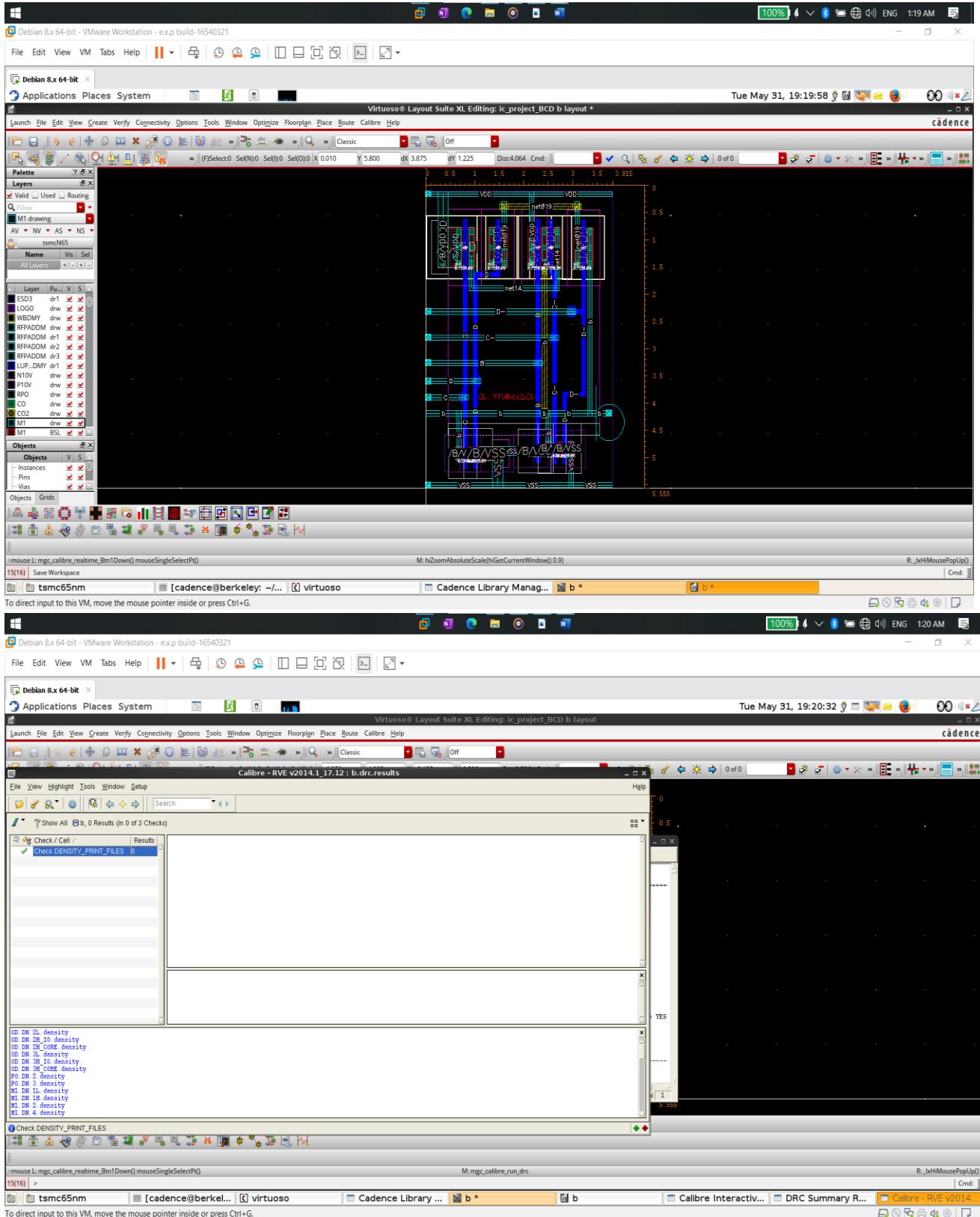


## LAYOUT:

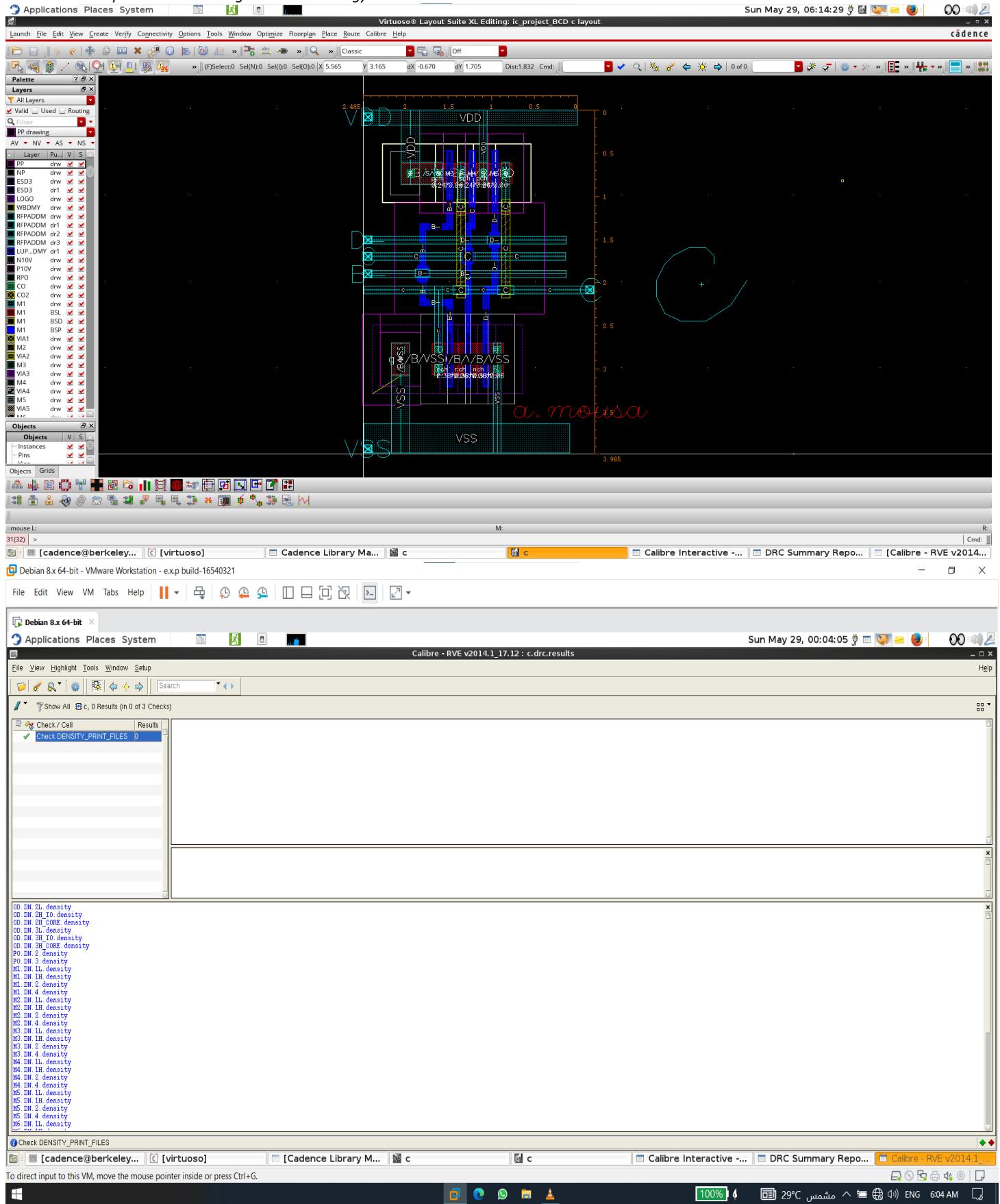
As mentioned before the project is to be divided into 7 blocks to simplify the job of building the whole Ic layout !



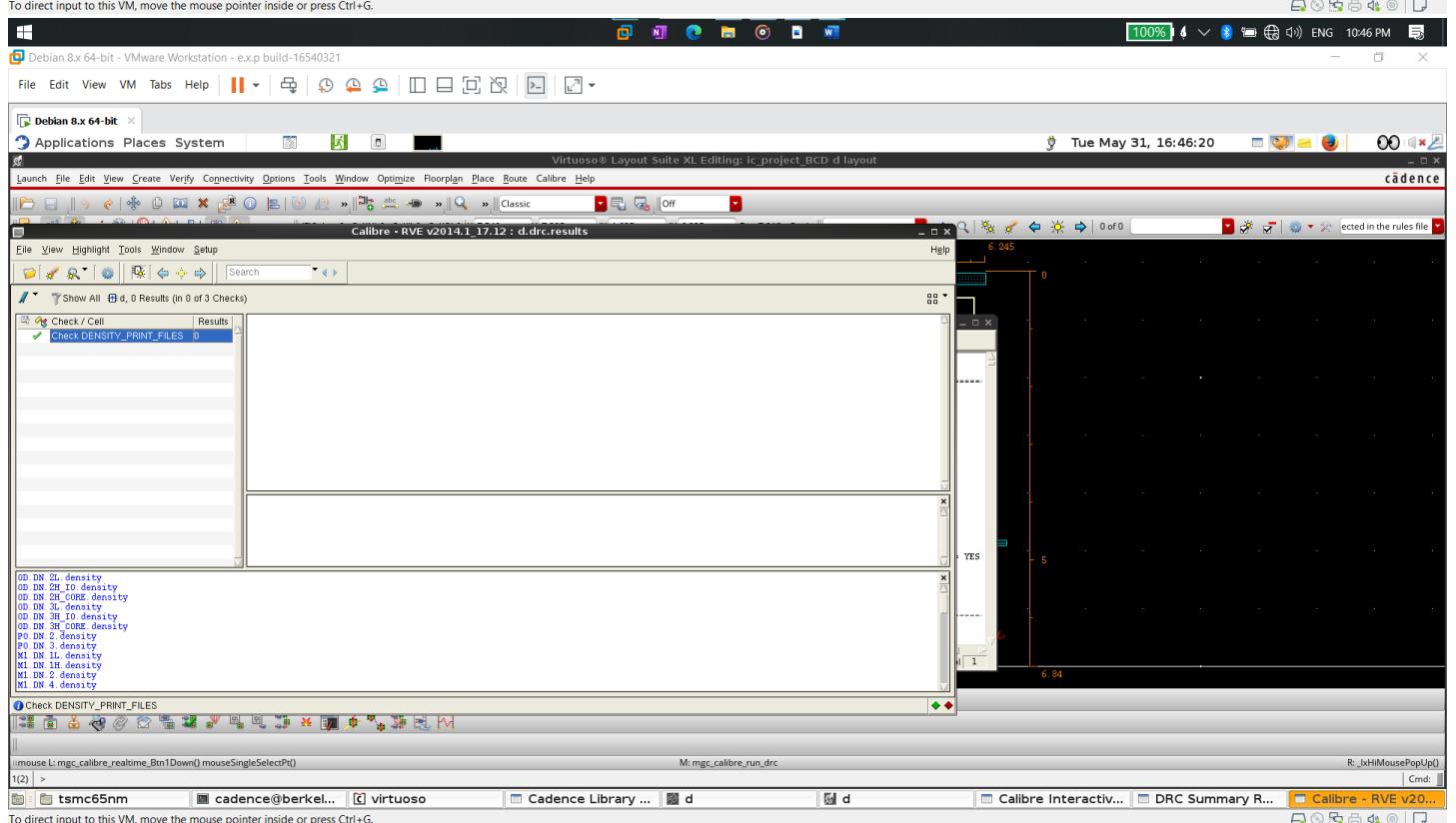
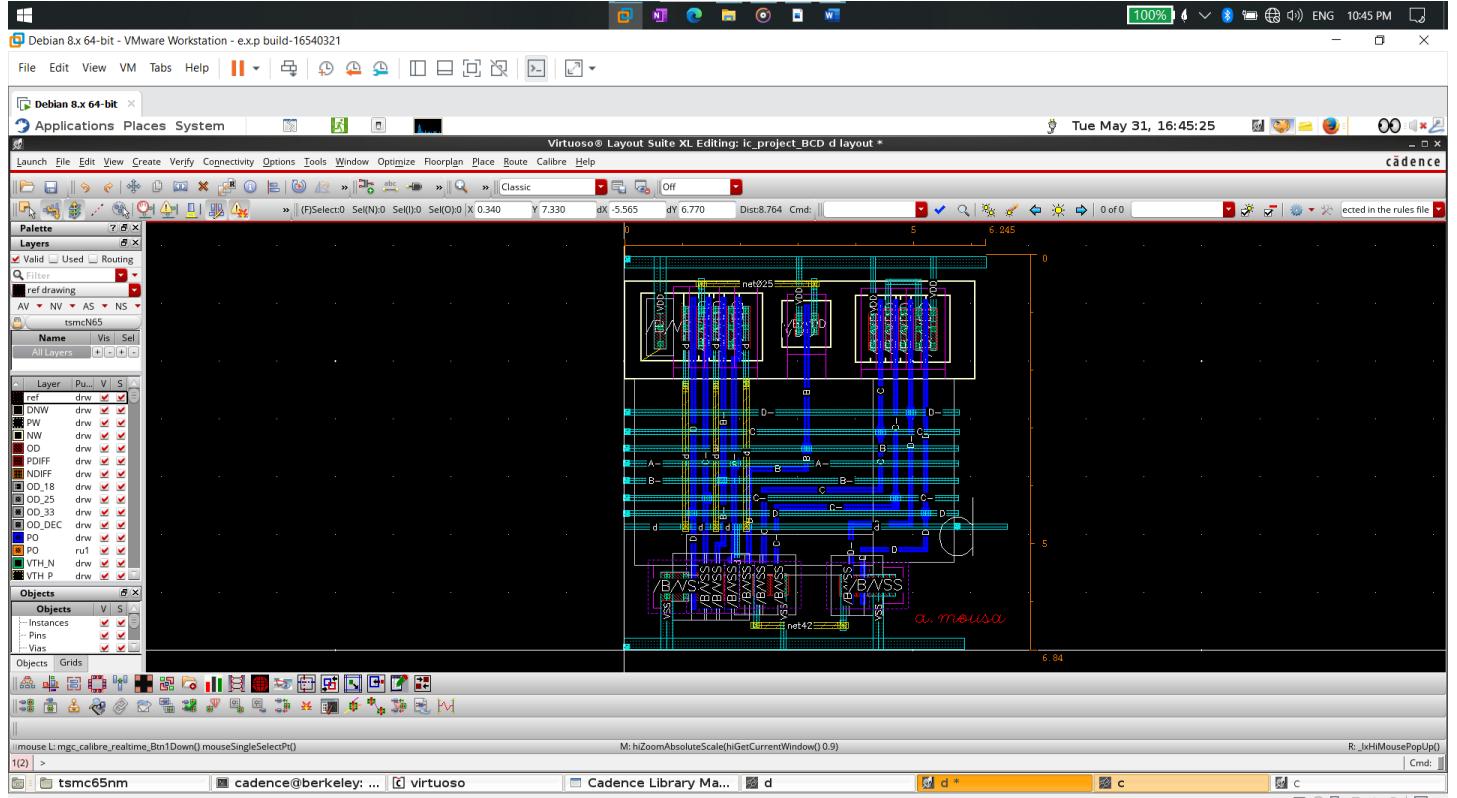
## BCD Decoder Implementation Using CMOS Technology



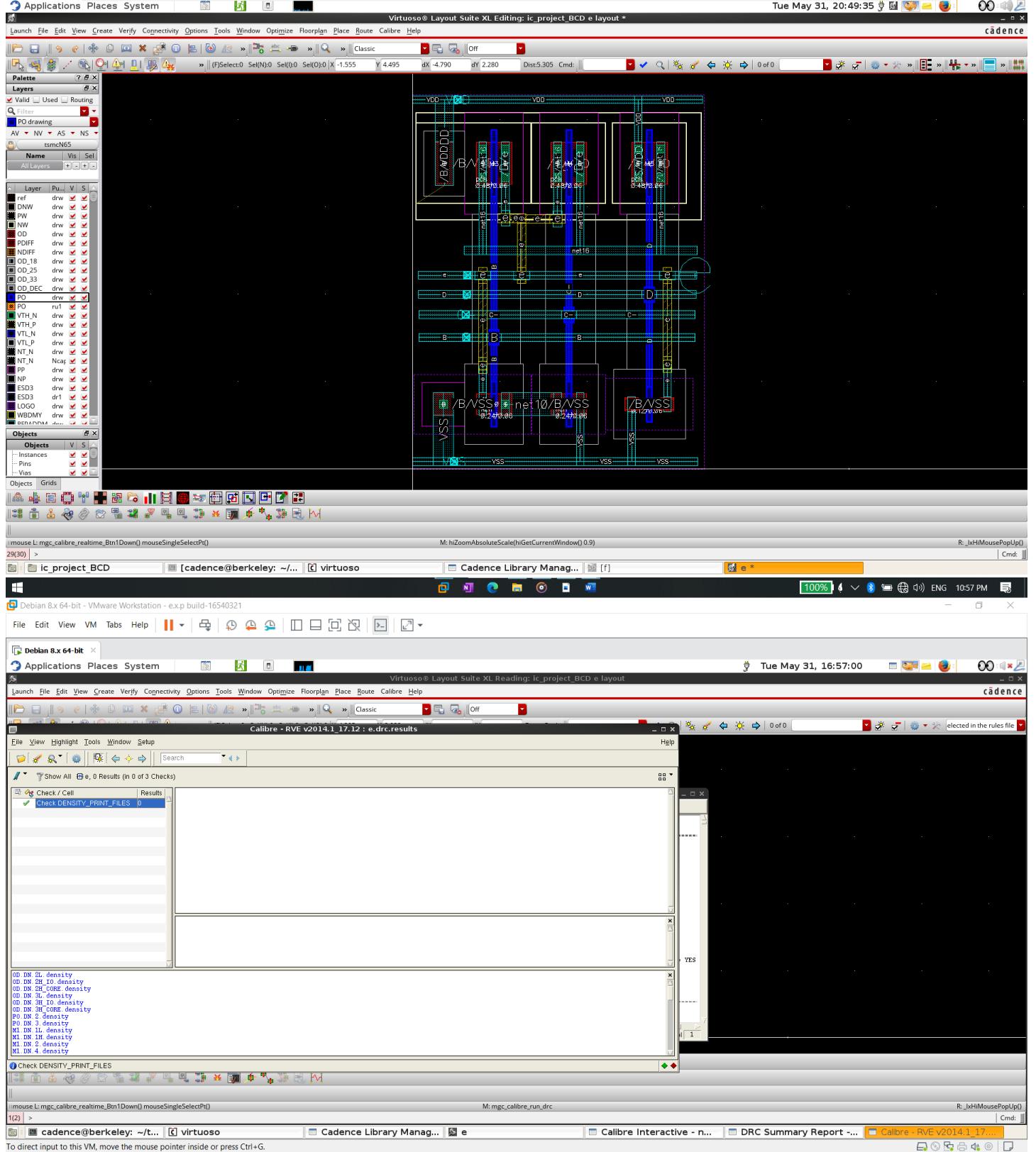
## BCD Decoder Implementation Using CMOS Technology



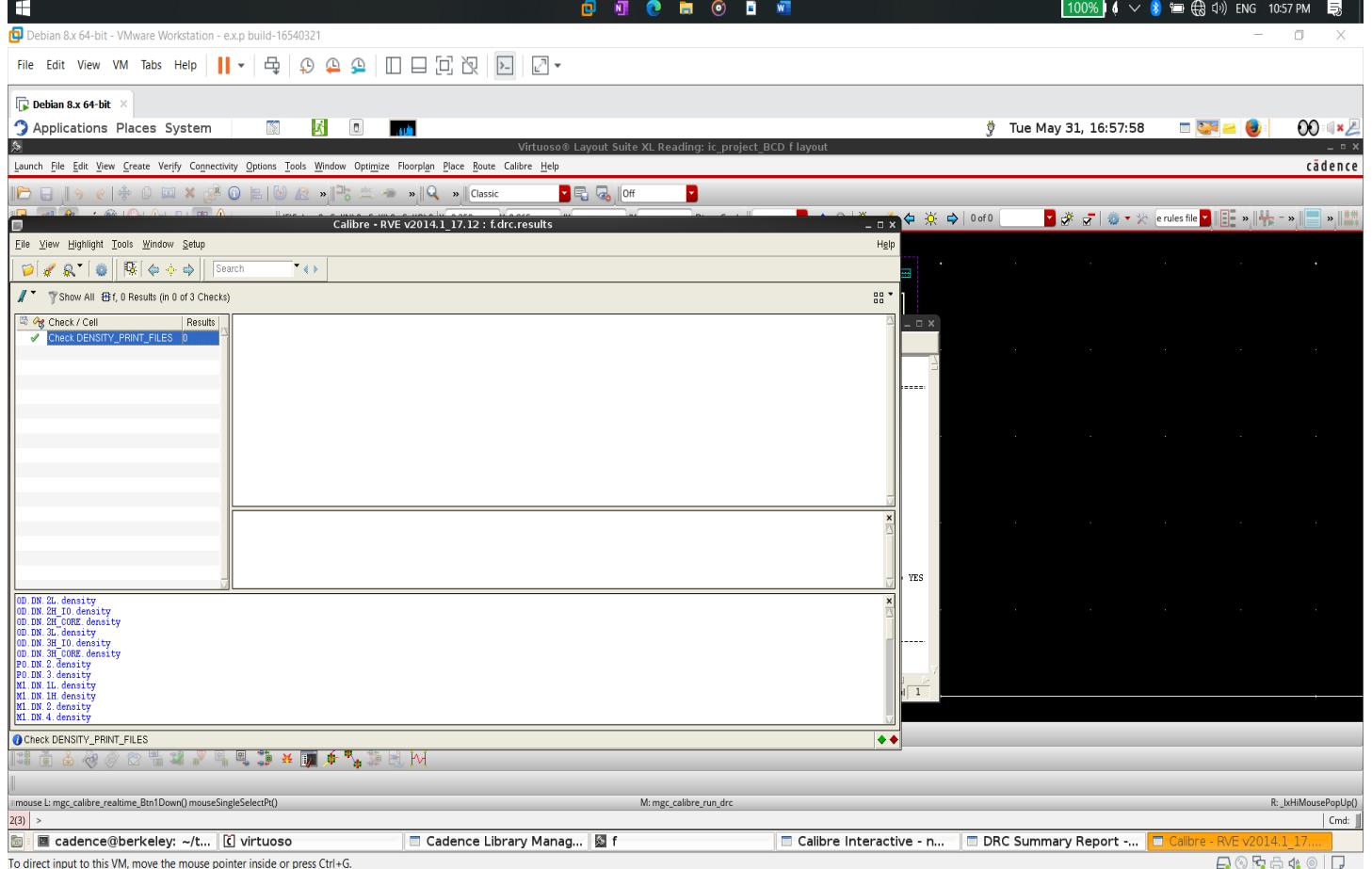
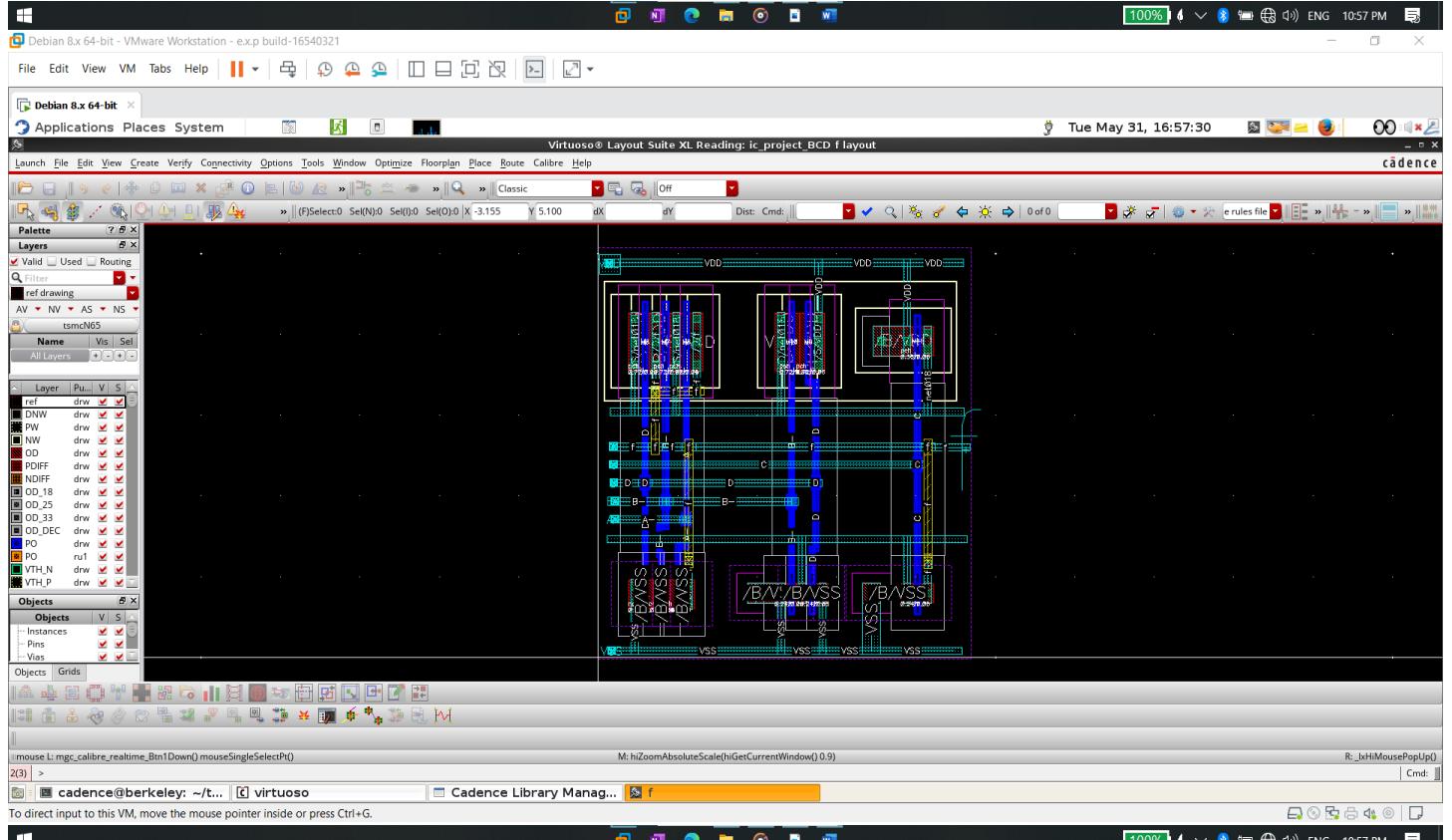
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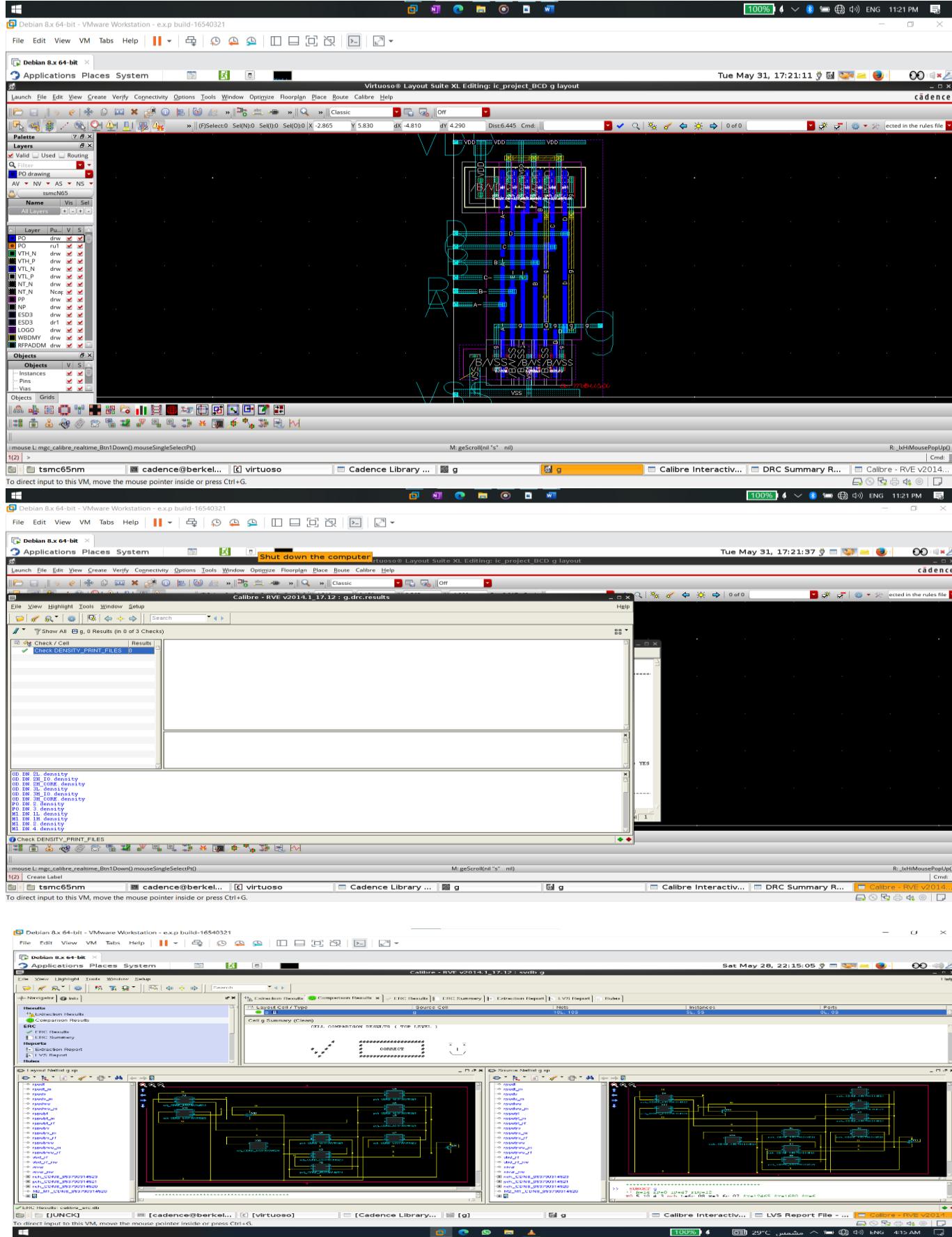
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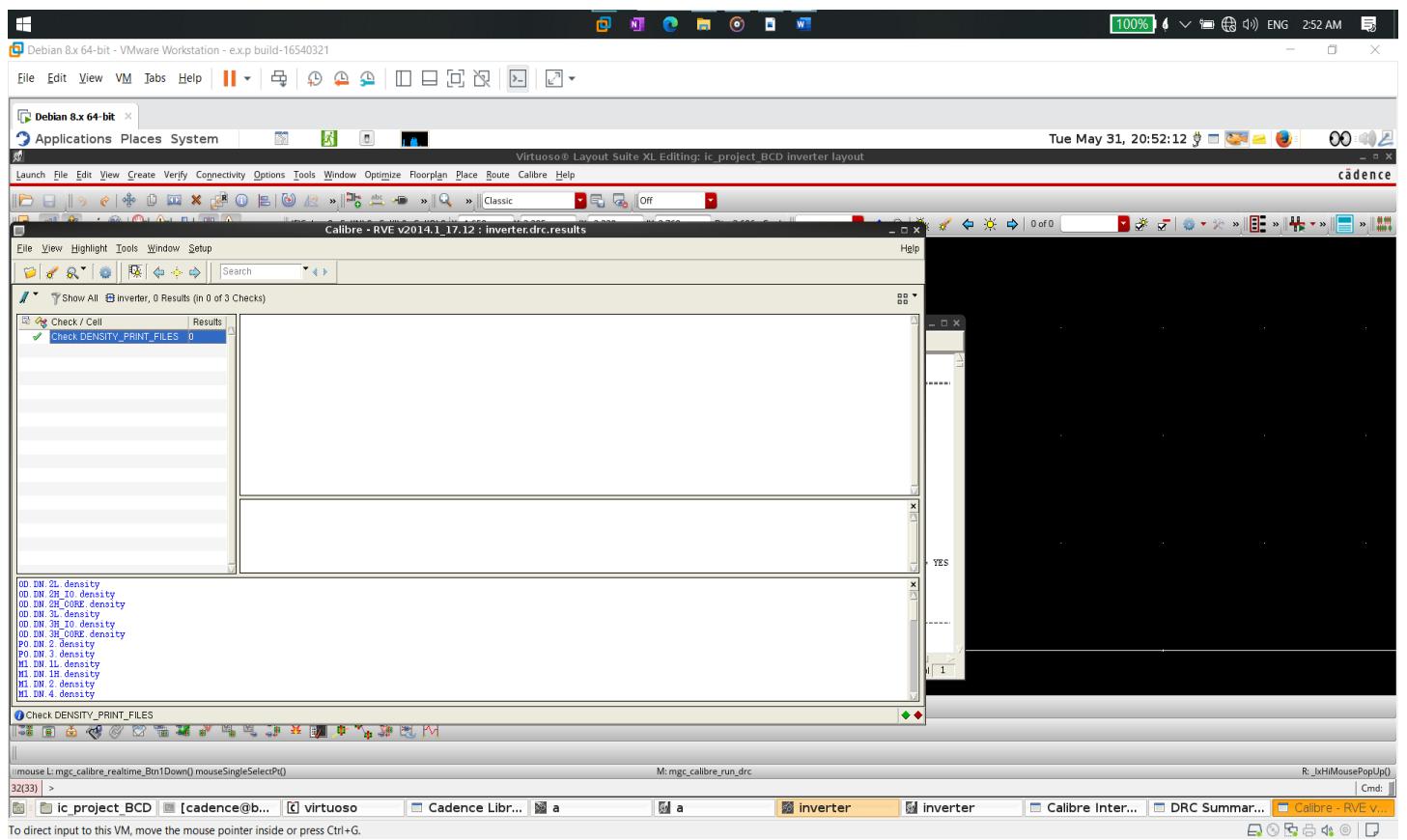
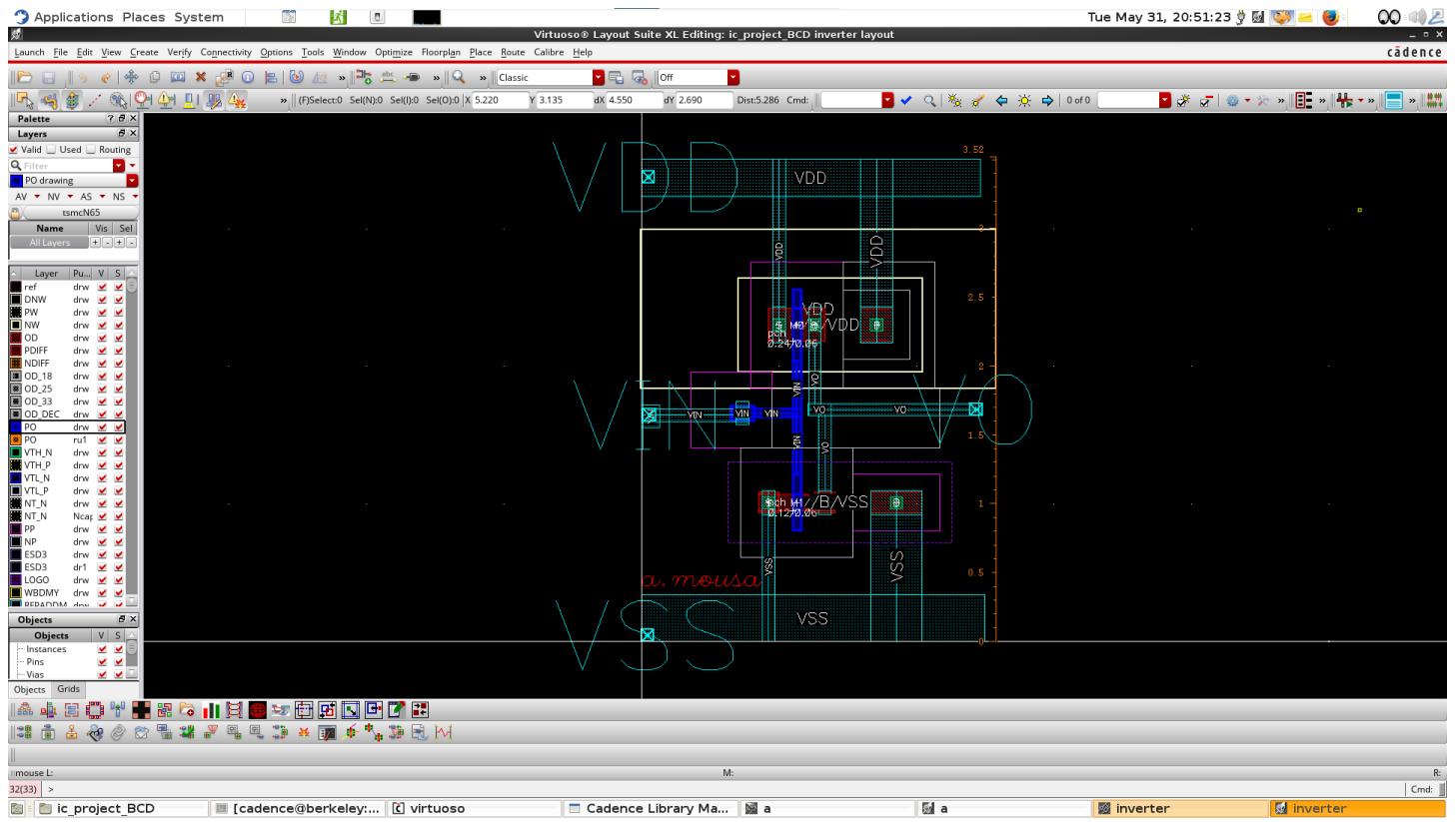


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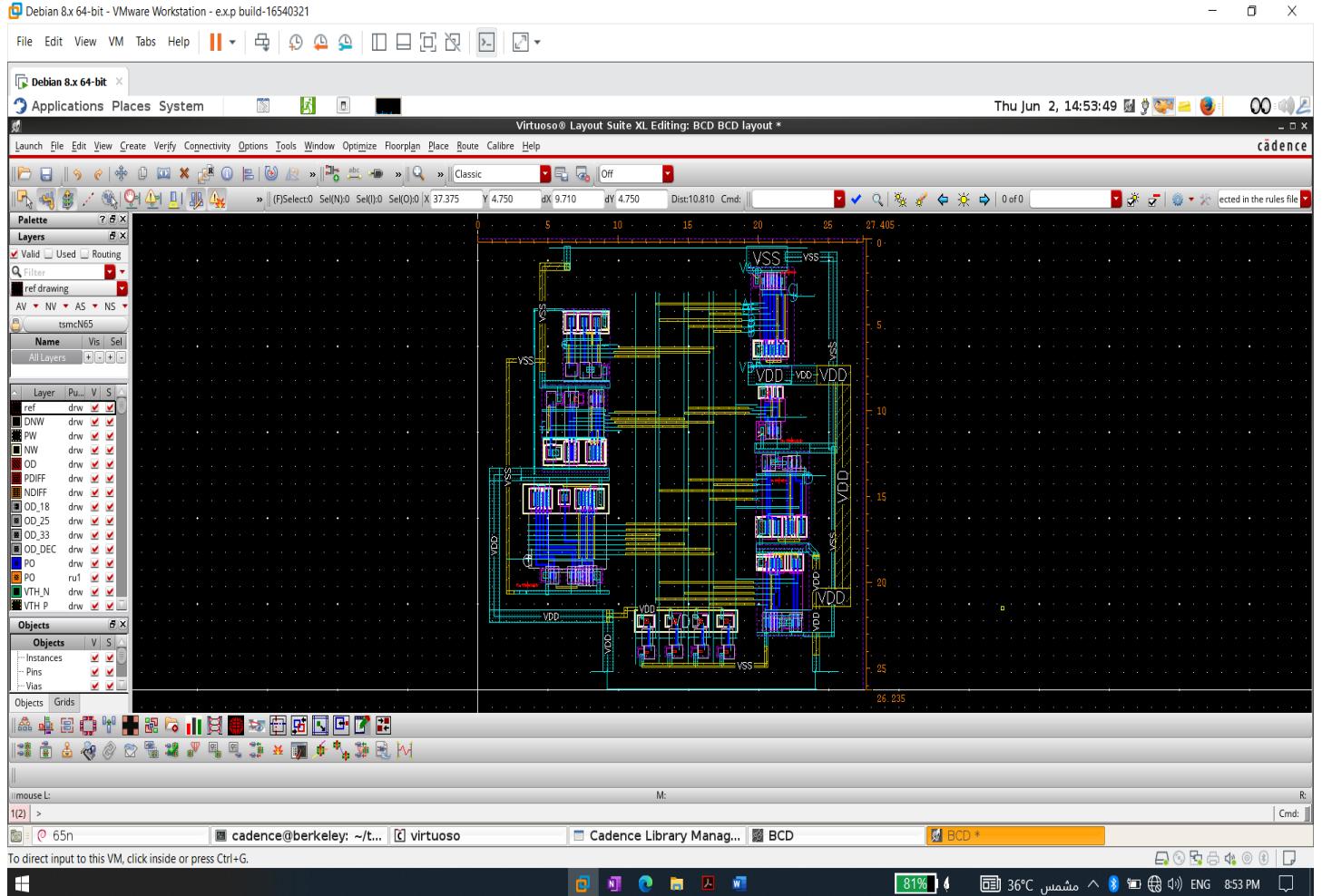


## BCD Decoder Implementation Using CMOS Technology

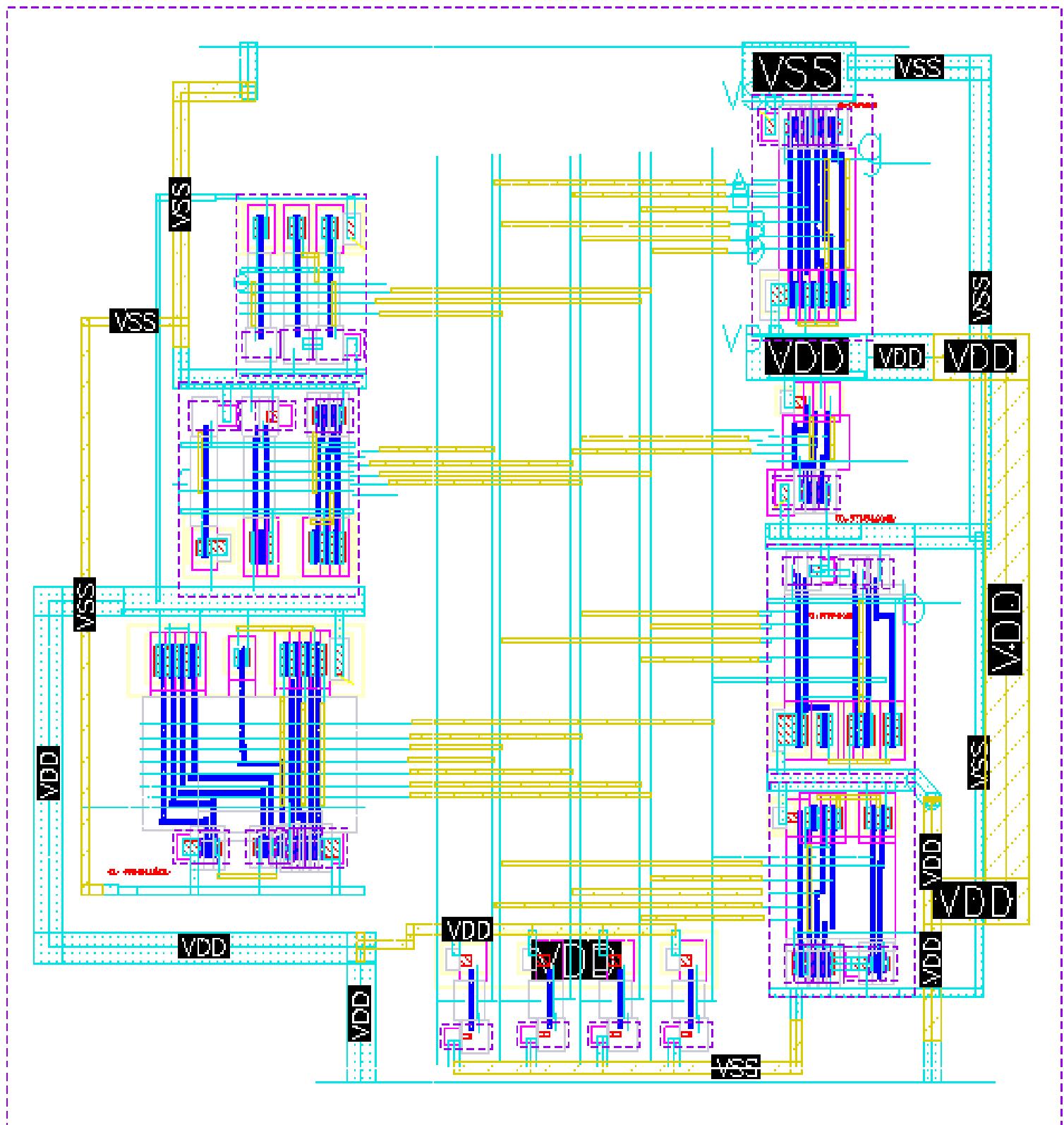
### inverter :



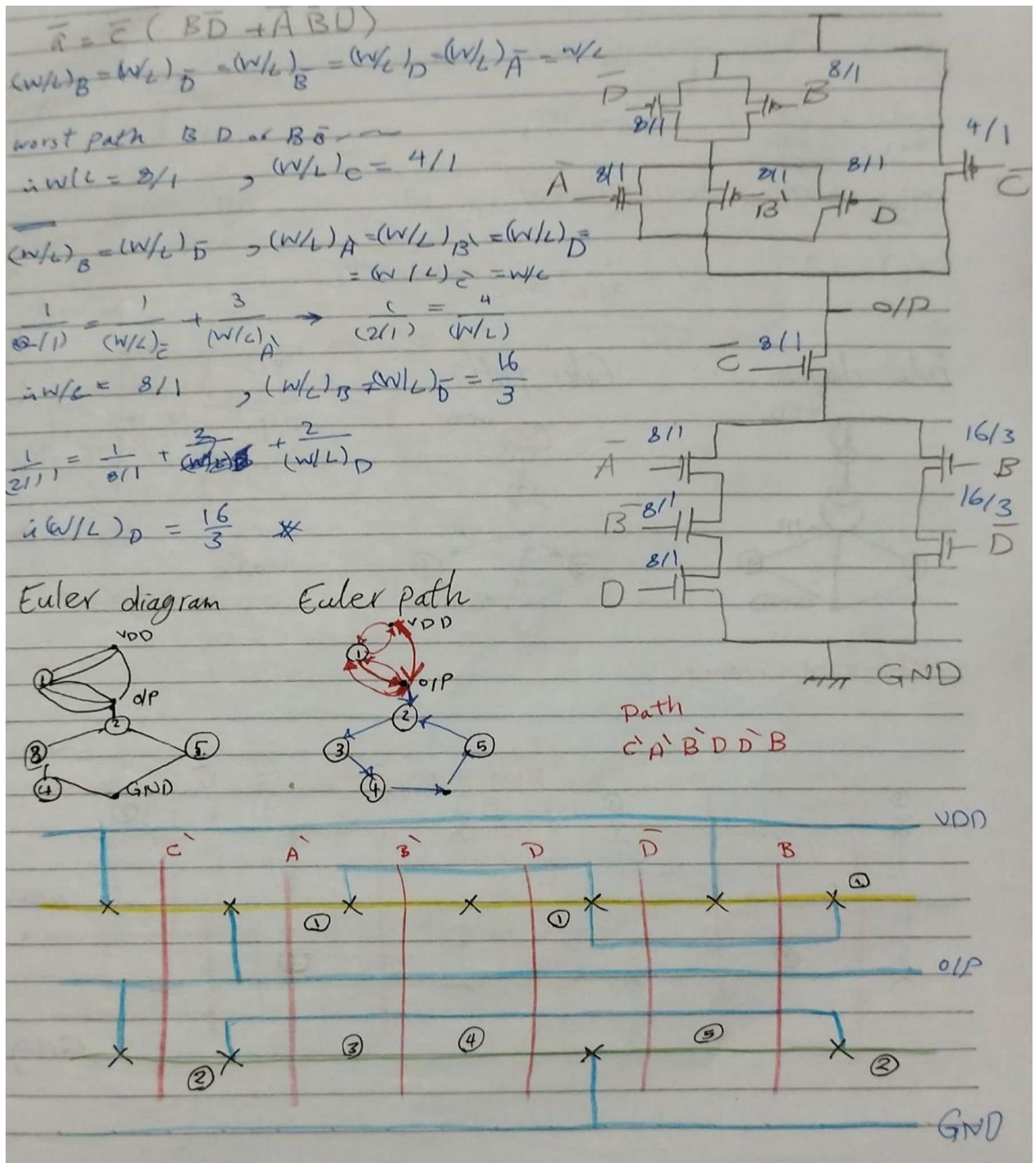
- Full IC Layout :



Final area used was around .. (27.4\*26.2) um

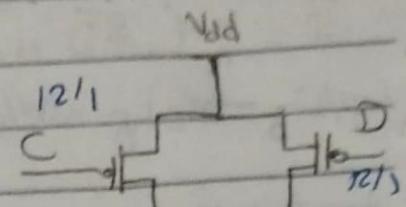


- Hand-Written draft: (stick diagram & sizing)



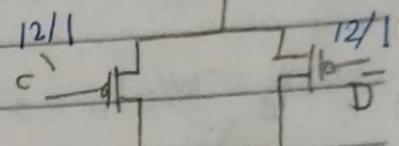
$$b = B \cdot (\bar{C} + \bar{D}) \cdot (C + D)$$

$$(W/L)_C = (W/L)_B = (W/L)_{\bar{C}} = (W/L)_{\bar{D}} = W/L$$

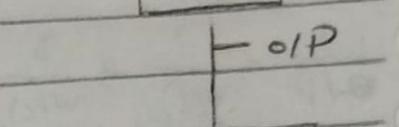


$$\frac{1}{4/1} = \frac{3}{W/L} \quad \therefore W/L = 12/1$$

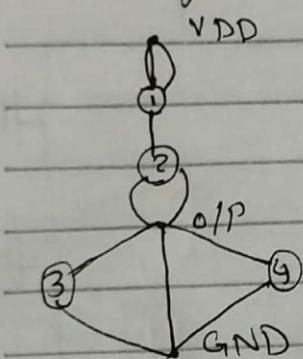
$$(W/L)_C = (W/L)_D = (W/L)_{\bar{C}} = (W/L)_{\bar{D}} = W/L$$



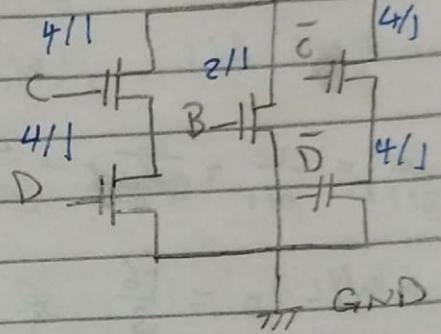
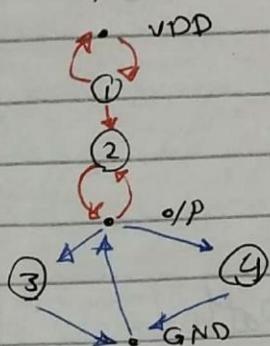
$$(W/L)_B = 2/1 \quad \frac{1}{2/1} = \frac{2}{W/L} \Rightarrow W/L = 4/1$$



Euler diagram

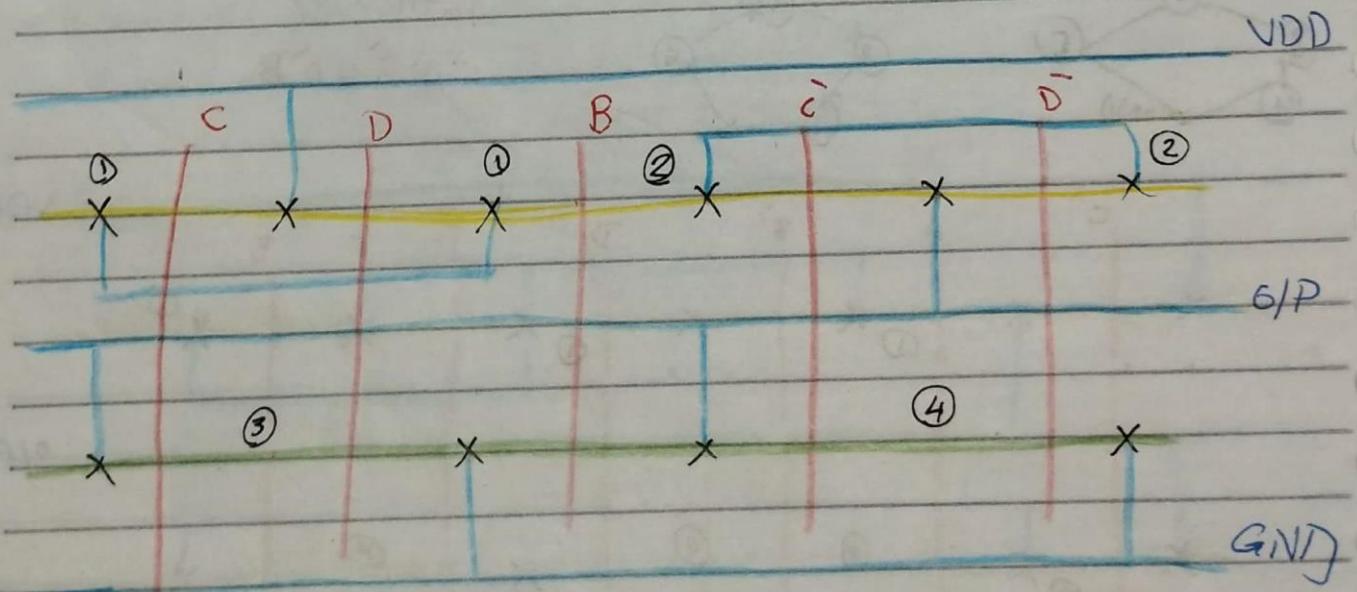


Euler Path.



path  
CD B̄ C̄ D̄

Stick diagram:-



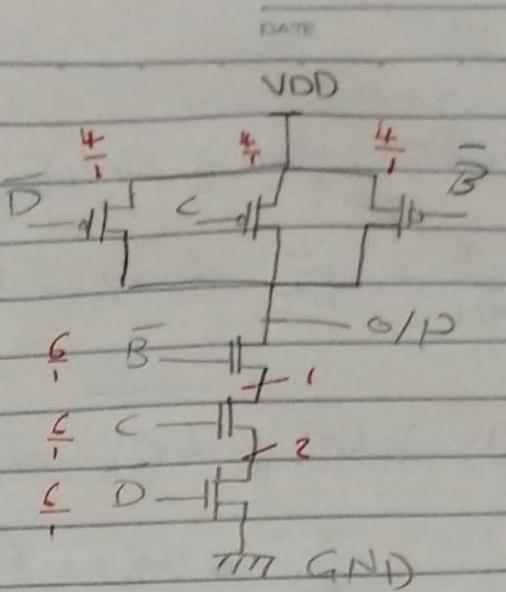
$\bar{C} = \bar{B} \bar{C} \bar{D}$

$$(w/L)_{\bar{D}} - (w/L)_C - (w/L)_{\bar{B}} - (w/L)_{\bar{D}} = \frac{4}{7}$$

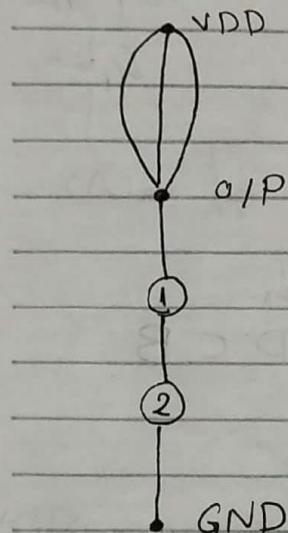
$$\frac{1}{(w/L)_W} = \frac{1}{(w/L)_{\bar{B}}} + \frac{1}{(w/L)_C} + \frac{1}{(w/L)_{\bar{D}}}$$

$$\Rightarrow (w/L)_{\bar{B}} = (w/L)_C = (w/L)_{\bar{D}} = (w/L)$$

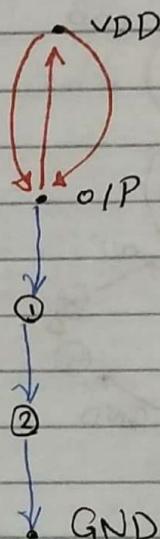
$$\therefore \frac{1}{2/1} = \frac{3}{(w/L)} \Rightarrow (w/L) = \frac{6}{1}$$



Euler diagram

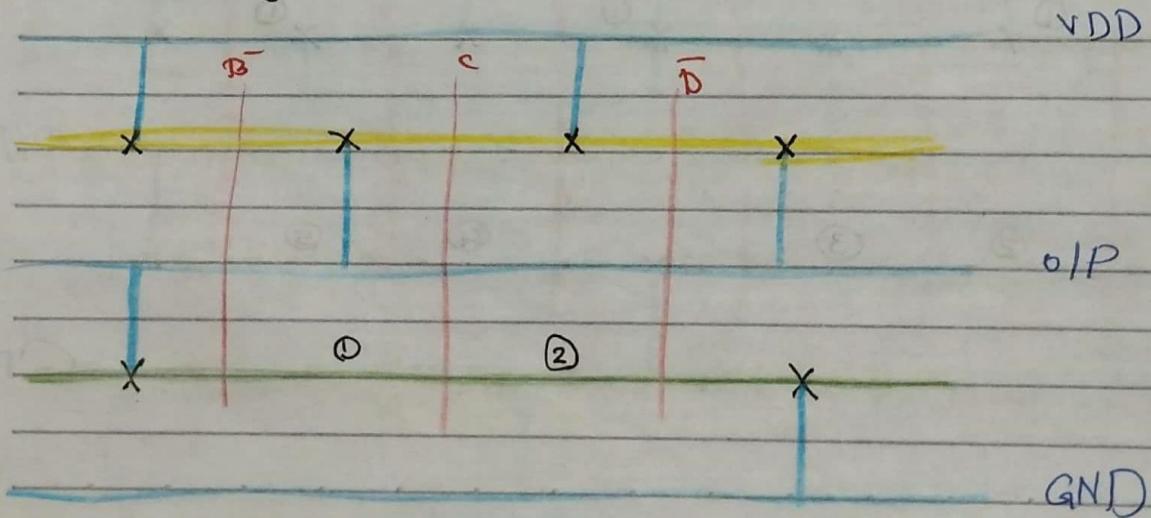


Euler Path



Path  
 $\bar{B} C \bar{D}$

Stick diagram

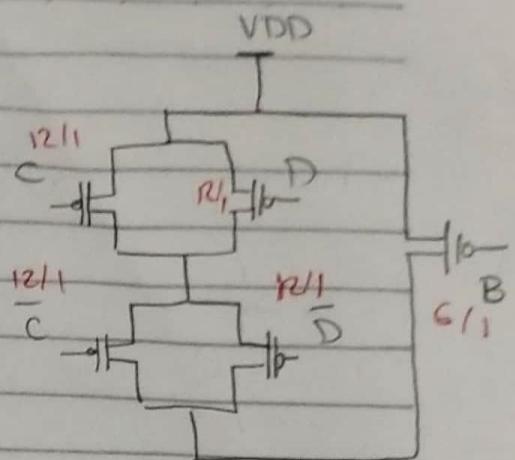


$$d = \bar{A}\bar{B}\bar{C}D + B(CD + \bar{C}\bar{D})$$

$$(W/L)_C = (W/L)_D = (W/L)_{\bar{C}} = (W/L)_{\bar{D}}$$

$$= (W/L)_A = (W/L)_B = (W/L)_{\bar{A}} = (W/L)_{\bar{B}} = W/L$$

$$\frac{1}{w/l} = \frac{3}{w/l} \Rightarrow W/L = 12/1$$

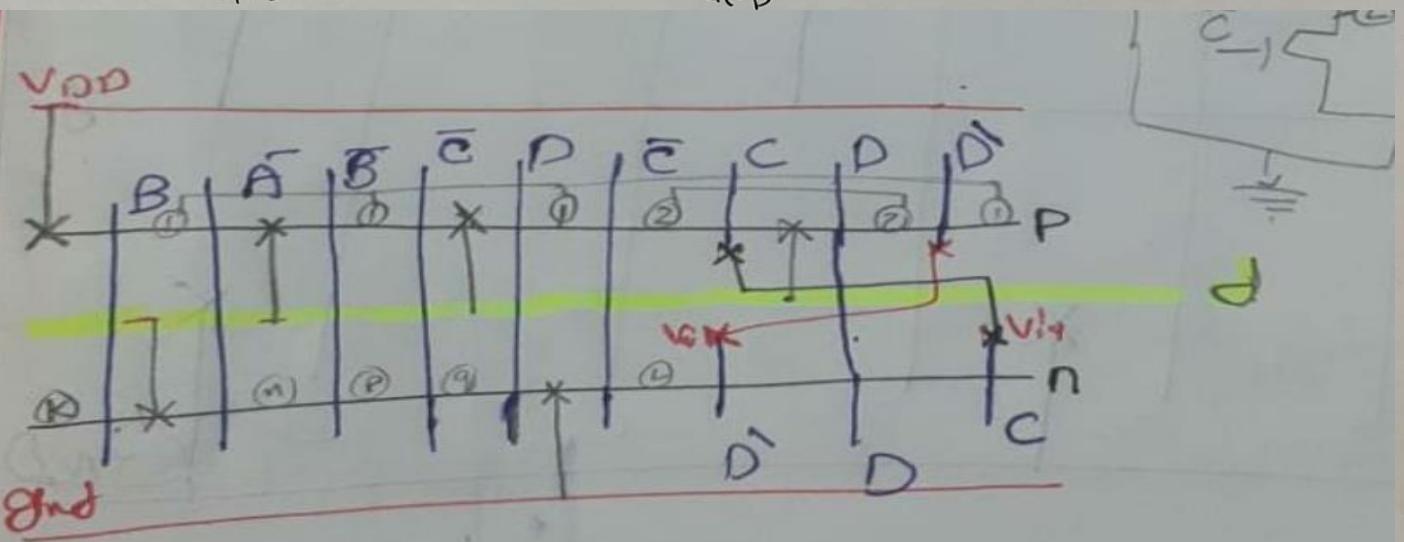
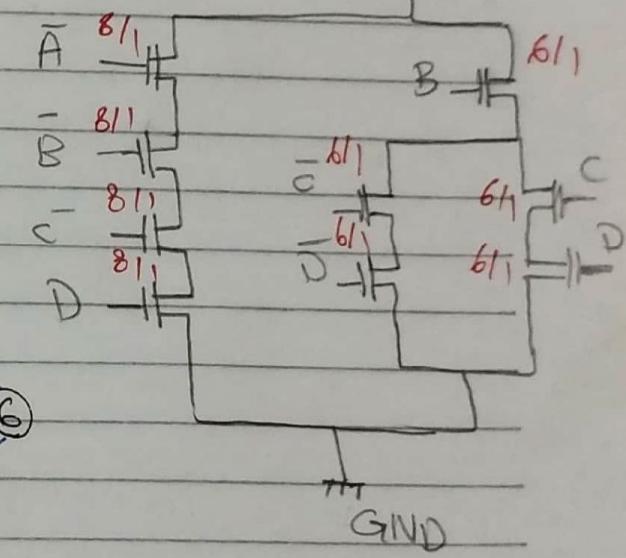
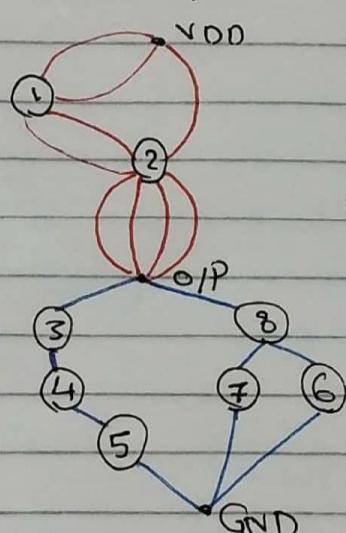
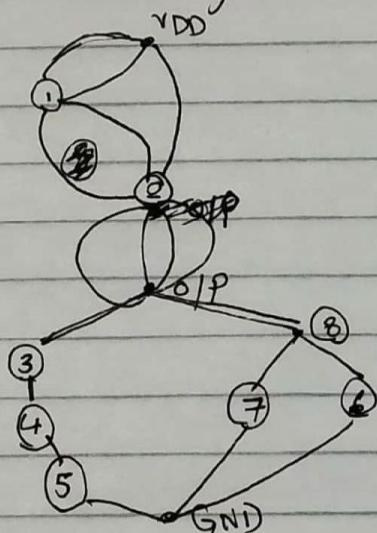


$$(W/L)_A = (W/L)_B = (W/L)_{\bar{C}} = (W/L)_{\bar{D}} = \frac{8}{1}$$

$$(W/L)_{\bar{C}} = (W/L)_{\bar{D}} = (W/L)_C = (W/L)_D = (W/L)_B = \frac{6}{1}$$

$\swarrow$  Euler diagram

Euler path.



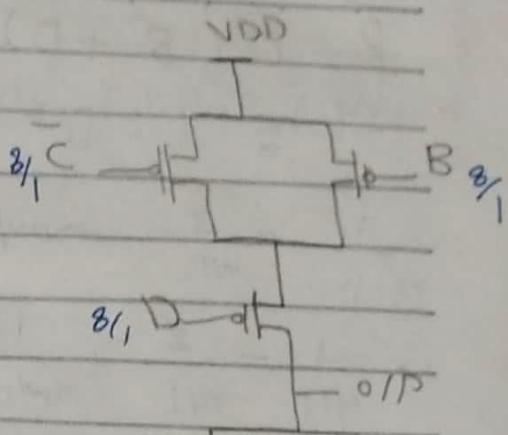
$$\bar{C} = BC + D$$

$$(w/l)_B - (w/l)_{\bar{C}} = (w/l)_D = (w/l)$$

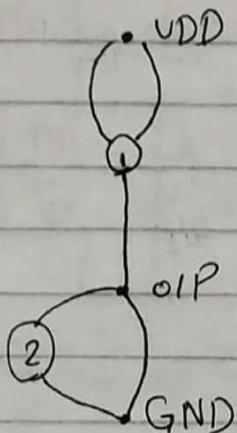
$$\frac{1}{L} = \frac{2}{w/l} \quad \text{in } (w/l) = 8/1$$

$$(w/l)_B = (w/l)_{\bar{C}}$$

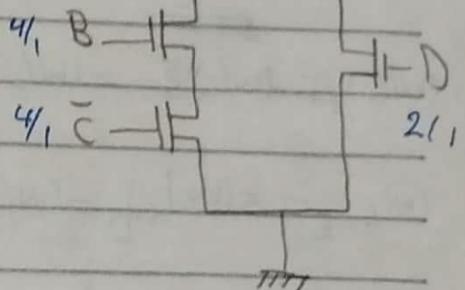
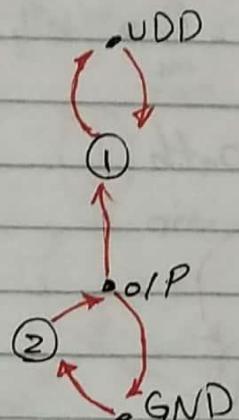
$$\frac{1}{L} = \frac{9}{(w/l)_B} \quad \text{in } (w/l)_B = 9/1, (w/l)_D = 2/1$$



Euler diagram

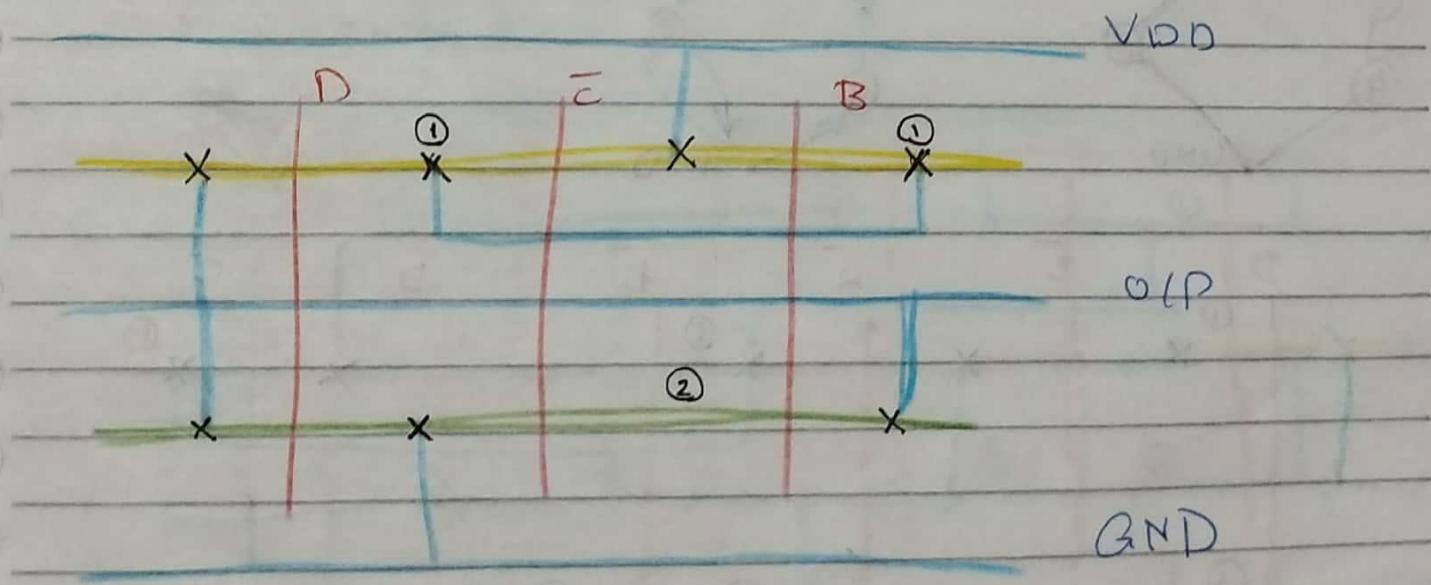


Euler path



Path D C B

Stick diagram :-

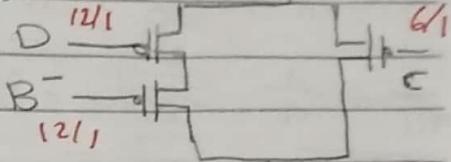


$$\bar{f} = C(\bar{B} + D) + \bar{A}\bar{B}D$$

$$(w/l)_B = (w/l)_D = (w/l)_A = (w/l)_D = (w/l)_B = (w/l)_C$$

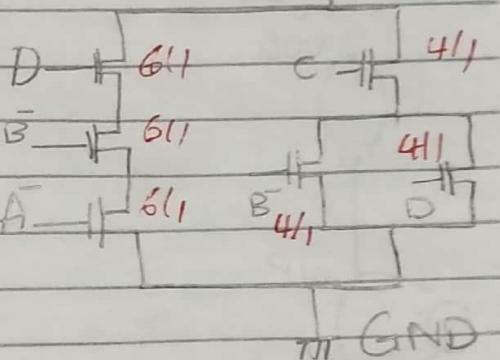
$$\frac{1}{(4/1)} = \frac{3}{w/l} \Rightarrow (w/l) = 12/1$$

$$\frac{1}{4/1} = \frac{2}{12/1} + \frac{1}{(w/l)_C} \Rightarrow (w/l)_C = \frac{6}{1}$$

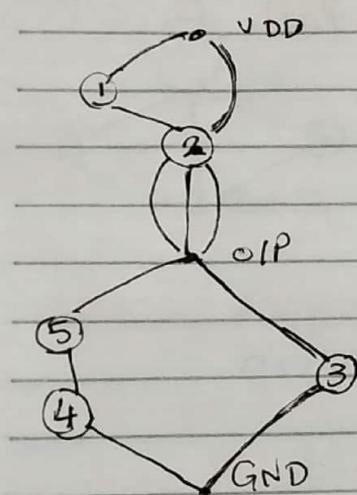


$$(w/l)_A = (w/l)\bar{B} = (w/l)_D \Rightarrow \frac{1}{2/1} = \frac{3}{w/l} \Rightarrow w/l = 6/1$$

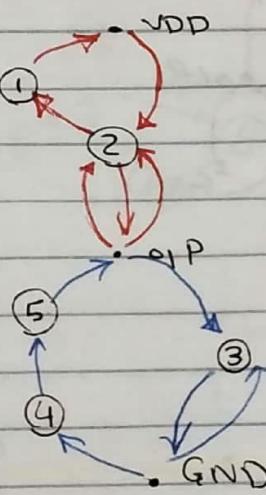
$$(w/l)_B = (w/l)_D = (w/l)_C \Rightarrow \frac{1}{2/1} = \frac{2}{w/l} \Rightarrow w/l = 4/1$$



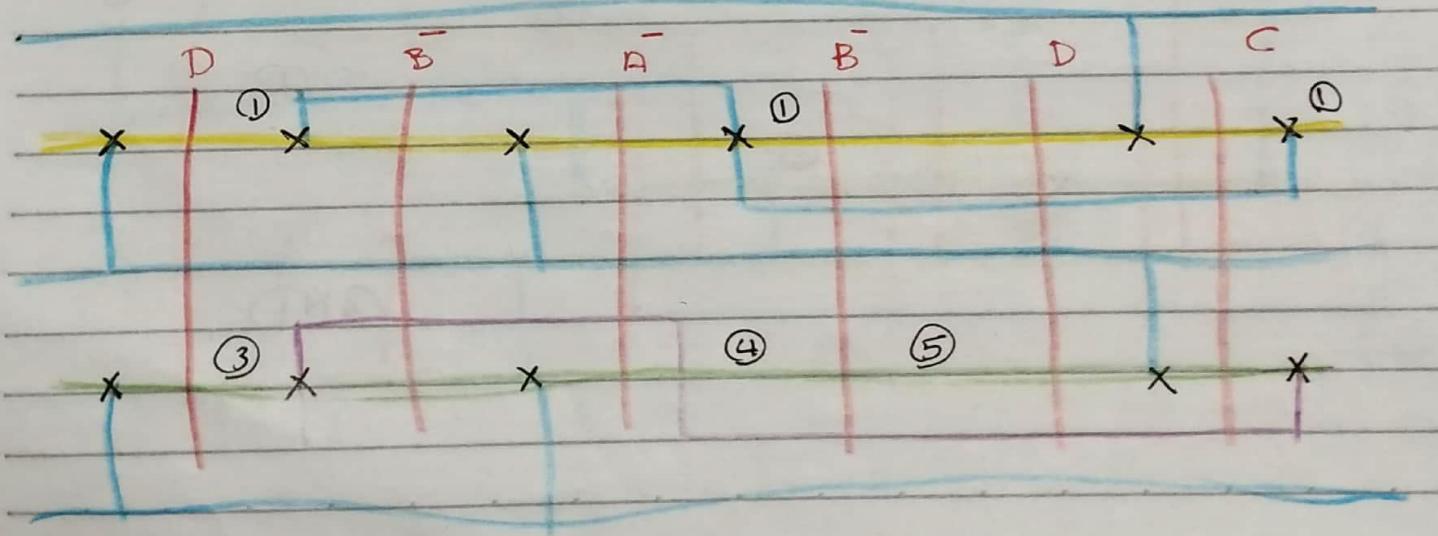
Euler diagram



Euler path.

Path  
D  $\bar{B}$  A  $\bar{B}$  D C

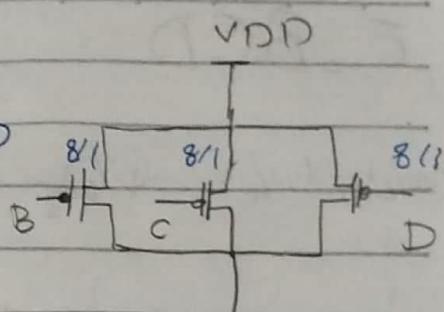
M2



$$g = \bar{A}\bar{B}\bar{C} + BCD$$

$$(w/l)_{\bar{A}} = (w/l)_{\bar{B}} = (w/l)_{\bar{C}} = (w/l)_B = (w/l)_C = (w/l)_D = w/l$$

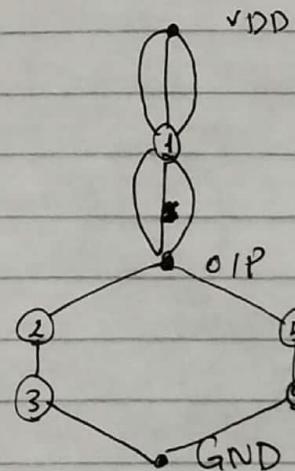
$$\frac{1}{4/1} = \frac{2}{w/l} \Rightarrow (w/l) = 8/1$$



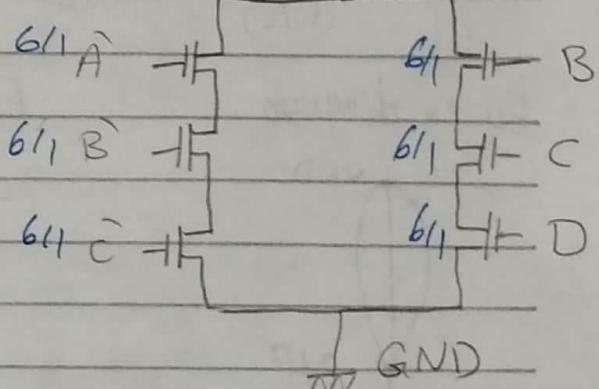
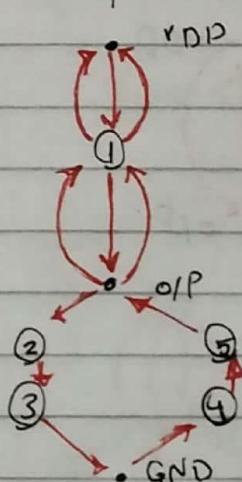
$$(w/l)_{\bar{A}} = (w/l)_{\bar{B}} = (w/l)_{\bar{C}} = (w/l)_B = (w/l)_C = (w/l)_D = w/l$$

$$\frac{1}{2/1} = \frac{3}{w/l} \Rightarrow (w/l) = 6/1$$

Euler diagram



Euler path



Path

$\bar{A}\bar{B}\bar{C}DCB$

stick diagram

