**Project**

The code file is attached. It includes design as well its UVM testbench with RAL Model.

**Tasks:**

1. Update the **ctrl_wr** sequence class
    a. Here the write method is used to write random data on the DUT register.
    b. Comment for loop, and first use **get()** method to check the desired value
    c. The use **set()** method to update the desired value and verify that if the desired value is updated
    d. Now use **update()** method, it will write the desired value on DUT
    e. During simulation, run both sequences, write as well as read for diagnosis.
    f. Now explain the purpose of each method. Submit the code and screenshot of the result.

2. **Predict()** updates both the desired as well as mirror value. And **mirror()** also does same
    a. Explore **predict()** method and **mirror()** method, and write the difference
    b. Use **write()** method to write a certain value ( ex 4'h5)
    c. Get desired and mirrored value and store in variables, and print them
    d. Now use **predict()** method with some value lets say ( 4'h3)
    e. Now again use **get()** and **get_mirrored_value()** methods and print the desired and mirrored value
    f. Now use the **mirror()** method and again get the desired and mirrored value. There will be an error. Explain the reason
    g. Write the observation

3. **FRONT_DOOR Access**
    a. In sequence class, Use **write()** and **read()** methods, with argument UVM_FRONTDOOR, and perform front door access.

4. **BACKDOOR Access**
    a. Explain what is backdoor access and what is its benefit.
    b. In reg block :
        i. Add hdl path
        ii. Use add_hdl_path_slice method to configure the DUT register that we can access using backdoor access

    c. In register sequence class, use write method with backdoor access and write some data,
    d. Now check desired as well as mirrored value
    e. In backdoor access we prefer using **poke** over the **write** method and **peek** over **read** method. Use these methods and attach the screenshot.