

Part II: Integrate riscv-dv test generator

- Generate a random test using riscv-dv <https://github.com/google/riscv-dv>. This has a UVM based flow as well as python based to generate any test. It's suggested to use Python based flow: https://github.com/google/riscv-dv/tree/master/pygen/pygen_src

Install RISC-V-DV-PyFlow

- Open the terminal in any directory of your choice.
- Clone the repository in your local terminal. It will not run in VNC due to the old Ubuntu version.
- Enter the command `git clone https://github.com/chipsalliance/riscv-dv.git`
- `cd riscv-dv`
- Install pip3 in your terminal using `sudo apt-get install python3-pip`
- `pip3 install -r requirements.txt` # install dependencies (only once)
- `python3 run.py --help`

Running the Generator

- `python3 run.py --test=riscv_arithmetic_basic_test --simulator=pyflow`
- After running the above command. An output directory will be generated with format like this `out_yyyy-mm-dd` (here y,m, and d represents the actual year, month and date).
- `cd` to this `out_yyyy-mm-dd` directory.
- Then `cd` `asm-test` directory.
- In this directory two single tests `riscv_arithmetic_basic_test_0.S` and `riscv_arithmetic_basic_test_1.S` will have been created.
- Create a new directory `assembly_test` in some other place and copy these tests in it.
- Again go to `riscv-dv` directory.
- `cd` to `user_extension` directory.
- Copy `user_define.h` and `user_init.s` from here in your `assembly_test` directory.

Riscv toolchain

- Make a new folder `toolchain` in any directory.
- Go to <https://github.com/riscv-collab/riscv-gnu-toolchain/releases>
- Choose and download a pre-built riscv32-elf-ubuntu toolchain compatible with the version of your ubuntu.
- Now extract the tar file in the `toolchain` directory.
- Open the terminal here.
- `cd <extracted_folder_name>/riscv/bin`
- `pwd` #it will print the complete address of the present working directory
- copy the <address>
- `export RISCVC=<address>`
- `echo $RISCVC` #it must provide the address you just assigned to it

- `export PATH=$PATH:$RISCV`
- `echo PATH` #now the address of RISCV must be appended at the end of other addresses in PATH variable
- `echo ~/.bashrc` #the basrc file will be opened
- Add these two lines at the end of this file
 1. `export RISCV=<address>` #the same RISCV address
 2. `export PATH=$PATH:$RISCV`
- Close the file.

Back to the terminal

- `source ~/.bashrc`
- Close the terminal.
- Go to this link:
https://github.com/riscv-software-src/riscv-isa-sim/blob/master/arch_test_target/spike/link.ld
- Place this link.ld file in assembly_test directory
- Stay in the assembly_test directory.
- Open the terminal in this directory and run the following three commands:
 1. `riscv32-unknown-elf-gcc -march=rv32imc -mabi=ilp32 -nostdlib -Tlink.ld riscv_arithmetic_basic_test_0.S -o riscv_arithmetic_basic_test_0.elf`
 2. `riscv32-unknown-elf-objdump -d riscv_arithmetic_basic_test_0.elf &> dis.ass`
 3. `riscv32-unknown-elf-objcopy -O binary riscv_arithmetic_basic_test_0.elf riscv_arithmetic_basic_test_0.bin`
- `riscv_arithmetic_basic_test_0.bin` and `dis.ass` will be generated in this directory.
- Now provide `riscv_arithmetic_basic_test_0.bin` to your UVM testbench to test Ibex core.
- To automate the above process you can create a makefile.