test id	hdd section	test name	test status	description or objective of test	stimulus geneation procedure	test passes when	test fails when	checking procedure
test_001		read_single_byte_nonseq_single_Htransfer	Pass	Basic Read Data (Byte Sized)	HTRANS to 2'b10 (indicating a non-sequential transfer) HWRITE to 0 (indicating a read operation) HRESET to 1 (de-asserting the reset state) HADDR to the random address of memory HSIZE to one of {0, 1, 2} (specifying the data size here it is 0) HBURST to 3'b000 (indicating a single transfer burst) HPROT to 4'b0001 (Data access)	The HRDATA signal provides the correct data from the specified address, and the HRESP signal is set to 0, indicating an "OKAY" response.	HRDATA does not provide the correct data from the address	The `HRDATA` signal fails to deliver the correct data from the specified address.
test_002		write_single_byte_nonseq_single_Htransfer	Pass	Basic Write Byte Sized	HTRANS to 2'b10 (indicating a non-sequential transfer) HWRITE to 1 (indicating a write operation) HRESET to 1 (de-asserting the reset state) HADDR to the random address of memory HSIZE to one of {0, 1, 2} (specifying the data size here it is 0) HBURST to 3'b000 (indicating a single transfer burst) HPROT to 4'b0001 (Data access)	The `HWDATA` signal is written to the memory at the specified address.	The `HWDATA` signal is not correctly written to the memory at the specified address.	Store the same data in a dummy memory at the corresponding address. Next, read the value from the original memory at the specified address and compare it with the data in the dummy memory to ensure consistency.
test_003		write_single_halfword_nonseq_single_Htransfer	Pass	Basic Write Half-Word Sized	HTRANS to 2'b10 (indicating a non-sequential transfer) HWRITE to 1 (indicating a write operation) HRESET to 1 (de-asserting the reset state) HADDR to the random address of memory HSIZE to one of {0, 1, 2} (specifying the data size here it is 1) HBURST to 3'b000 (indicating a single transfer burst) HPROT to 4'b0001 (Data access)	The `HWDATA` signal is written to the memory at the specified address.	The `HWDATA` signal is not correctly written to the memory at the specified address.	Store the same data in a dummy memory at the corresponding address. Next, read the value from the original memory at the specified address and compare it with the data in the dummy memory to ensure consistency.
test_004		Reset Single Transfer Test	Pass	In reset mode, the transfer mode switches to 0 (IDLE), preventing any read or write operations until the reset signal is de-asserted.	HRESET=0	During the reset phase, the slave must guarantee that the HREADYOUT signal remains HIGH and that the memory is initialized to a predetermined known state.	If HREADYOUT is not HIGH and the memory has not been initialized, the system may not function as intended.	Upon reset, both the testbench and the DUT memories are initialized to the value "00000000" Consequently, all addresses will contain the same data word until a different value is written following the de-assertion.
test_005		HSELx Test (Slave Select Test)	Pass	Verifies the operational integrity of the selection bit for HSEL (Slave Enable).	HSEL=0	The slave does not perform any read or write operations, and HRDATA is returning a default value.	If the slave executes any operation.	Using waveform

test_006		WRAP4 Burst Transfer Test for Word	Pass	Conducts a write/read burst test where the address is aligned to a 16-byte boundary.	HTRANS to 2'b11 and 2'b10 (indicating a non-sequential and seq transfer) HWRITE to 0 or 1 (indicating a read/write operation) HRESET to 1 (de-asserting the reset state) HADDR to 0x20, 0x24, 0x28, 0x2C HSIZE to one of {0, 1, 2} (specifying the data size here it is 2) HBURST to 3'b010 (indicating a Wrap 4 burst) HPROT to 4'b0001 (Data access)	The HRDATA output from the Design Under Test (DUT) at each address must match the HWDATA that was written to that specific address.	The HRDATA retrieved from the specified address does not correspond to the HWDATA that was written to that address.	Write HWDATA to four distinct addresses, then transition to Reading mode. Sequentially perform the reading process for each address and verify the results against the reference model.
test_007		Increment 4 Burst Test for Byte Transfers	Pass	Conducts a Write/Read BURST test in which the address increments with each beat of the byte transfer	HTRANS to 2'b11 and 2'b10 (indicating a non-sequential and seq transfer) HWRITE to 0 or 1 (indicating a read/write operation) HRESET to 1 (de-asserting the reset state) HADDR to 0x1, 0x2, 0x3, 0x4 HSIZE to one of {0, 1, 2} (specifying the data size here it is 0) HBURST to 3'b011 (indicating a 4 beat incrementing burst) HPROT to 4'b0001 (Data access)	The HRDATA output from the Design Under Test (DUT) at each address must match the HWDATA that was written to that specific address.	The HRDATA retrieved from the specified address does not correspond to the HWDATA that was written to that address.	Write HWDATA to four distinct addresses, then transition to Reading mode. Sequentially perform the reading process for each address and verify the results against the reference model.
test_008		Increment 4 Burst Test for Half-Word Transfers	Pass	Conducts a Write/Read BURST test in which the address increments with each beat of the half-word transfer	HTRANS to 2'b11 and 2'b10 (indicating a non-sequential and seq transfer) HWRITE to 0 or 1 (indicating a read/write operation) HRESET to 1 (de-asserting the reset state) HADDR to 0x2, 0x4, 0x6, 0x8 HSIZE to one of {0, 1, 2} (specifying the data size here it is 1)	The HRDATA output from the Design Under Test (DUT) at each address must match the HWDATA that was written to that specific	The HRDATA retrieved from the specified address does not correspond to the HWDATA that was written to that address.	Write HWDATA to four distinct addresses, then transition to Reading mode. Sequentially perform the reading process for each address and verify the results
test_009		Increment 4 Burst Test for Word Transfers	Pass	Conducts a Write/Read BURST test in which the address increments with each beat of the word transfer	HTRANS to 2'b11 and 2'b10 (indicating a non-sequential and seq transfer) HWRITE to 0 or 1 (indicating a read/write operation) HRESET to 1 (de-asserting the reset state) HADDR to 0x4, 0x8, 0xC, 0x10 HSIZE to one of {0, 1, 2} (specifying the data size here it is 2) HBURST to 3'b011 (indicating a 4 beat incrementing burst) HPROT to 4'b0001 (Data access)	The HRDATA output from the Design Under Test (DUT) at each address must match the HWDATA that was written to that specific address.	The HRDATA retrieved from the specified address does not correspond to the HWDATA that was written to that address.	Write HWDATA to four distinct addresses, then transition to Reading mode. Sequentially perform the reading process for each address and verify the results against the reference model.
test_010		Write/Read Test for Byte	Pass	This test involves an alternate byte write/read operation using incrementing addresses. Initially, a value is written to a specific address, followed by reading from that same address to verify that the data has been accurately stored in the DUT. At the conclusion of each operation, the address is updated to facilitate writing to a different location during the next cycle.	HTRANS to 2'b10 (indicating a non-sequential transfer) HWRITE to 1 or 0 (indicating a Write/Read operation) HRESET to 1 (de-asserting the reset state) HADDR to the random address of memory HSIZE to one of {0, 1, 2} (specifying the data size here it is 0) HBURST to 3'b000 (indicating a single transfer burst) HPROT to 4'b0001 (Data access)	HRDATA returns the data that matches the value previously written to the corresponding address.	The data read from the specified address does not match the data that was previously written.	Write the HWDATA to a designated address, and then verify the HRDATA value at that same address in subsequent clock cycles to ensure correctness. This validation can be performed through simulation.

test_011		Write/Read Test for Half Word	Pass	This test involves an alternate half-word write/read operation using incrementing addresses. Initially, a value is written to a specific address, followed by reading from that same address to verify that the data has been accurately stored in the DUT. At the conclusion of each operation, the address is updated to facilitate writing to a different location during the next cycle.	HTRANS to 2'b10 (indicating a non-sequential transfer) HWRITE to 1 or 0 (indicating a Write/Read operation) HRESET to 1 (de-asserting the reset state) HADDR to the random address of memory HSIZE to one of {0, 1, 2} (specifying the data size here it is 1) HBURST to 3'b000 (indicating a single transfer burst) HPROT to 4'b0001 (Data access)	HRDATA returns the data that matches the value previously written to the corresponding address.	The data read from the specified address does not match the data that was previously written.	Write the HWDATA to a designated address, and then verify the HRDATA value at that same address in subsequent clock cycles to ensure correctness. This validation can be performed through simulation.
test_012		Write/Read Test for Word	Pass	This test involves an alternate word write/read operation using incrementing addresses. Initially, a value is written to a specific address, followed by reading from that same address to verify that the data has been accurately stored in the DUT. At the conclusion of each operation, the address is updated to facilitate writing to a different location during the next cycle.	HTRANS to 2'b10 (indicating a non-sequential transfer) HWRITE to 1 or 0 (indicating a Write/Read operation) HRESET to 1 (de-asserting the reset state) HADDR to the random address of memory HSIZE to one of {0, 1, 2} (specifying the data size here it is 2) HBURST to 3'b000 (indicating a single transfer burst) HPROT to 4'b0001 (Data access)	HRDATA returns the data that matches the value previously written to the corresponding address.	The data read from the specified address does not match the data that was previously written.	Write the HWDATA to a designated address, and then verify the HRDATA value at that same address in subsequent clock cycles to ensure correctness. This validation can be performed through simulation.

assertion description