CISC

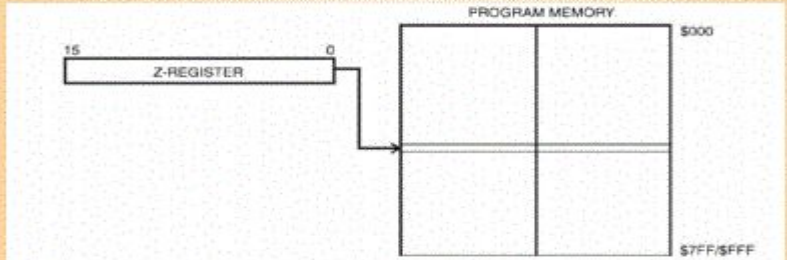
- Richer instruction set, some simple, some very complex
- Instructions generally take more than 1 clock to execute
- Instructions of variable size
- Instructions interface with memory in multiple mechanisms with complex addressing modes
- No pipelining
- Upward compatibility within a family
- Microcode control
- Work well with simpler compiler

RISC

- Simple, primitive instructions and addressing modes.
- Instructions typically execute in one clock cycle.
- Uniformed length instructions and fixed instruction format.
- Instructions interface with memory via fixed mechanisms.
- Pipelining
- Instruction set is orthogonal (little overlapping of instruction functionality.
- Hardwired control
- Complexity pushed to the compiler.

9 – Indirect Program Addressing

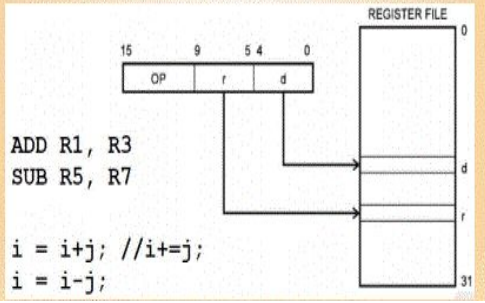
- In these types of instructions, the Z register is used to point to the program memory. (Up to 64 Kbytes of program memory)




```
IJMP  ;Indirect Jump to (Z) PC ← Z
ICALL ;Indirect Call to (Z) PC ← Z,STACK = PC  + 1
```

2 - Register Direct (Two Registers)

- Two registers are involved.
  - Rs: Source register
  - Rd: Destination register
  - Instruction reads the two registers and operates on their contents and stores the result back in the destination register.




```
ADD R1, R3
SUB R5, R7

i = i+j; //i+=j;
i = i-j;
```

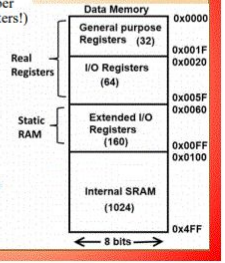
3 – Immediate Mode

- A constant value is in the instruction
- This will be store with program code in program memory space (Flash memory on AVR)

```
SUBI R4, 8   ;Subtract Constant from Register
ADIW R26, 5  ;Add Immediate to Word
             ;R27:R26 ← R27:R26 + 5  --
                   Double register operation
                   Uses special register pairs
i -= 8;
a += 29;
```


6 – (cont) I/O Ports using Indirect

- The ports can also be accessed using SRAM access commands, e.g. ST and LD. Just add 0x20 to the port number (the first 32 addresses are the registers!) and access the port that way. Like demonstrated here:




```
.DEF SomeRegister = R16

   LDI ZH,HIGH(PORTB+32)
   LDI ZL,LOW(PORTB+32)
   LD SomeRegister,Z
```


Extended I/O

- For I/O registers located in extended I/O map, I/O register direct commands like "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" cannot be used. They must be replaced with direct (memory) and indirect (memory) instructions that allow access to extended I/O, typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".