AlphaLogos: Logic Synthesis Optimization using Quine–McCluskey Algorithm

Demo Test Cases Report

Digital Design I

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Demo Link: AlphaLogos

1 TEST CASE: $F(A, B, C) = A+B'C$

1.1 Truth Table

A	B	C	A+B'C
False	False	False	False
True	False	False	True
False	True	False	False
True	True	False	True
False	False	True	True
True	False	True	True
False	True	True	False
True	True	True	True

1.2 Canonical Forms

SoP: AB'C' + ABC' + A'B'C + AB'C + ABC

PoS: (A+B+C) (A+B'+C) (A+B'+C')

1.3 Prime Implicants

PIs: B'C + A

1.4 Essential Prime Implicants

EPIs: B'C + A

1.5 Uncovered Minterms

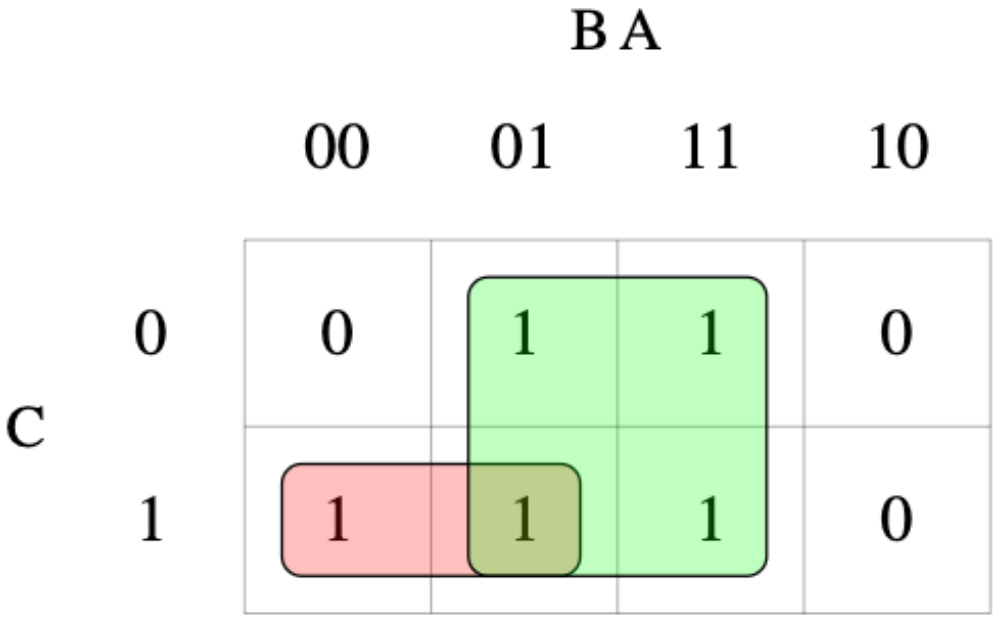
Uncovered Minterms: No Uncovered Minterms

1.6 Minimized Expression

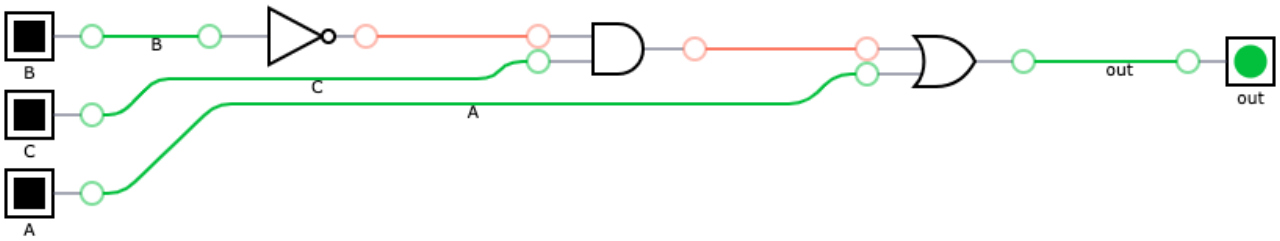
Minimized Expression: B'C + A

Number of MOSFETs: 12

1.7 Karnaugh Map



1.8 Logic Circuit



2 TEST CASE: $F(A, B, C, D) = ABC'+DC+B'$

2.1 Truth Table

A	B	C	D	ABC'+DC+B'
False	False	False	False	True
True	False	False	False	True
False	True	False	False	False
True	True	False	False	True
False	False	True	False	True
True	False	True	False	True
False	True	True	False	False
True	True	True	False	False
False	False	False	True	True
True	False	False	True	True
False	True	False	True	False
True	True	False	True	True
False	False	True	True	True
True	False	True	True	True
False	True	True	True	True
True	True	True	True	True

2.2 Canonical Forms

SoP: A'B'C'D' + AB'C'D' + ABC'D' + A'B'CD' + AB'CD' + A'B'C'D

PoS: (A+B'+C+D) (A+B'+C'+D) (A'+B'+C'+D) (A+B'+C+D')

+ AB'C'D + ABC'D + A'B'CD + AB'CD + A'BCD + ABCD

2.3 Prime Implicants

PIs: AC' + AD + CD + B'

2.4 Essential Prime Implicants

EPIs: AC' + CD + B'

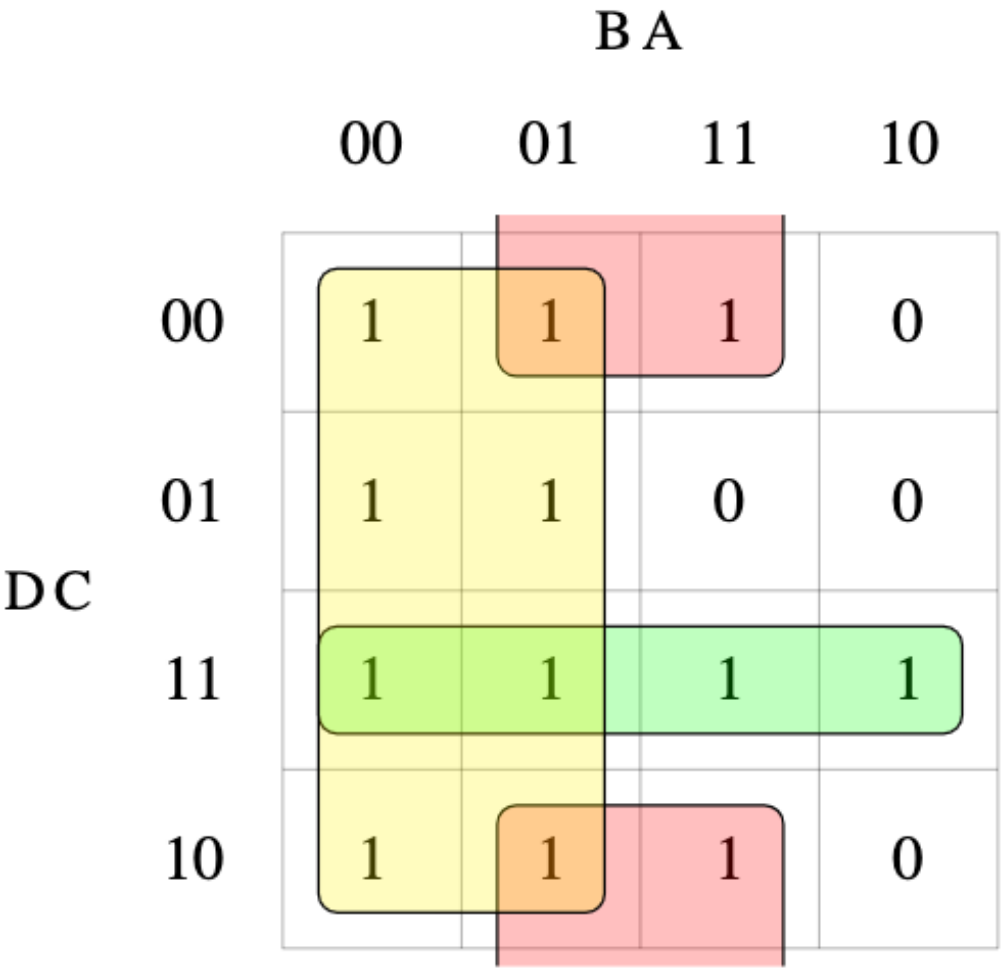
2.5 Uncovered Minterms

Uncovered Minterms:	No Uncovered Minterms

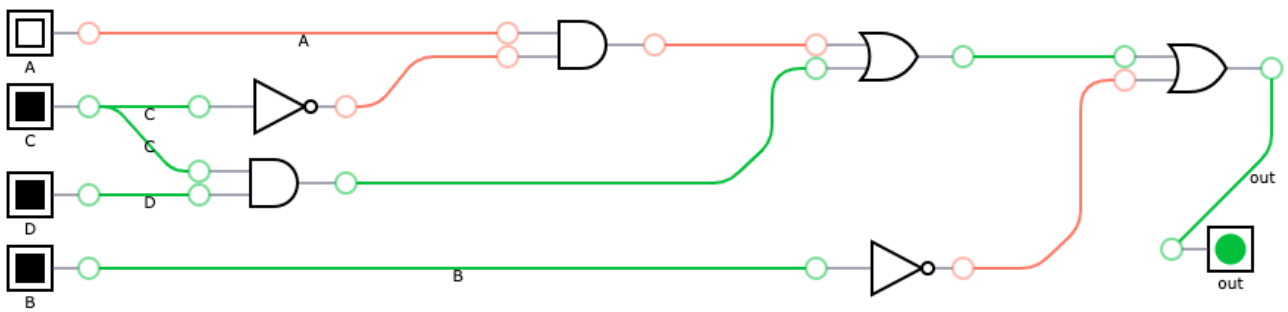
2.6 Minimized Expression

Minimized Expression:	AC' + CD + B'
Number of MOSFETs:	20

2.7 Karnaugh Map



2.8 Logic Circuit



3 TEST CASE: $F(A, B, C) = AA'+BB'+CC'$

3.1 Truth Table

A	B	C	AA'+BB'+CC'
False	False	False	False
True	False	False	False
False	True	False	False
True	True	False	False
False	False	True	False
True	False	True	False
False	True	True	False
True	True	True	False

3.2 Canonical Forms

SoP: 0

PoS: (A+B+C) (A'+B+C) (A+B'+C) (A'+B'+C) (A+B+C')

(A'+B+C') (A+B'+C') (A'+B'+C')

3.3 Prime Implicants

PIs: 0

3.4 Essential Prime Implicants

EPIs: 0

3.5 Uncovered Minterms

Uncovered Minterms: **No Uncovered Minterms**

3.6 Minimized Expression

Minimized Expression: **0**

Number of MOSFETs: **0**

3.7 Karnaugh Map

C \ BA	00	01	11	10
0	0	0	0	0
1	0	0	0	0

4 TEST CASE: $F(A, B, C) = (A+A')(B+B')(C+C')$

4.1 Truth Table

A	B	C	(A+A')(B+B')(C+C')
False	False	False	True
True	False	False	True
False	True	False	True
True	True	False	True
False	False	True	True
True	False	True	True
False	True	True	True
True	True	True	True

4.2 Canonical Forms

SoP: A'B'C' + AB'C' + A'BC' + ABC' + A'B'C + AB'C + A'BC + ABC

PoS: 1

4.3 Prime Implicants

PIs: 1

4.4 Essential Prime Implicants

EPIs: 1

4.5 Uncovered Minterms

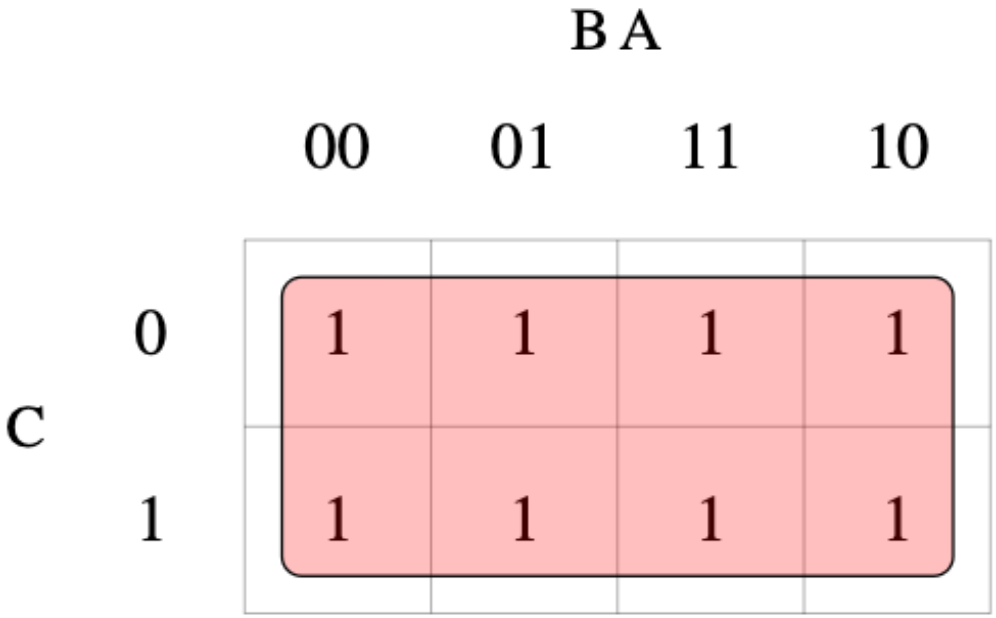
Uncovered Minterms: No Uncovered Minterms

4.6 Minimized Expression

Minimized Expression: 1

Number of MOSFETs: 0

4.7 Karnaugh Map



5 TEST CASE: $F(A, B, C, D) = C+AD'+A'BC'D+AB'C$

5.1 Truth Table

C	A	D	B	C+AD'+A'BC'D+AB'C
False	False	False	False	False
True	False	False	False	True
False	True	False	False	True
True	True	False	False	True
False	False	True	False	False
True	False	True	False	True
False	True	True	False	False
True	True	True	False	True
False	False	False	True	False
True	False	False	True	True
False	True	False	True	True
True	True	False	True	True
False	False	True	True	True
True	False	True	True	True
False	True	True	True	False
True	True	True	True	True

5.2 Canonical Forms

SoP: CA'D'B' + C'AD'B' + CAD'B' + CA'DB' +

PoS: (C+A+D+B) (C+A+D'+B) (C+A'+D'+B)

+ CADB' + CA'D'B + C'AD'B + CAD'B + C'A'DB + CA'DB + CADB

(C+A+D+B') (C+A'+D'+B')

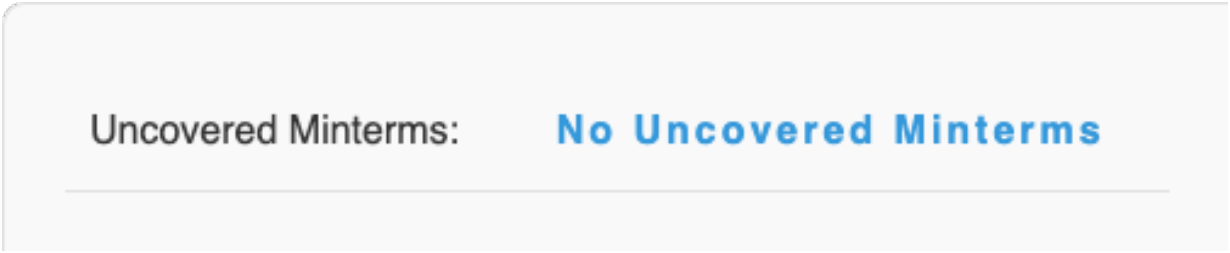
5.3 Prime Implicants

PIs: A'DB + AD' + C

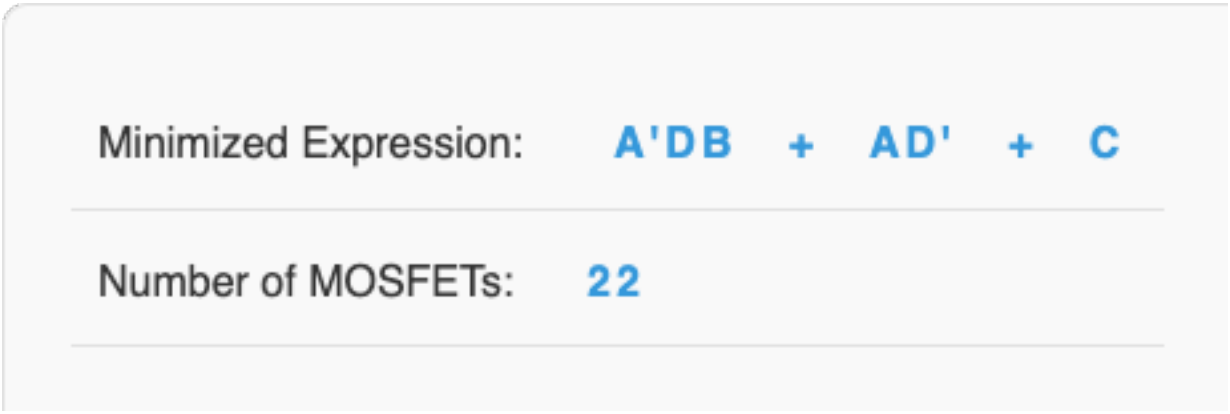
5.4 Essential Prime Implicants

EPIs: A'DB + AD' + C

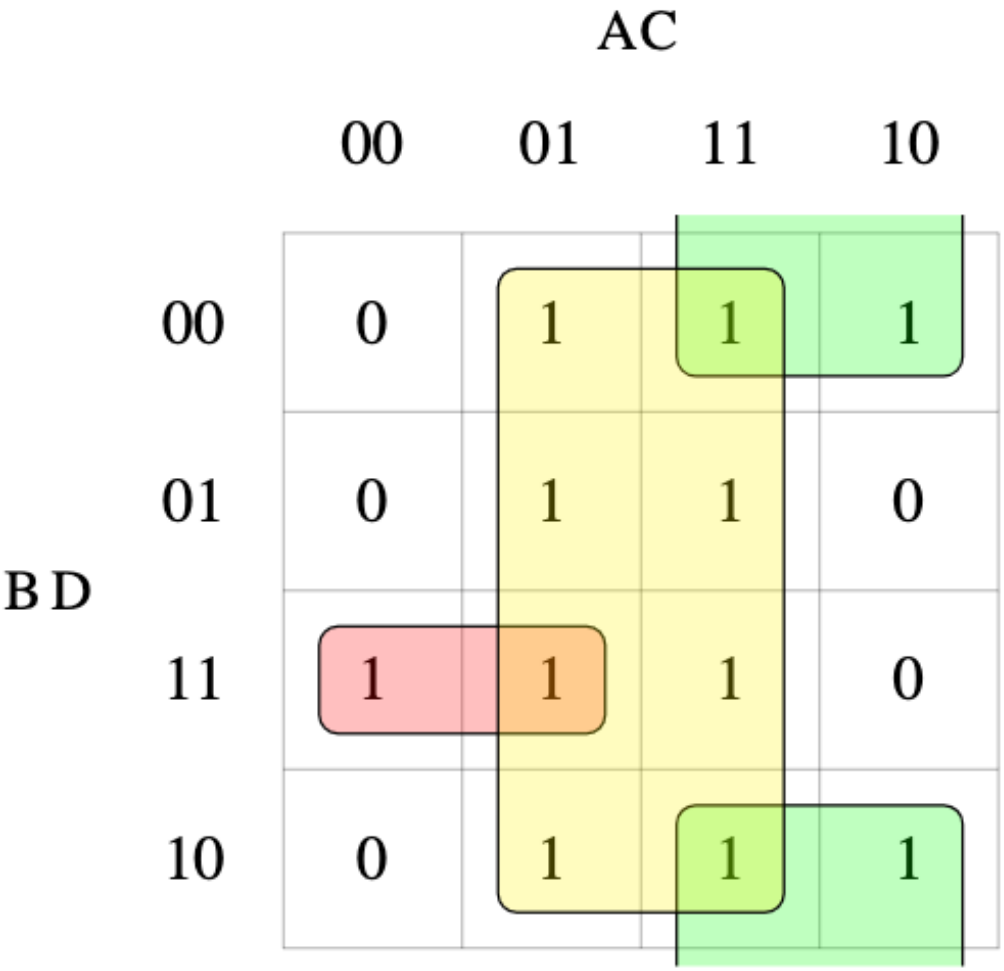
5.5 Uncovered Minterms



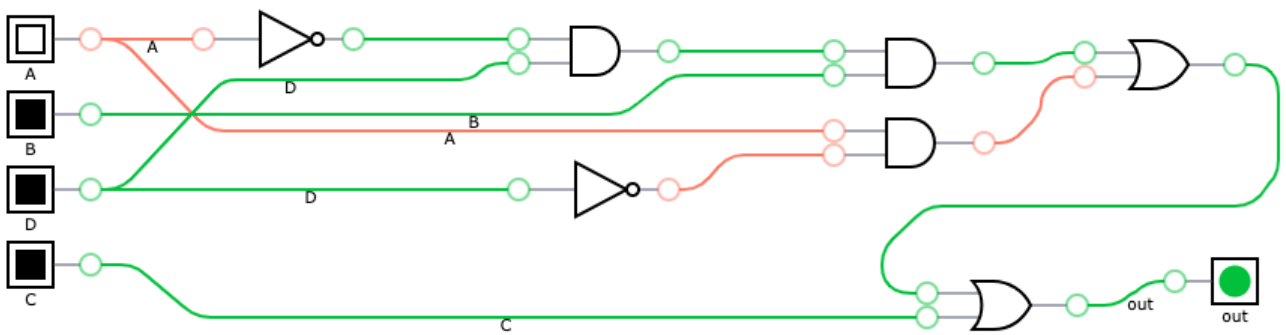
5.6 Minimized Expression



5.7 Karnaugh Map



5.8 Logic Circuit



6 TEST CASE: $F(A, B, C, D) = AB'C'+BD+A'C'D +A'BC+ACD+ABC'+A'CD'$

6.1 Truth Table

A	B	C	D	AB'C'+BD+A'C'D +A'BC+ACD+ABC'+A'CD'
False	False	False	False	False
True	False	False	False	True
False	True	False	False	False
True	True	False	False	True
False	False	True	False	True
True	False	True	False	False
False	True	True	False	True
True	True	True	False	False
False	False	False	True	True
True	False	False	True	True
False	True	False	True	True
True	True	False	True	True
False	False	True	True	False
True	False	True	True	True
False	True	True	True	True
True	True	True	True	True

6.2 Canonical Forms

SoP: AB'C'D' + ABC'D' + A'B'CD' + A'BCD' +

PoS: (A+B+C+D) (A+B'+C+D) (A'+B+C'+D)

+ A'B'C'D + AB'C'D + A'BC'D + ABC'D + AB'CD + A'BCD + ABCD

(A'+B'+C'+D) (A+B+C'+D')

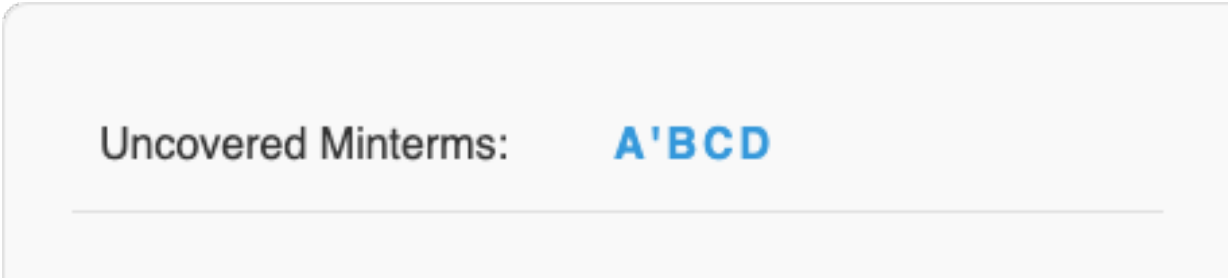
6.3 Prime Implicants

PIs: A'CD' + A'BC + AC' + C'D + AD + BD

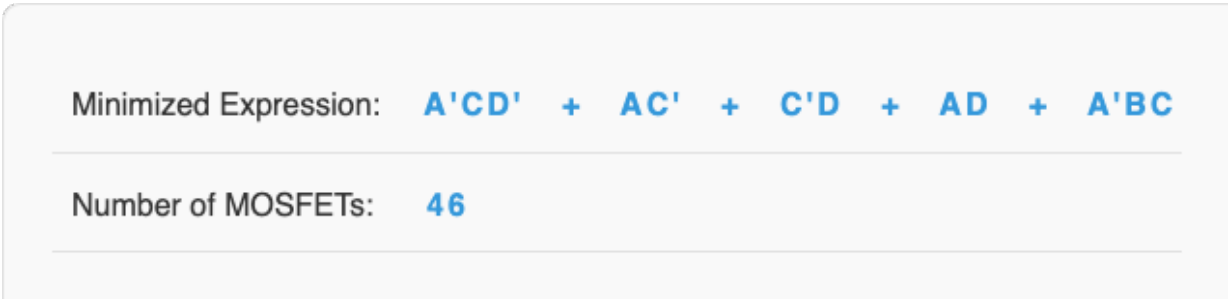
6.4 Essential Prime Implicants

EPIs: A'CD' + AC' + C'D + AD

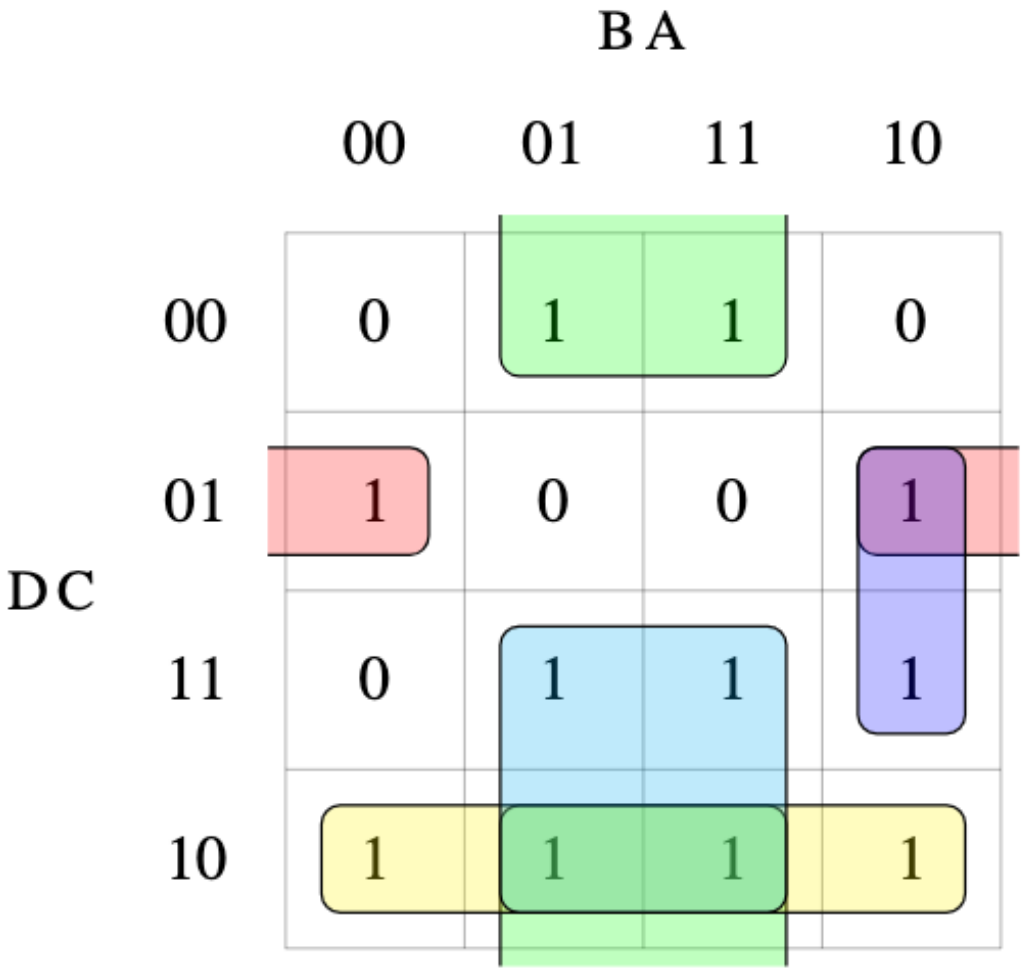
6.5 Uncovered Minterms



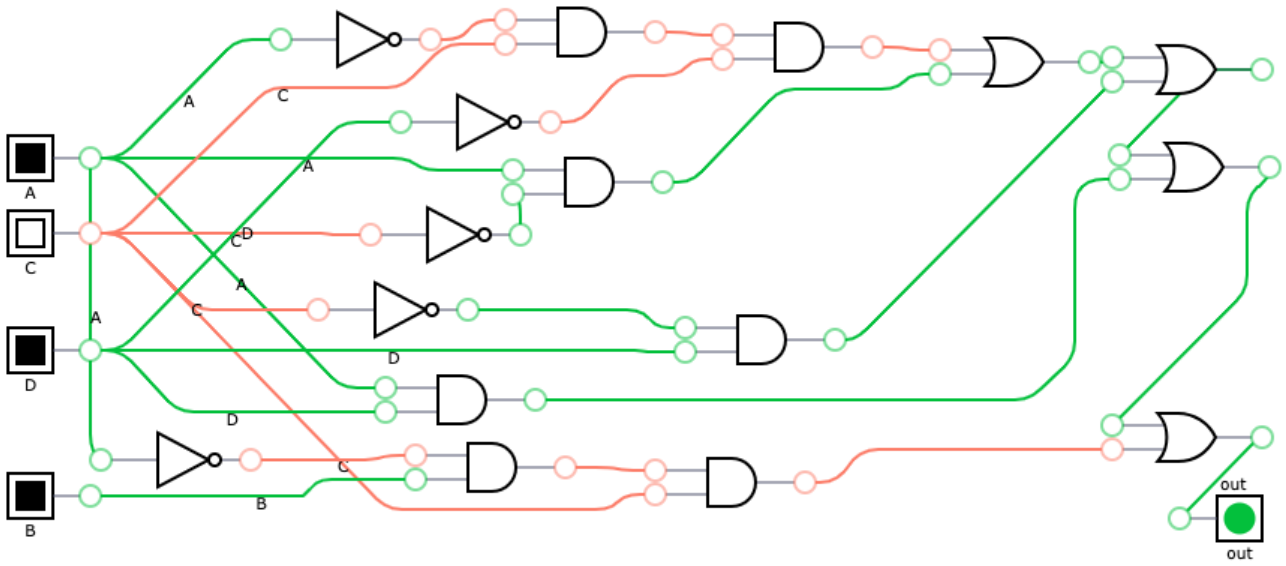
6.6 Minimized Expression



6.7 Karnaugh Map



6.8 Logic Circuit



7 TEST CASE: $F(A, B, C, D) = (A+B')(A+C'+D)(B+D)(C+D')$

7.1 Truth Table

A	B	C	D	(A+B')(A+C'+D)(B+D)(C+D')
False	False	False	False	False
True	False	False	False	False
False	True	False	False	False
True	True	False	False	True
False	False	True	False	False
True	False	True	False	False
False	True	True	False	False
True	True	True	False	True
False	False	False	True	False
True	False	False	True	False
False	True	False	True	False
True	True	False	True	False
False	False	True	True	True
True	False	True	True	True
False	True	True	True	False
True	True	True	True	True

7.2 Canonical Forms

SoP: ABC'D' + ABCD' + A'B'CD + AB'CD + ABCD

PoS: (A+B+C+D) (A'+B+C+D) (A+B'+C+D) (A+B+C'+D)

(A'+B+C'+D) (A+B'+C'+D) (A+B+C+D') (A'+B+C+D')

(A+B'+C+D') (A'+B'+C+D') (A+B'+C'+D')

7.3 Prime Implicants

Pls: ABD' + ABC + B'CD + ACD

7.4 Essential Prime Implicants

EPIs: ABD' + B'CD

7.5 Uncovered Minterms

Uncovered Minterms: ABCD

7.6 Minimized Expression

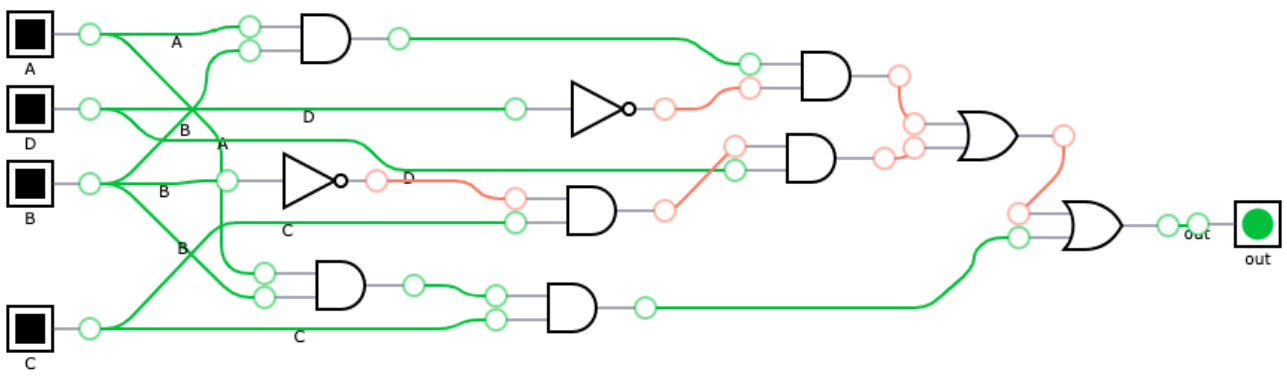
Minimized Expression: ABD' + B'CD + ABC

Number of MOSFETs: 32

7.7 Karnaugh Map

DC \ BA	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	1	1	1	0
10	0	0	0	0

7.8 Logic Circuit



8 TEST CASE: $F(A, B, C, D) = (a+b")(c+b)'$

8.1 Truth Table

a	b	c	(a+b")(c+b)'
False	False	False	False
True	False	False	True
False	True	False	False
True	True	False	False
False	False	True	False
True	False	True	False
False	True	True	False
True	True	True	False

8.2 Canonical Forms

SoP: ab'c'

PoS: (a+b+c) (a+b'+c) (a'+b'+c) (a+b+c') (a'+b+c') (a+b'+c') (a'+b'+c')

8.3 Prime Implicants

PIs: ab'c'

8.4 Essential Prime Implicants

EPIs: ab'c'

8.5 Uncovered Minterms

Uncovered Minterms: No Uncovered Minterms

8.6 Minimized Expression

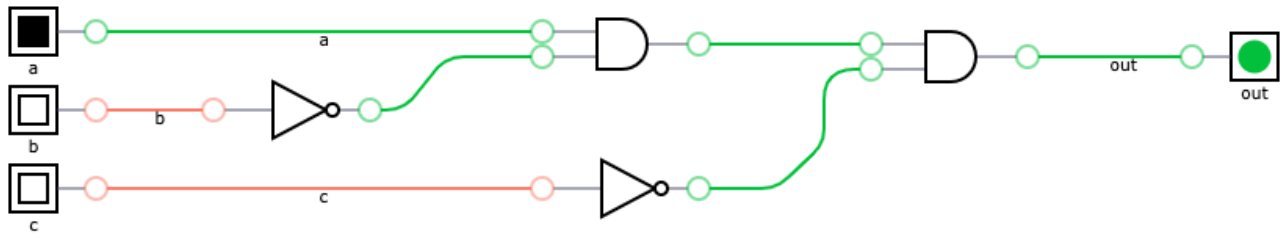
Minimized Expression: ab'c'

Number of MOSFETs: 8

8.7 Karnaugh Map

c \ ba	00	01	11	10
0	0	1	0	0
1	0	0	0	0

8.8 Logic Circuit



9 TEST CASE: $F(A, B, C, D) = aa'+bb'+dd''+c$

9.1 Truth Table

a	b	d	c	aa'+bb'+dd''+c
False	False	False	False	False
True	False	False	False	False
False	True	False	False	False
True	True	False	False	False
False	False	True	False	True
True	False	True	False	True
False	True	True	False	True
True	True	True	False	True
False	False	False	True	True
True	False	False	True	True
False	True	False	True	True
True	True	False	True	True
False	False	True	True	True
True	False	True	True	True
False	True	True	True	True
True	True	True	True	True

9.2 Canonical Forms

SoP: a'b'dc' + ab'dc' + a'bdc' + abdc' + a'b'd'c + ab'd'c +

PoS: (a+b+d+c) (a'+b+d+c) (a+b'+d+c) (a'+b'+d+c)

+ a'bd'c + abd'c + a'b'dc + ab'dc + a'bdc + abdc

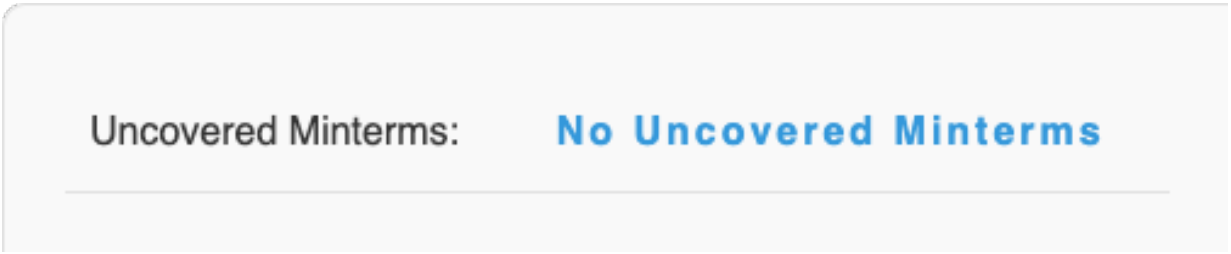
9.3 Prime Implicants

PIs: d + c

9.4 Essential Prime Implicants

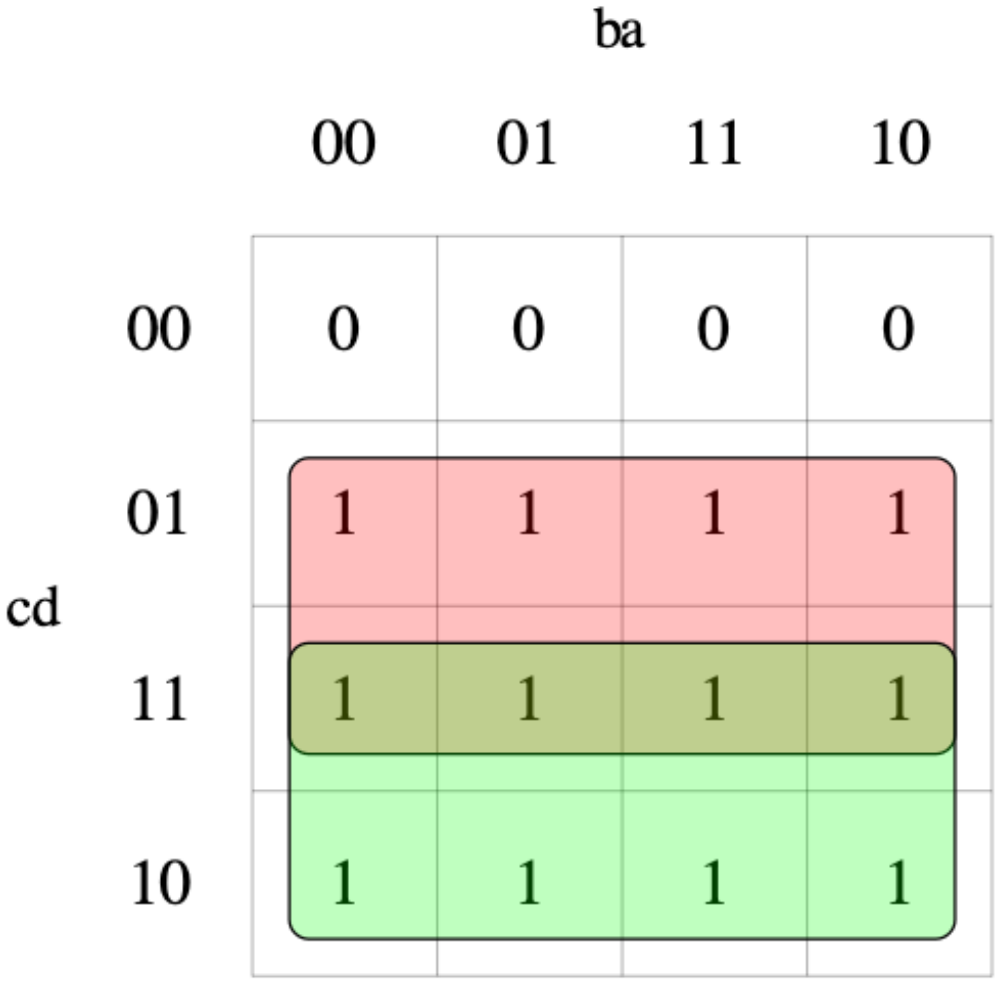
EPIs: d + c

9.5 Uncovered Minterms

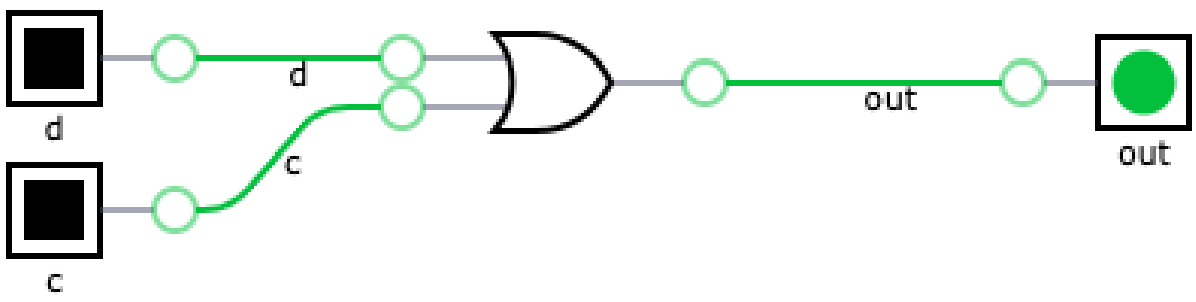


9.6 Minimized Expression

9.7 Karnaugh Map



9.8 Logic Circuit



10 TEST CASE: $F(A, B, C, D) = AB'C' + BD' + A'C'D + A'BC + ACD$

10.1 Truth Table

A	B	C	D	AB'C' + BD' + A'C'D + A'BC + ACD
False	False	False	False	False
True	False	False	False	True
False	True	False	False	True
True	True	False	False	True
False	False	True	False	False
True	False	True	False	False
False	True	True	False	True
True	True	True	False	True
False	False	False	True	True
True	False	False	True	True
False	True	False	True	True
True	True	False	True	False
False	False	True	True	False
True	False	True	True	True
False	True	True	True	True
True	True	True	True	True

10.2 Canonical Forms

SoP: AB'C'D' + A'BC'D' + ABC'D' + A'BCD' + ABCD' + A'B'C'D + AB'C'D + A'BC'D + AB'CD + A'BCD + ABCD

PoS: (A+B+C+D) (A+B+C'+D) (A'+B+C'+D) (A'+B'+C+D') (A+B+C'+D')

10.3 Prime Implicants

PIs: AC'D' + AB'C' + B'C'D + A'C'D + AB'D + ACD + BD' + A'B + BC

10.4 Essential Prime Implicants

EPIs: No Essential Prime Implicants

10.5 Uncovered Minterms

Uncovered Minterms: AB'C'D' + A'BC'D' + ABC'D' + A'BCD' + ABCD'

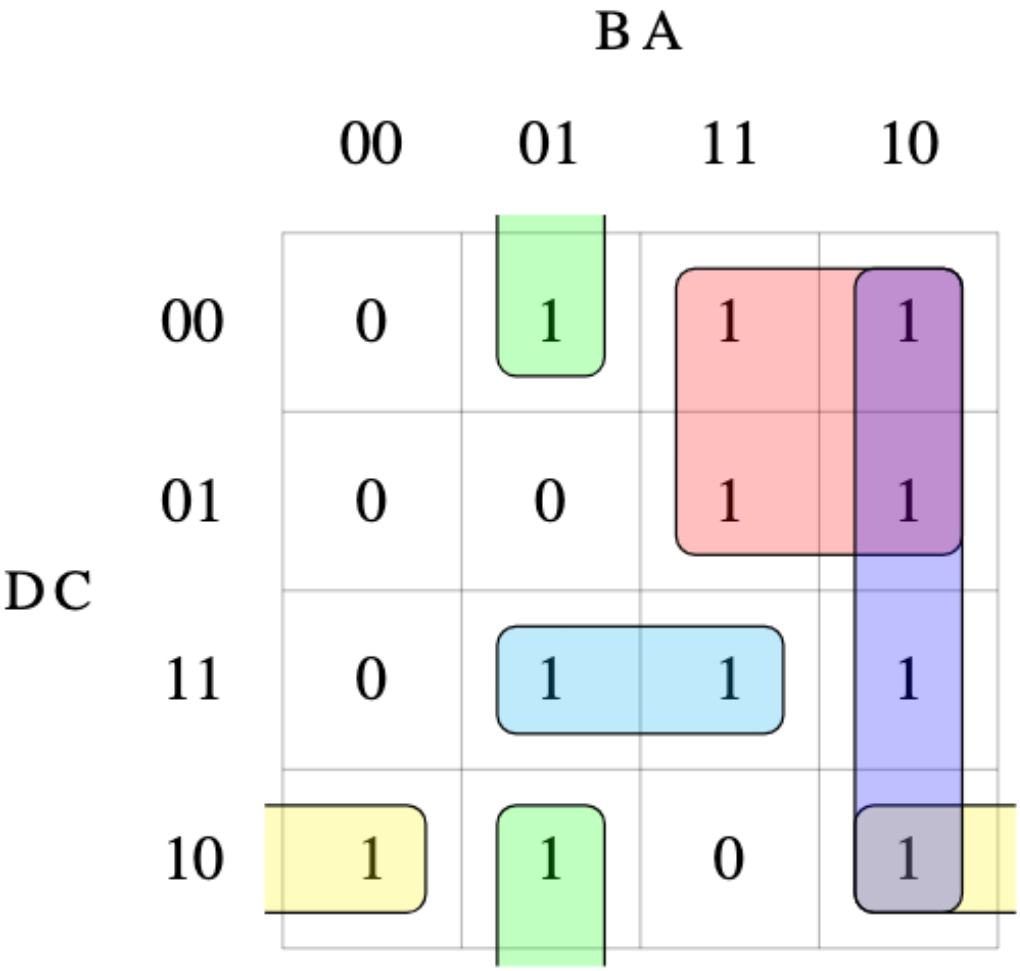
+ A'B'C'D + AB'C'D + A'BC'D + AB'CD + A'BCD + ABCD

10.6 Minimized Expression

Minimized Expression: BD' + AB'C' + A'C'D + ACD + A'B

Number of MOSFETs: 48

10.7 Karnaugh Map



10.8 Logic Circuit