Cache Controller

- *A Soft IP Core for Direct Mapped Caches*
- ***Version: 1.0***

Specifications

- Direct Mapped Cache Controller.
- Designed for single banked caches
- Write-Through policy on write hits.
- No-Write-Allocate or Write-Around policy on write misses.
- Tag Array is incorporated within.
- Configurable Index and Tag widths.
- No Write Buffer or other optimizations.

RTL Schematic

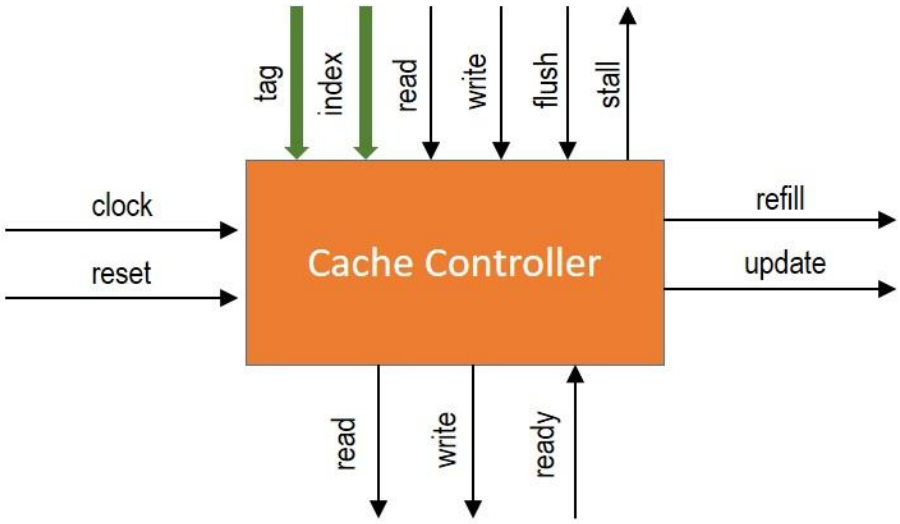

Fig. Cache Controller Interface

Ports

Signal	Direction	Bus width	Description
clock	in	-	Clock input same as the Processor.
reset	in	-	Active-low Asynchronous Reset to reset all the states and signals.
flush	in	-	Active-high signal to Flush and invalidate all the Cache Lines.
read	in	-	Active-high signal from the processor to read from Cache.
write	in	-	Active-high Signal from the processor to write to Cache.
index	in	configurable	Index header of the requested address.
tag	in	configurable	Tag header of the requested address.
ready	in	-	Active-high signal from Main Memory to acknowledge that the data is ready.
refill	out	-	Active-high signal to Cache Memory to refill the Cache Line using the data block read from Main Memory.
update	out	-	Active-high signal to Cache Memory to update the corresponding word on the Cache Line, on a write hit.
stall	out	-	Active-high signal to stall the processor on read/write misses and write hits.
read (from Main Memory)	out	-	Active-high signal to Main Memory to fetch the required data block on a read miss.
write (to Main Memory)	out	-	Active-high signal to Main Memory to write the word on a write hit/miss.

Hit and Miss Latencies

- **Handling Read Hits and Misses**

  All Read Hits are straight forward. No stalling on the processor for Read Hits. However, Read Misses stall the processor so as to fetch the requested data block from the Main Memory in the meantime. Fetching of the data block is followed by updating the Cache Line and then finally followed by a Read Hit to complete the read cycle. Read Miss has the most expensive penalty in the design.

- **Handling Write Hits and Misses**

  All Write Hits/Misses stall the processor for same number of cycles. Hence, they are equivalent in the amount of penalty. This is because of the Write-Through Policy in the design that mandates writing to Main Memory on all Write Hits for Data Coherence/Consistency. Write-Around Policy is followed on Write Misses. The misses write the data directly to the Main Memory, without loading the data block to the Cache.

Action	Latency (clock cycles)	Stall (clock cycles)
Read Hit	2	-
Read Miss	6	4
Write Hit	4	2
Write Miss	4	2

Table. Hit time/ Miss penalties

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