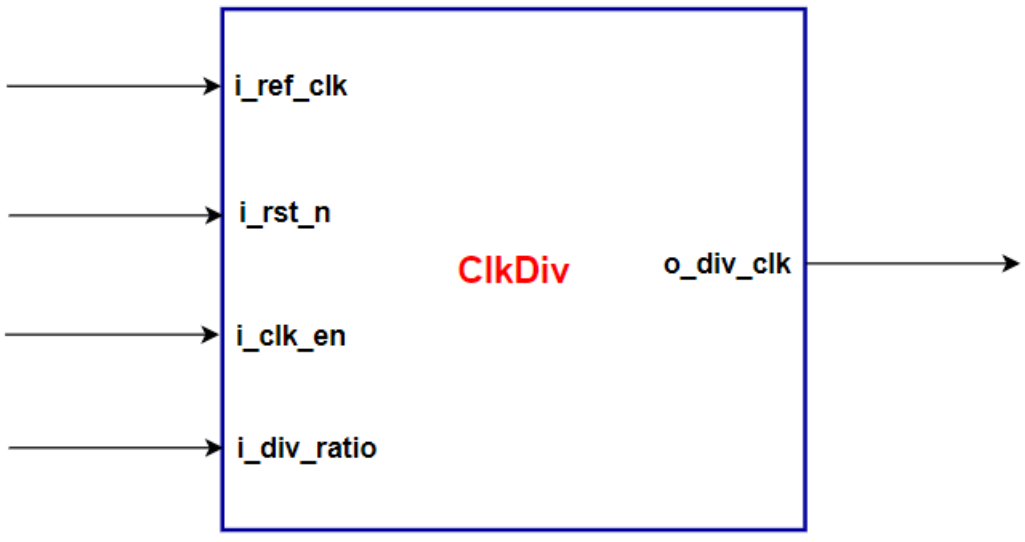
Clock Divider

Introduction: -

A clock divider is a circuit that takes an input signal of a frequency **fin** and generates an output signal of a frequency **fout**, where

fout = fin / n and ''n'' is an integer

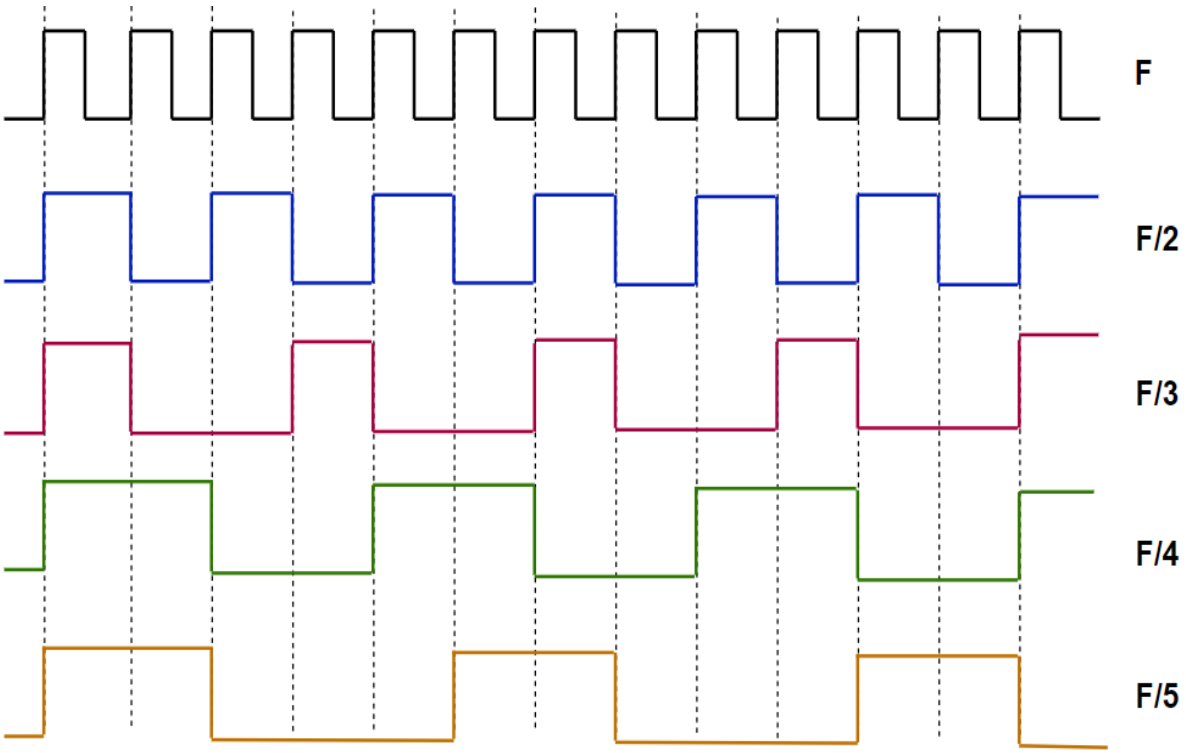
Block Interface



Ports Description

Signal Name	Description	Width
I_ref_clk	Reference Frequency	**1**
I_rst_n	Active Low Asynchronous Reset	**1**
I_clk_en	Clock Divider Block Enable	**1**
I_div_ratio	The divided ratio (integer value)	**1**

Waveforms



Requirements: -

1. Write a Verilog Code to capture the above specifications
2. Write a testbench to test generation of different frequencies of both odd and even divided ratio of the reference frequency