

Assignment 1.2

RST Synchronizer

Introduction: -

Asynchronous reset has many issues during de-assertion as it may violate the recovery and removal times of the Flip Flop, so **Reset Synchronizer** in digital circuit is needed to synchronize the de-assertion of the asynchronous reset with respect to the clock domain. In other words, a reset synchronizer manipulates the asynchronous reset to have synchronous de-assertion.

Block Interface



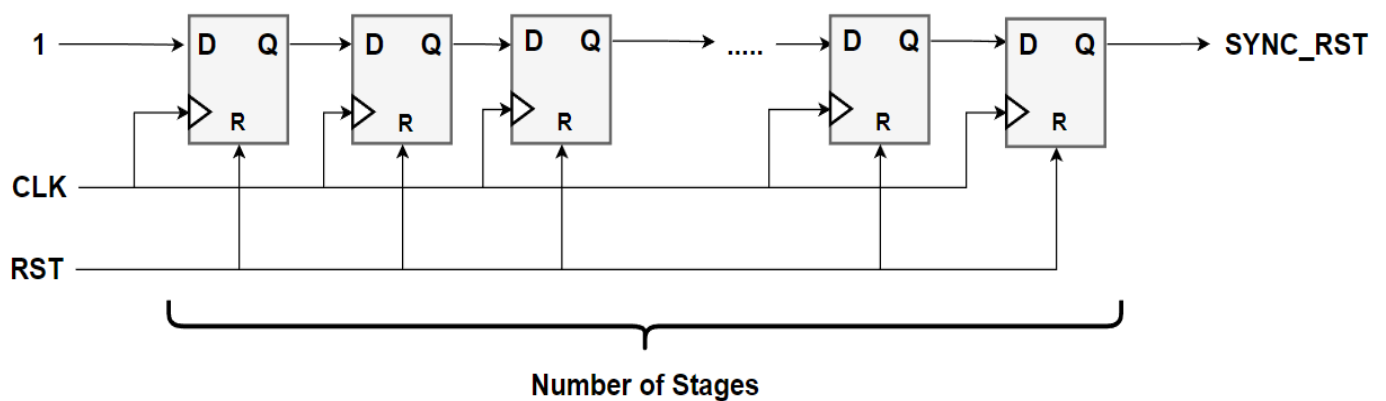
Ports Description

Signal Name	Description	Width
RST	Asynchronous reset	1
CLK	Destination domain clock	1
SYNC_RST	Synchronized Reset	1

Parameter Description

parameter Name	Description
NUM_STAGES	Number of Flip Flop Stages

Block Diagram



Hint: The above block diagram is used to synchronize the de-assertion of the active low reset.

Required

1. Write a Verilog Code to capture the above block diagram.
2. Write a testbench to validate the de-assertion of the asynchronous reset to be synchronous with the clock edge.