Assignment 3

16-bit ALU

Introduction: -

ALU is the fundamental building block of the processor, which is responsible for carrying out the **arithmetic**, **logic** functions, **Shift** functions and **Comparison** functions.

Specification:

- ALU **Operands** (A, B)
- ALU Result (ALU OUT)
- ALU operands and output Result are of **16-bit** width.
- ALU **Result** (ALU_OUT) is registered.
- The ALU function is carried out according to the value of the ALU_FUN input signal stated in the table in the following page and any other value for ALU_FUN not stated in the table, ALU_OUT must equal to 16'b0
- Arith_flag is activated "High" only when ALU performs one of the arithmetic operations (Addition, Subtraction, Multiplication, division), otherwise "LOW"
- Logic_flag is activated "High" only when ALU performs one of the Boolean operations (AND, OR, NAND, NOR, XOR, XNOR), otherwise "LOW"
- CMP_flag is activated "High" only when ALU performs one of the Comparison operations (Equal, Greater than, less than), otherwise "LOW"
- Shift_flag is activated "High" only when ALU performs one of the shifting operations (shift right, shift left), otherwise "LOW"

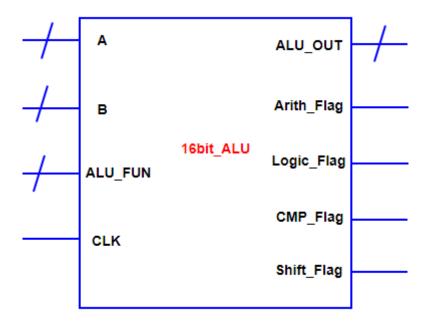
ALU_FUN Table

ALU_FUN	Operation	ALU_OUT
0000	Arithmatic : Addition	
0001	Arithmatic : Subtraction	
0010	Arithmatic: Multiplication	
0011	Arithmatic : Division	
0100	Logic : AND	
0101	Logic : OR	
0110	Logic : NAND	
0111	Logic : NOR	
1000	Logic : XOR	
1001	Logic : XNOR	
1010	CMP: A = B	Equal to 1
1011	CMP: A > B	Equal to 2
1100	CMP: A < B	Equal to 3
1101	SHIFT: A >> 1	
1110	SHIFT: A << 1	

Hint: Use Case statement to describe the behavior of this table and use default case if needed.

Hint: You can use if statement inside case branches

Block Interface



- 1. Write a Verilog Code to capture the above specifications as well as the synthesis diagram of your code.
- 2. Write a testbench to test all the ALU functions with operating clock frequency 100 KHz