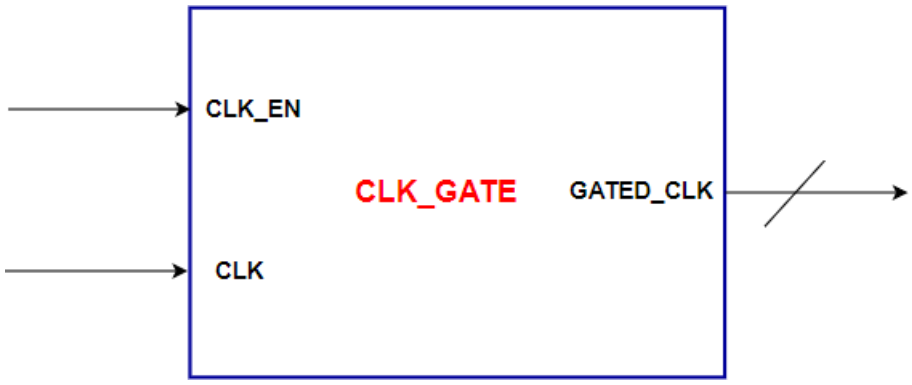
Clock Gating

Introduction: -

Clock Gating is the most popular and effective method to reduce **dynamic power consumption** by switching the clock off in idle duration of the block

Block Interface



Ports Description

Signal Name	Description	Width
CLK	Clock Signal	**1**
CLK_EN	Clock Enable	**1**
GATED_CLK	Gated Clock signal	**1**

Requirements: -

Write a Verilog Code of the above specifications