

AND LD LDA STA  
CLA INC CMA

Instruction Register

Fetch: R<sub>1</sub>T<sub>1</sub>

IR

IR as Source:

R<sub>1</sub>T<sub>2</sub>

Decoder

IR (12-14)

J → IR (15)



Design Read in memory

source ← memory

$\bar{R}T_1 : IR \leftarrow M[AR]$

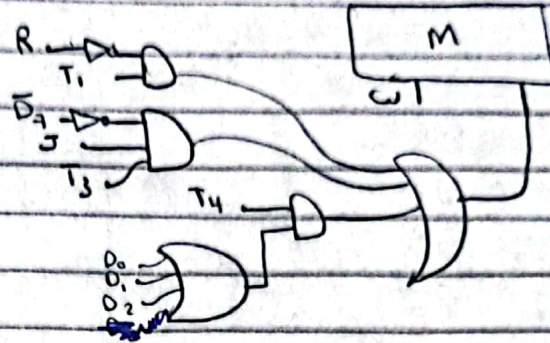
$\bar{D}_7 T_3 : AR \leftarrow M[AR]$

$D_0 T_4 : OR \leftarrow M[AR]$

$D_1 T_4 : OR \leftarrow M[AR]$

$D_2 T_4 : OR \leftarrow M[AR]$

~~$D_3 T_4 : OR \leftarrow M[AR]$~~



$$Read = \bar{R}T_1 + \bar{D}_7 T_3 + T_4 (D_0 + D_1 + D_2 + \bar{D}_3)$$

Design Write in memory

destination ← memory

$R T_1 : M[AR] \leftarrow TR$

$D_3 T_4 : M[AR] \leftarrow AC$

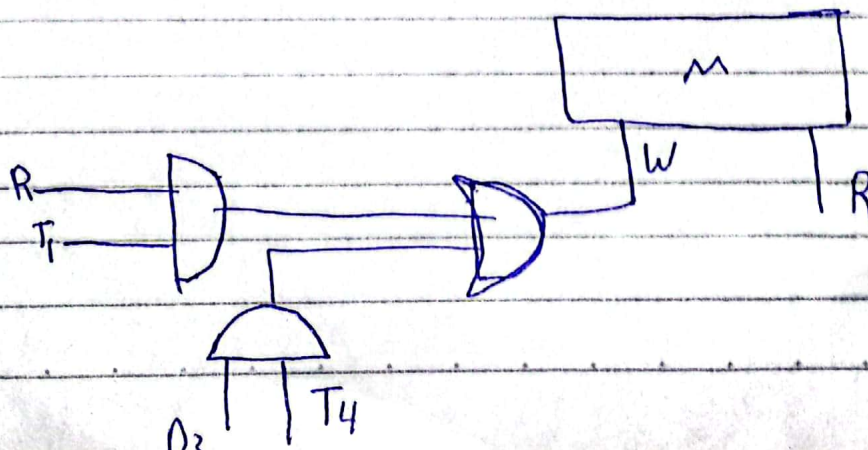
~~$D_5 T_4 : M[AR] \leftarrow PC$~~

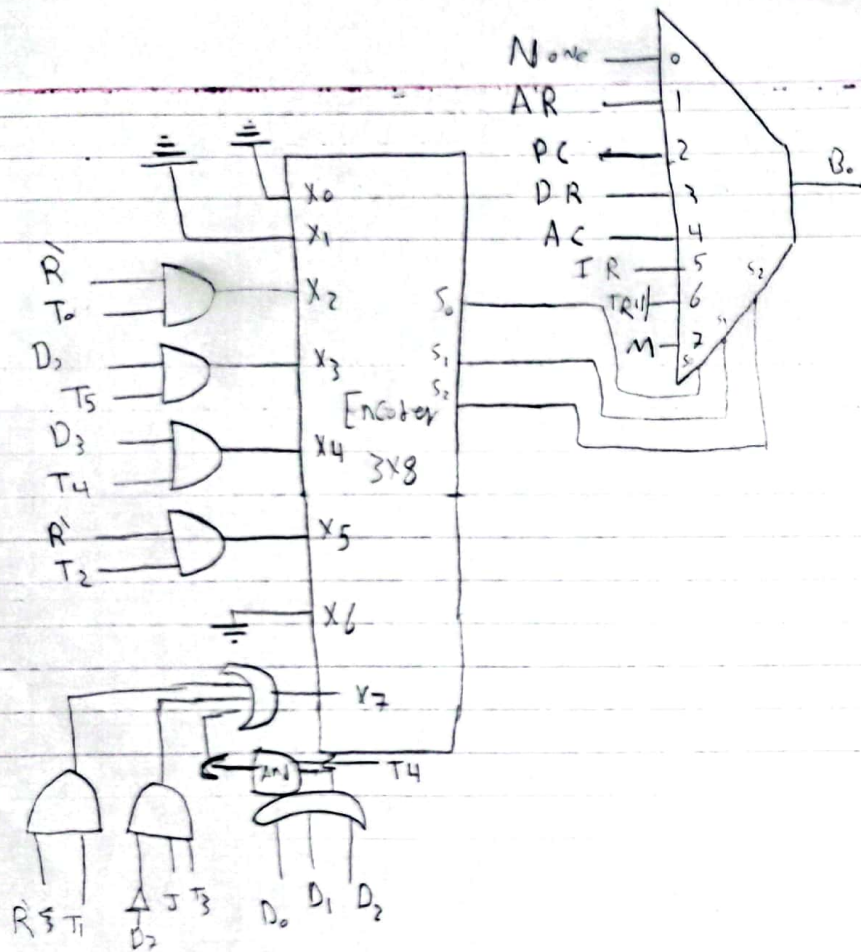
~~$D_6 T_6 : M[AR] \leftarrow OR$~~



$$Write = RT_1 + (D_3 + D_5 + D_6)T_4$$

write  $RT_1 + D_3 T_4$



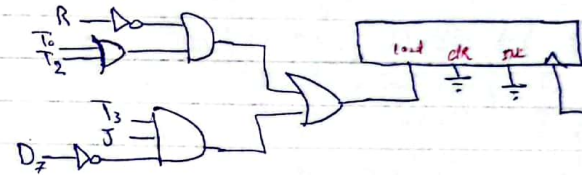


LD

Setch  $R'T_0$ Decode  $R'T_2$ Indirect  $D_7 J T_3$ 

INR

CIR



AR

 $AR \leftarrow PC$  $AR \leftarrow IR(0-11)$  $AR \leftarrow M[AR]$  $\bar{R} \cdot (T_0 + T_2) + \bar{D}_7 J T_3$ 

AND

ADD

LDA

STA

CIA

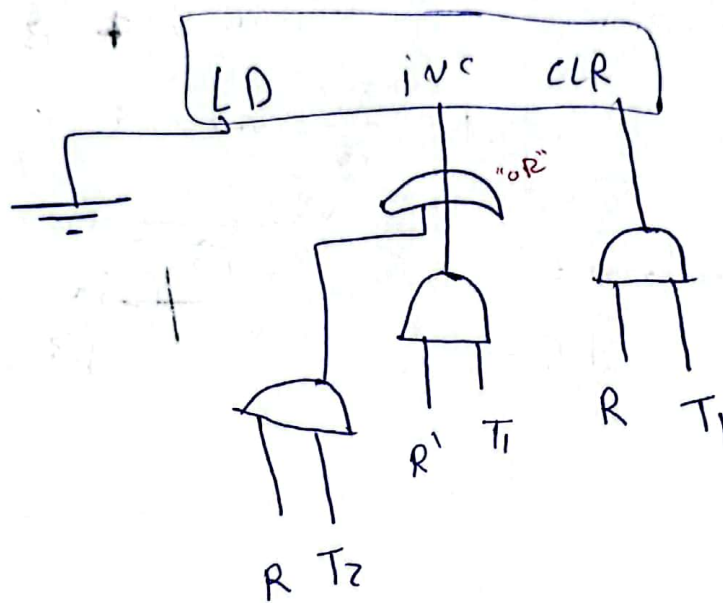
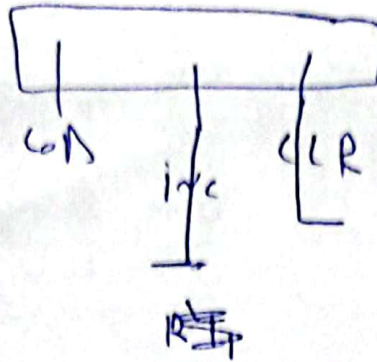
CMA

INC



~~AND~~  $D_0 T_4$

$\bar{R}$



PC

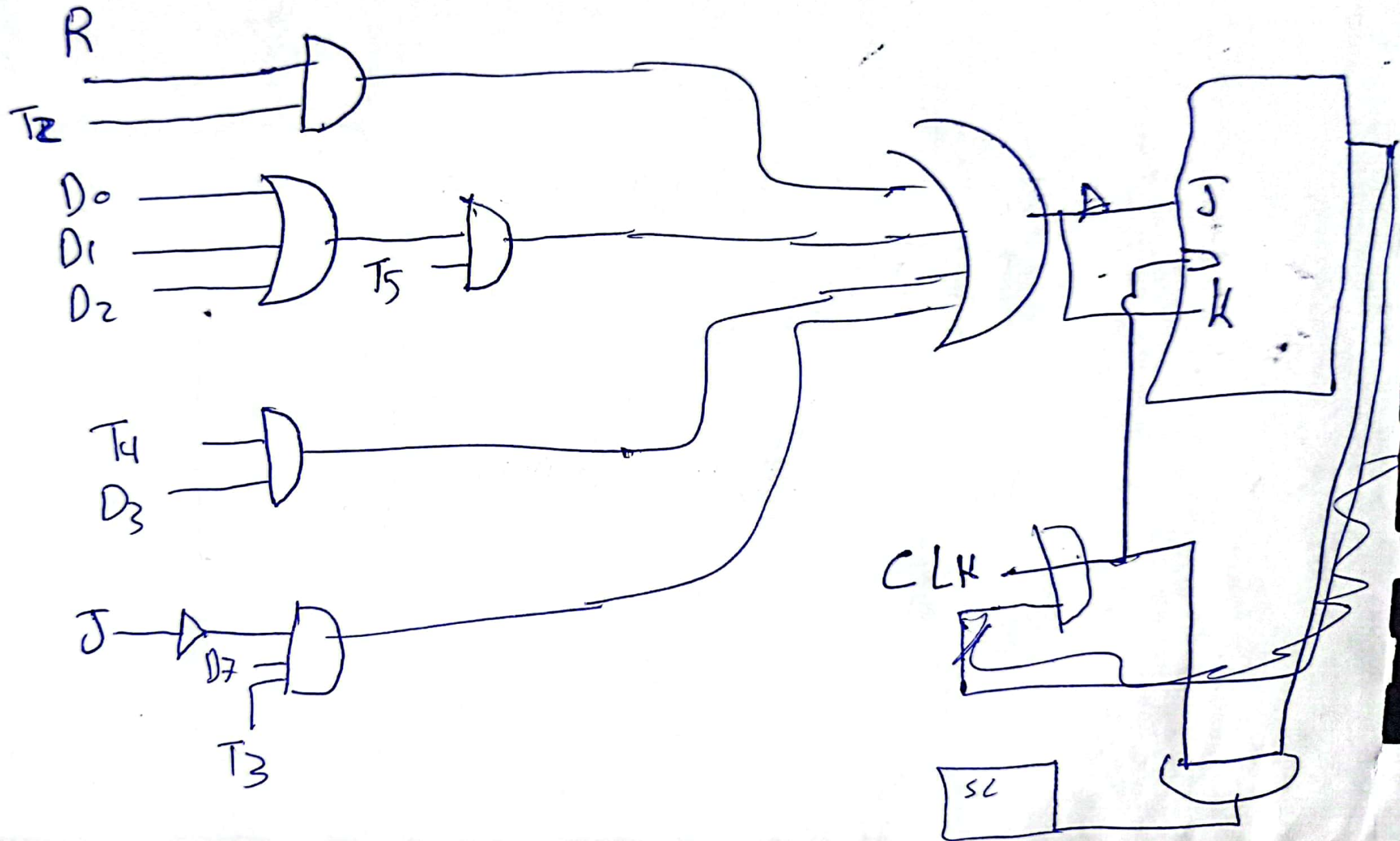
$$RT_2 + D_0 T_5 + D_1 T_5 + D_2 T_5 + D_3 T_4 + D_7 \bar{J} T_3$$

SC

~~$RT_2$~~

$$RT_2 + (D_0 + D_1 + D_2) T_5 + D_3 T_4 + D_7 \bar{J} T_3$$





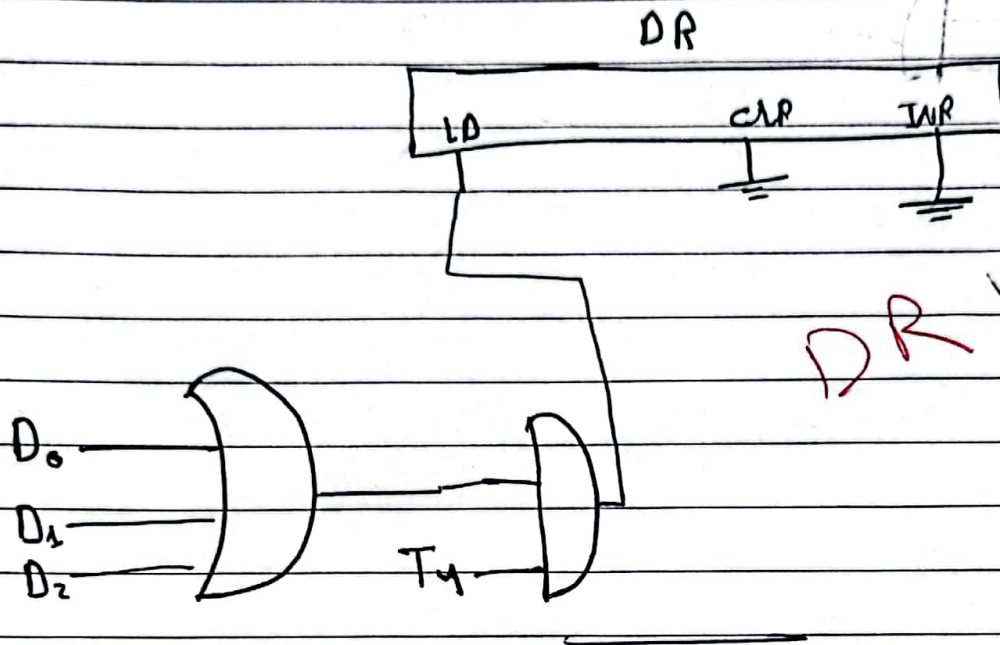
SUBJECT: \_\_\_\_\_

AND - Add - LDA - ST A

CLA - INR - CMA

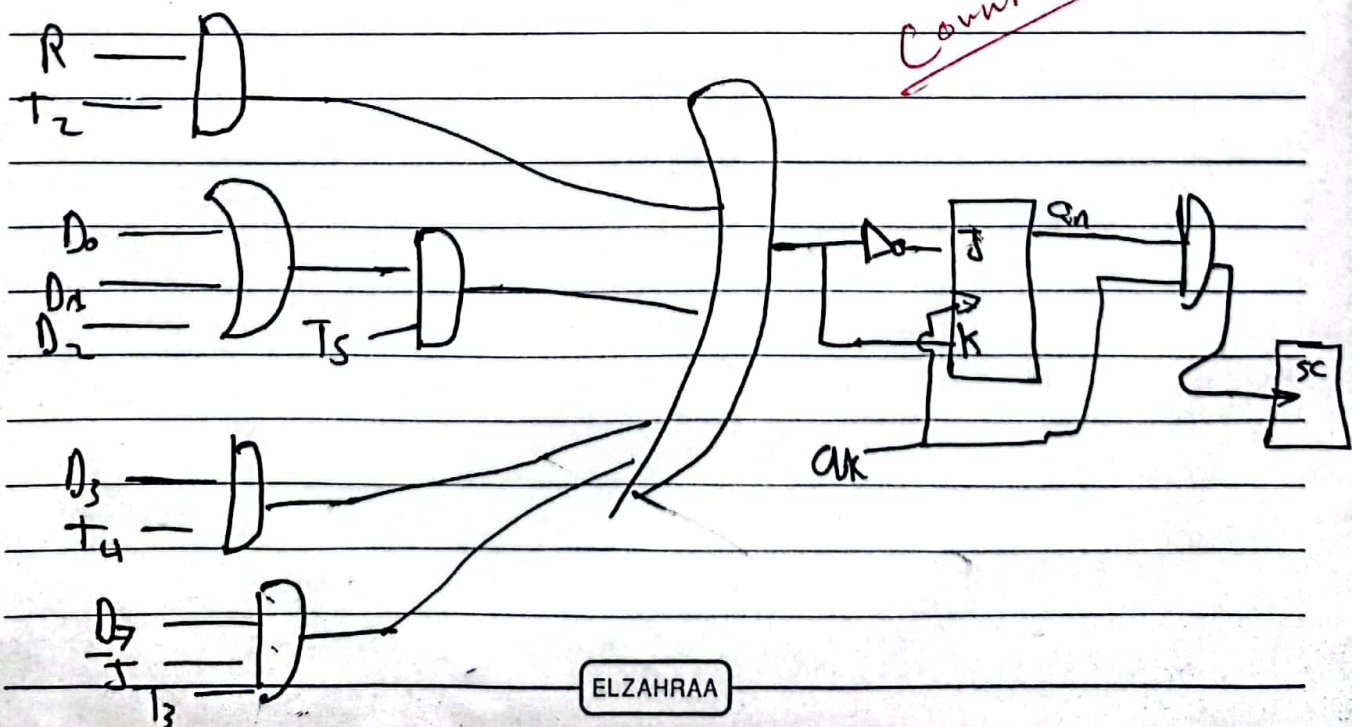
DATE: \_\_\_\_/\_\_\_\_/\_\_\_\_

$$LDA: D_0T_4 + D_1T_4 + D_2T_4 = T_4(D_0 + D_1 + D_2)$$



$$RT_2 + D_0T_5 + D_1T_5 + D_2T_5 + D_3T_4 + D_7\bar{J}T_3$$

$$RT_2 + T_5[D_0 + D_1 + D_2] + D_3T_4 + D_7\bar{J}T_3$$





SUBJECT: \_\_\_\_\_

DATE: / /

$D_2 T_5$

OR As a source

