Basic Mano Computer With Verilog

Team Member

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About The Project

- ## Components
  1. CLK
  2. Memory
  3. AR
  4. PC
  5. DR
  6. AC
  7. IR
  8. SC
  9. ALU
  10. MUX
  11. Decoder
  12. Encoder

- ## Instructions
  1. LDA (load accumulator from memory)
  2. AND (bitwise AND)
  3. ADD (addition)
  4. INC (increment accumulator)
  5. CMA (complement accumulator)
  6. CLA (clear accumulator)
  7. CME (complement E)

Control functions and Micro operation for the Basic computer.

Fetch	$R'T_0$:	AR ← PC
	$R'T_1$:	IR ← M[AR], PC ← PC + 1
Decode	$R'T_2$:	D0, ...D7 ← Decode IR (4-6),
		AR ← IR (0-3), I ← IR (7)
Indirect	D'_7IT_3:	AR ← M[AR]

→ Memory – Reference:

AND	D_0T_4:	DR ← M[AR]
	D_0T_5:	AC ← AC ^ DR, SC ← 0
ADD	D_1T_4:	DR ← M[AR]
	D_1T_5:	AC ← AC +DR, E ← COUI, SC← 0
LDA	D_2T_4:	AC ←M[AR]
	D_2T_5:	AC ← DR, SC ← 0

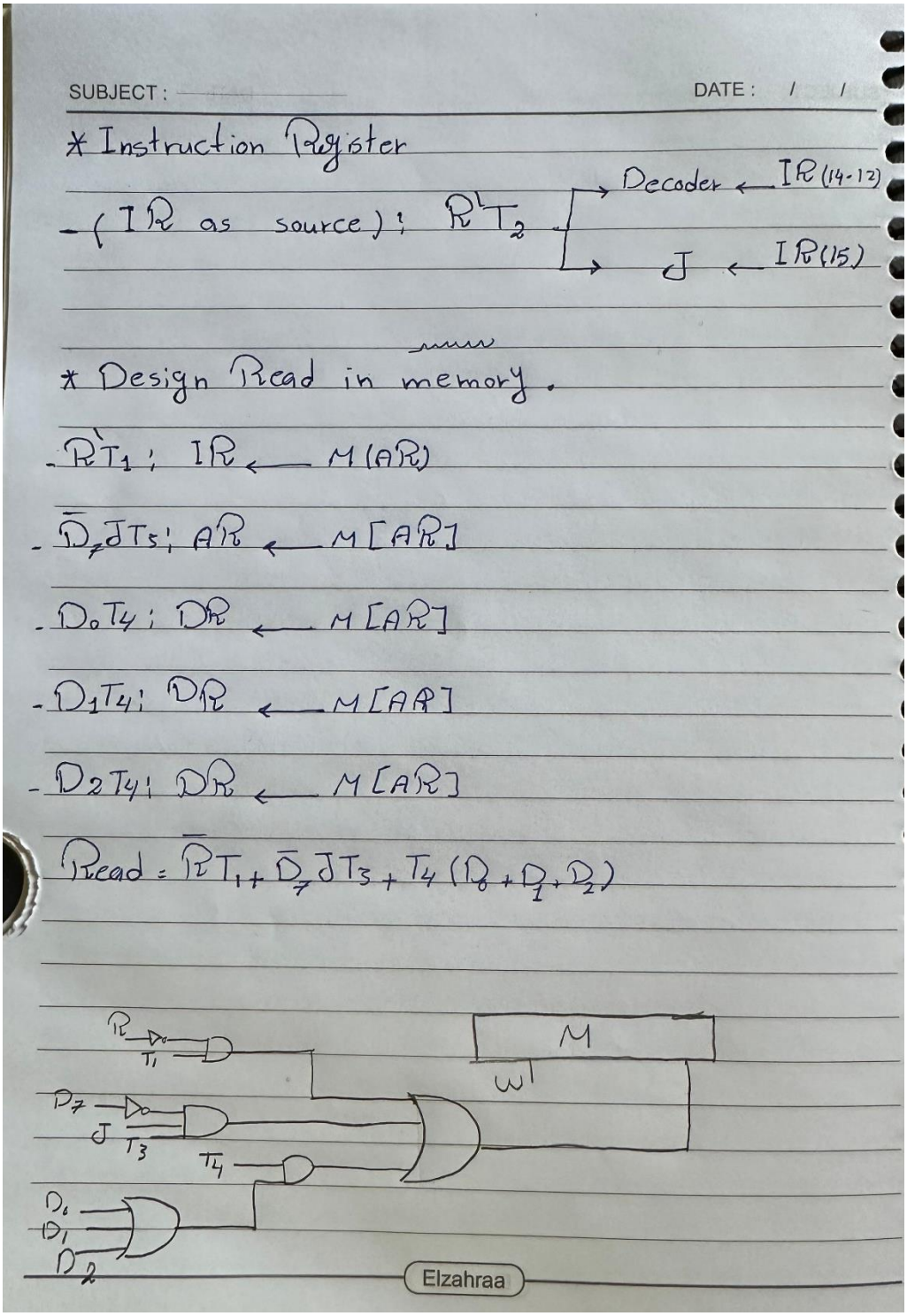
→ Register – Reference:

$D_7I'T_3$= r (common to all register – reference instructions)

$IR(i) = B_i$ (i = 0, 1, 2,3)

	r:	SC ← 0
CLA	rB_1:	AC ← 0
INC	rB_2:	AC ← AC + 1
CMA	rB_3:	AC ← ~AC

Project Designs



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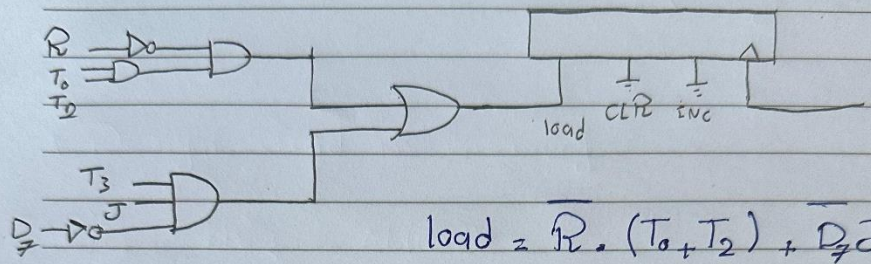
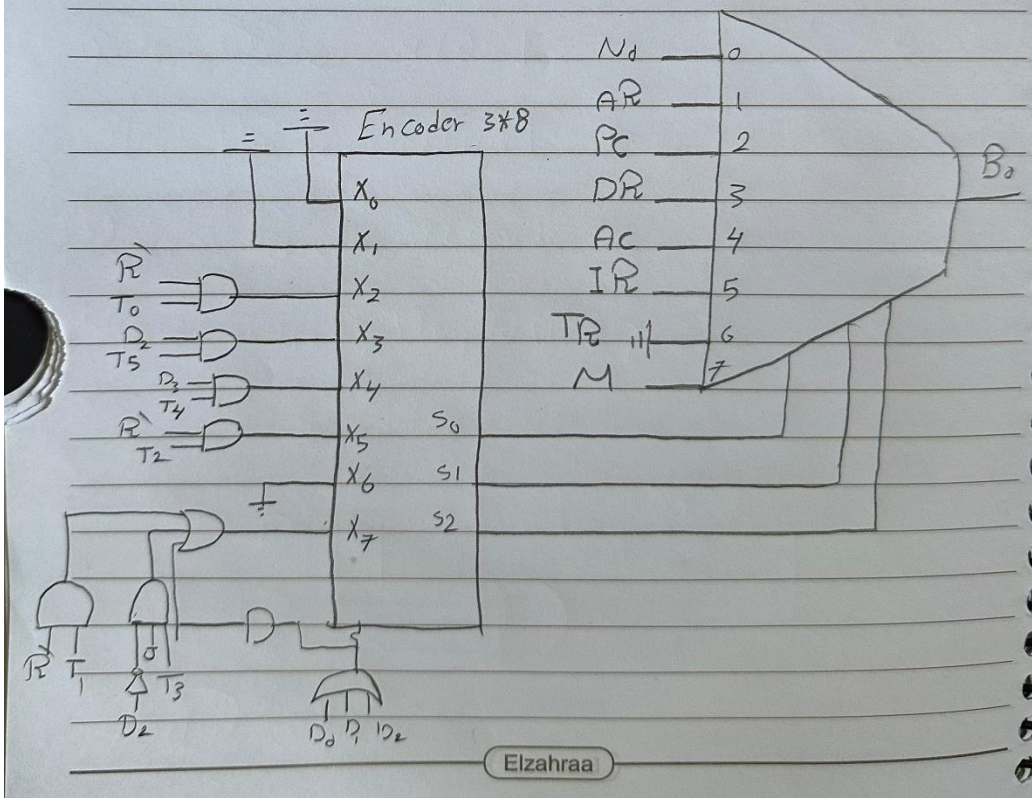
* AR → Address Register

Load Design in AR



$load = \overline{R} \cdot (T_0 + T_2) + D_7 J T_3$

* Common bus Design



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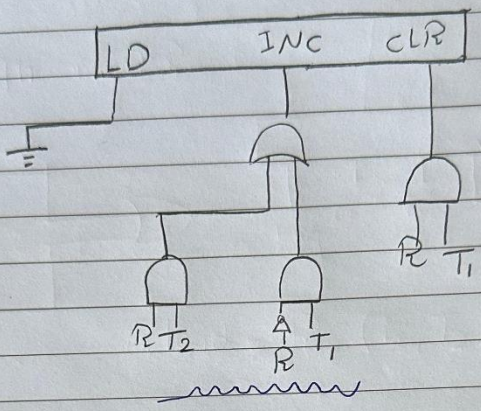
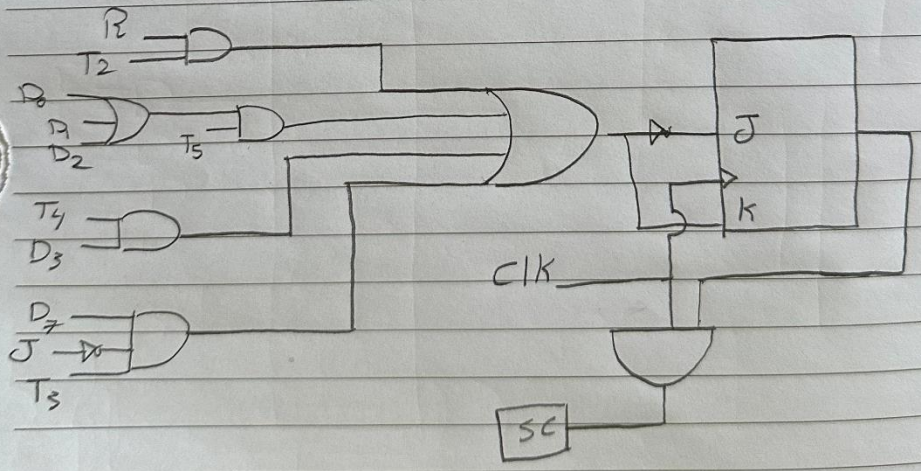
* Design clR and INC in PC .



* Design SC

$$R \cdot T_2 + D_0 T_5 + D_1 T_5 + D_2 T_5 + D_3 T_4 + D_7 \bar{J} T_3$$

$$= R T_2 + (D_0 + D_1 + D_2) T_5 + D_3 T_4 + D_7 \bar{J} T_3$$



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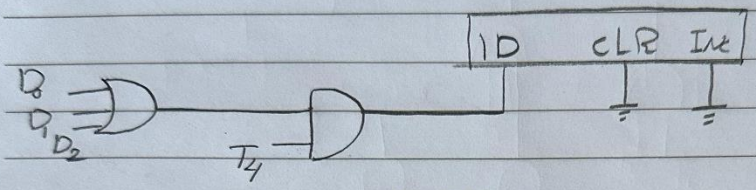
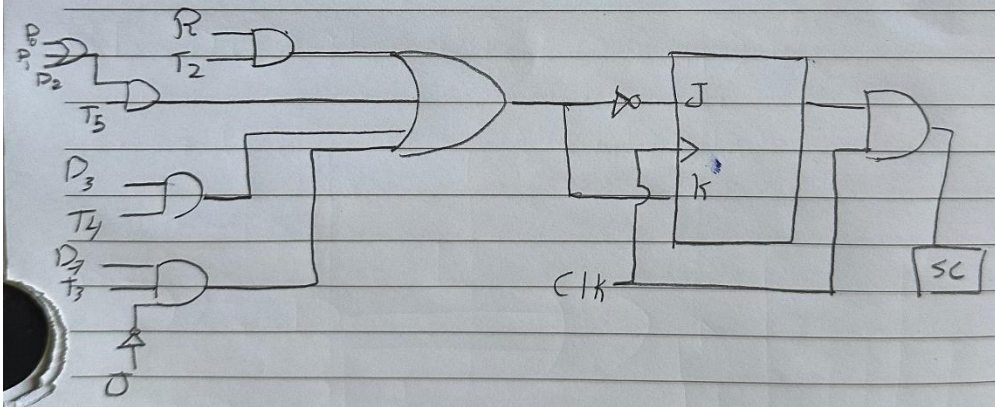
* Design LD in DR.

$LD = T_4 (D_0 + D_1 + D_2)$



* CLK Design in SC.

$CLK = \bar{R} T_2 + T_5 [D_0 + D_1 + D_2] + D_3 T_4 + D_7 \bar{J} T_3$



Processes

$0 \leftarrow 2F_H$	LDA	$AC = 45_H$
$1 \leftarrow 0E_H$	AND	$AC = 01_H$
$2 \leftarrow 1D_H$	ADD	$AC = 30_H$
$3 \leftarrow 74_H$	INC	$AC = 31_H$
$4 \leftarrow 78_H$	CMA	$AC = CE_H$
$5 \leftarrow 72_H$	CLA	$AC = 0_H$
$6 \leftarrow 71_H$	CME	$E = 1_H$
$D \leftarrow 2F_H$		
$E \leftarrow B9_H$		
$F \leftarrow 45_H$		

GitHub For Project

https://github.com/ahmed-rdwan/Mano-Basic-Computer-Using-verilog-language