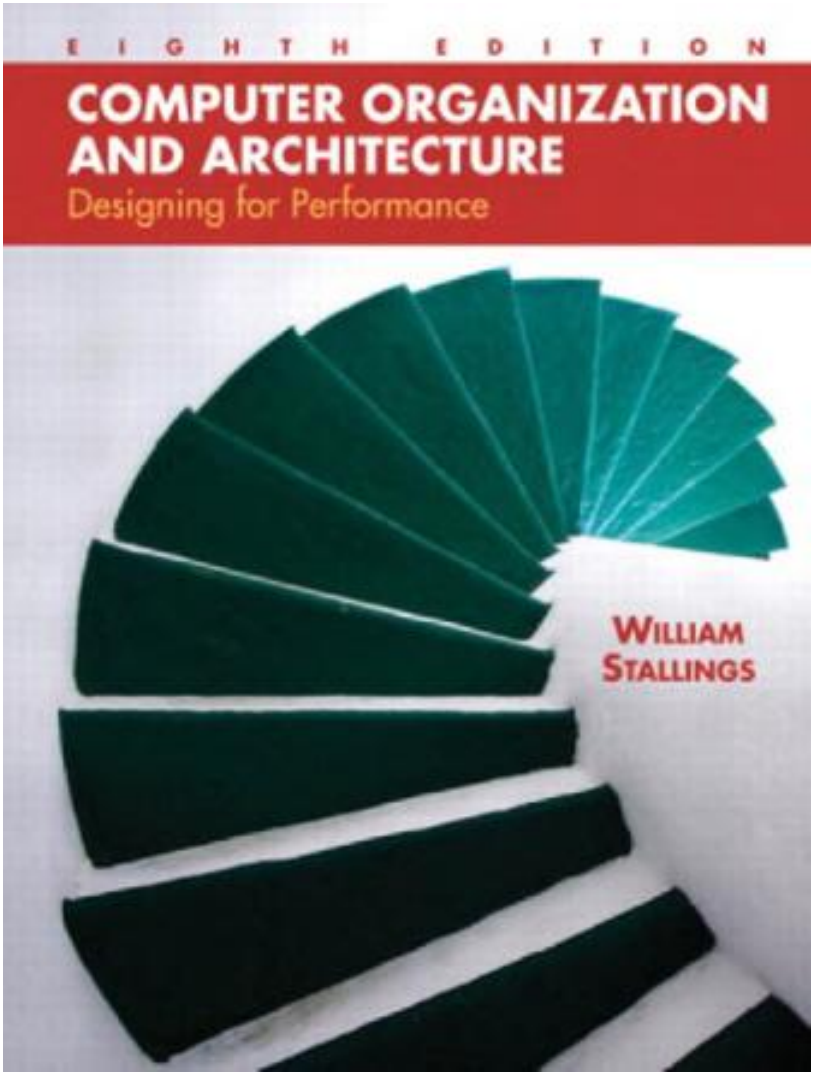
CSC220 – Computer Organization I

FALL SEMESTER 2023

Instructor: Prof. Khaled Hussein



Sheet 5 – Cache Memory

Topic	Duration
Cache Memory	2 hours

Document Revision History

Revision Number	File Name	Date
1	Sheet 5 – Cache Memory	

a. True or False:

1) Cache memory on hard disk is considered as internal memory of computer.
2) External memory is sometimes faster than internal memory's as in the case of the SSD hard disk.
3) One block can contain more than a word.
4) Hard disk and flash memory are addressed word by word.
5) Word size is used as a metric to measure the performance of any memory.
6) Memory cycle time must be less than memory access time.
7) Random access memory (RAM) apply the concept of memory cycle time.
8) The time required for the memory to "recover" before next access is Recovery time.
9) The memory cycle time is concerned with the processor.
10) Sequential access method starts at the beginning of memory and read in order till it finds the required location.
11) Cache memory utilizes the direct access method when dealing with CPU.
12) Both RAM and cache memory are independent on the previous location of data.
13) A comparison with contents of a portion of the stored data is made to achieve sequential access.
14) According to memory hierarchy, magnetic tapes lie at the bottom of the pyramid with the lowest speed in dealing with data among other memory devices.
15) Static RAM is slower that cache.
16) In a short period of time, the CPU is primarily working with fixed blocks of memory references.
17) The main memory consists of words, these words are grouped into blocks for mapping purposes and each block can contain a different number of words.
18) Cache includes tags to identify which block of main memory we need to retrieve.
19) Cache hit is when data is present in cache and we transfer it to CPU (fast) while cache miss is when data isn't present and we read the required block from main memory to cache then we transfer it to CPU (slow).

20) Mapping function is an algorithm for determining which main memory block currently occupying a cache line.

21) It is possible to arrive at a single “optimum” cache size for all architectures.

22) Cache is organized based on the mapping function used in the architecture.

23) In direct mapping, the number of locations in the main memory is the number of blocks that can be found in one line of cache.

24) In direct mapping, cache searching gets expensive.

25) In associative mapping, a main memory block can be loaded into any line of cache.

26) Replacement algorithm of direct mapping states that if cache misses, one line must be replaced by the required block data from main memory.

27) Replacement algorithms of associative mapping are implemented in software to achieve high speed.

28) The most effective/popular replacement algorithm for associative mapping is LFU. In write back policy, update/use bit is set when updating main memory.

29) As the block size increases from very small to larger sizes, the hit ratio will at first increase because of the principle of locality.

b. MCQ:

1) All of the following are examples of internal memory except ……..

   a) RAM b) Cache on hard disk c) Hard disk d) Cache on CPU

2) Internal memory deals with ……., while external memory deals with ……...

   a) Byte, word b) Word, block c) Word, byte d) Block, byte

3) The word size of any internal memory is determined by the size of …….

   a) Data bus b) Address bus c) Control size d) DR

4) …….. is a parameter used to measure the how good a memory is w.r.t. capacity.

   a) Access time b) Memory cycle time c) Transfer rate d) Word size

5) The time required before a second access can commence.is called ……...

   a) Memory cycle time b) Access time c) Transfer time d) Recovery time

6) The number of words of any internal memory is determined by the size of …….

a) Data bus b) Address bus c) Control size d) DR

7) ……. is an access method where individual blocks have unique address and the access time depends on the required location and the previous location of data.

a) Random access method b) Direct access method
c) Associative access method d) Sequential access method

8) In random access method, the access time required to access the next location is ……. the time required to access the last location.

a) More than b) Less than c) Multiple d) Equal to

9) ……. is an example for a memory device that utilizes the sequential access method.

a) Tape b) RAM c) Hard disk d) Cache

10) RAM is based on ……. technology, disk & Tape are based on ……. technology and CD & DVD are based on ……... technology.

a) Semiconductor, Magnetic and Optical b) Magnetic, Semiconductor and Optical
c) Optical, Magnetic and Semiconductor d) Magnetic, Optical and Semiconductor

11) For a memory with 5 lines address bus and a cache where each line can contain 4 words, the number of lines of cache needed to store all the words of the memory is ….

a) 6 b) 7 c) 8 d) 9

12) The size of cache have to be …….. for the cost purpose, and also……. so that the overall average access time is close to that of the cache alone.

a) small, small b) large, small c) small, large d) large, large

13) For a 32 Mbyte RAM,64 Kbyte cache and each block in cache is 8 bytes, how many locations in memory that can occupy the whole cache?

a) 256 b) 1024 c) 512 d) 128

14) In direct mapping, we only compare the tag field of memory address with the tag of exactly one line in cache because ……

a) Each byte in cache must be loaded into one byte in memory.
b) Each block from memory must be found in only one line in cache.
c) Each block in memory has unique tag.
d) Each block in cache must be loaded into one byte in memory

15)……. is a mapping function where the tag of each line of cache is compared to the tag in the memory address.

a) Associative b) Direct c) Indirect d) Set associative

16)Write policy is used to ensure ……..

a) The consistency/validation of data in cache and memory.
b) The efficiency of data transfer between cache and memory.
c) The redundancy of data between cache and memory.
d) The capability of the system to store data.

c. Problems:

1) What are the differences among sequential access, direct access, associative access and random access?
2) What is the general relationship among access time, memory cost, and capacity?
3) What is an addressable unit?
4) What are the 2 most important characteristics of a memory?
5) Mention and explain the parameters used to measure how good a memory can be w.r.t performance and capacity.
6) Explain and give 1 example for the 4 memory access methods then state if each one of them is dependent or independent on current or previous location of data.
7) What is meant by volatility, erasability and power consumption of different memory technologies.
8) For a memory with 4-bit address lines, 8-bit word and a cache with 4 lines, how many words are there in each line of cache? (To store the whole memory)
9) For a direct-mapped cache, a main memory address is viewed as consisting of three fields. List and define the three fields.
10) Mentions the pros and cons of direct mapping and associative mapping.
11) Why do we have to check that memory is up to date before replacing a line/block in cache.
12) Discuss each of the following:
    i. “Write through” policy
    ii. “Write back” policy
    iii. What are the pros and cons of write through policy?

13) Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

   i. How is a 16-bit memory address divided into tag, line number, and byte number?

   ii. How many total bytes of memory can be stored in the cache?

   iii. Why the tag is also stored in the cache?

d. Assignment:

1) Mention the full hierarchy list of memory devices and the technology used to make each one of them.

2) Explain the cache operation (cache hit and cache miss).

3) In the typical cache organization, how does the Cache connect to the processor?

4) Mention and explain the techniques used in mapping function.

5) What is meant by LRU, FIFO and LFU replacement algorithms.

Thank You