

Project 2

Team Members:

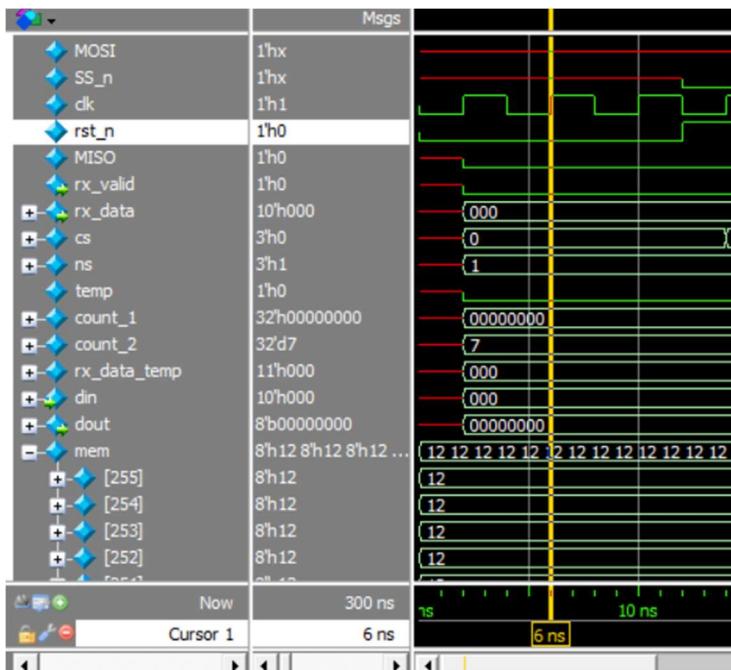
Youssef Mohamed Mamdoh

Ahmed Hossam Rafik algamal

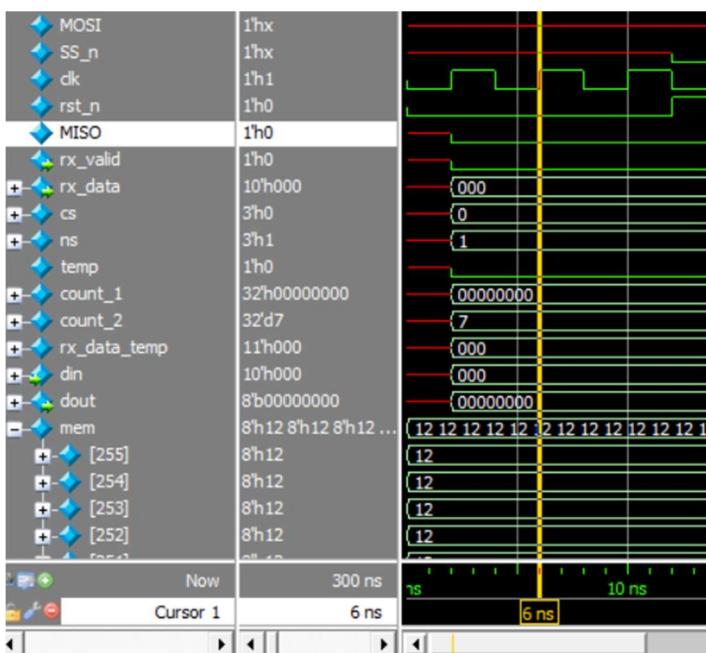
Moustafa saad Dawood

Waveform snippets:

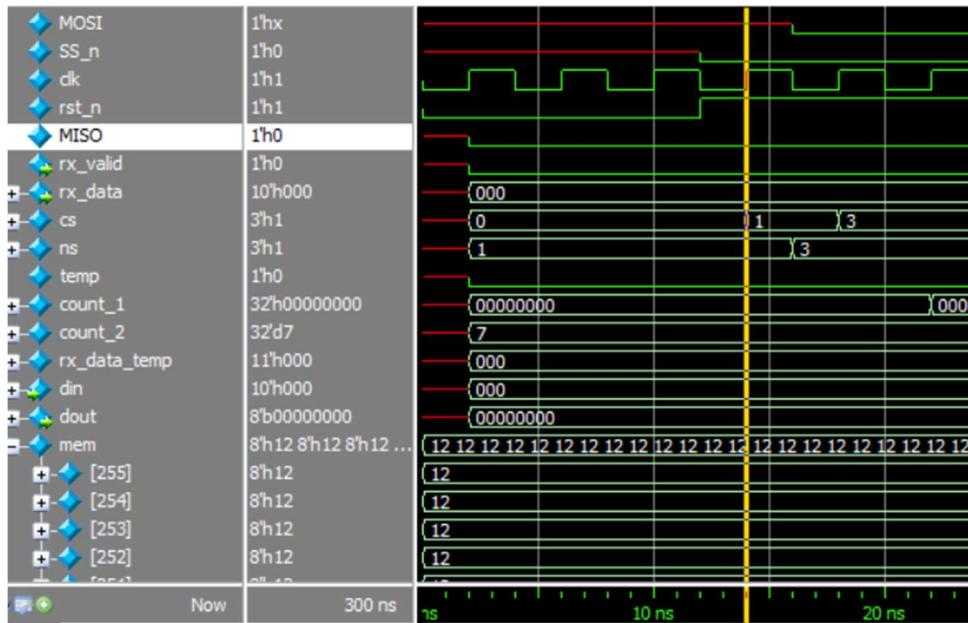
When reset is active:



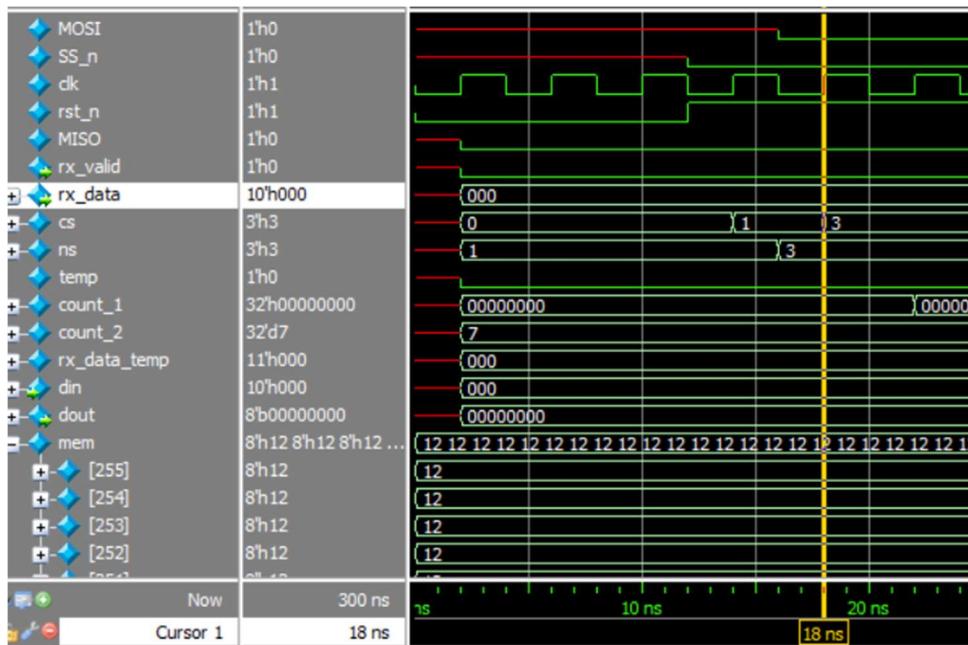
Rst is inactive and cs=IDLE:



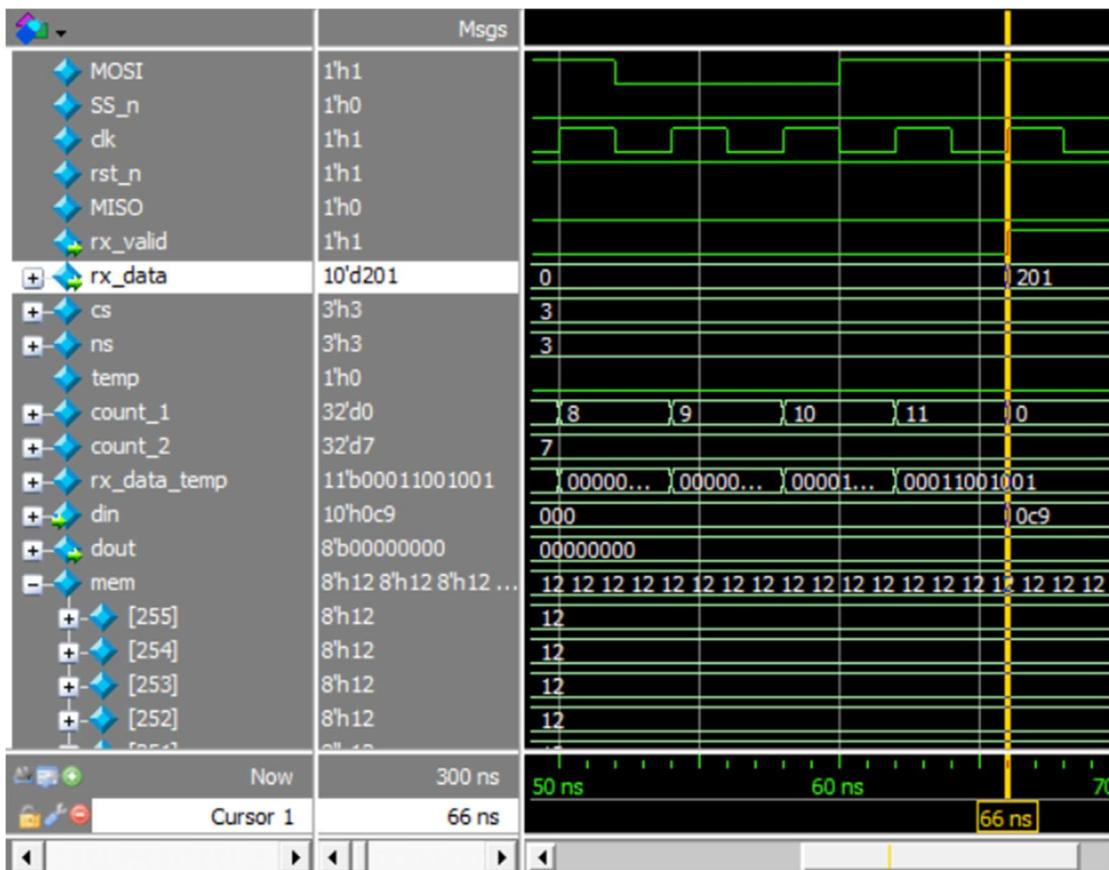
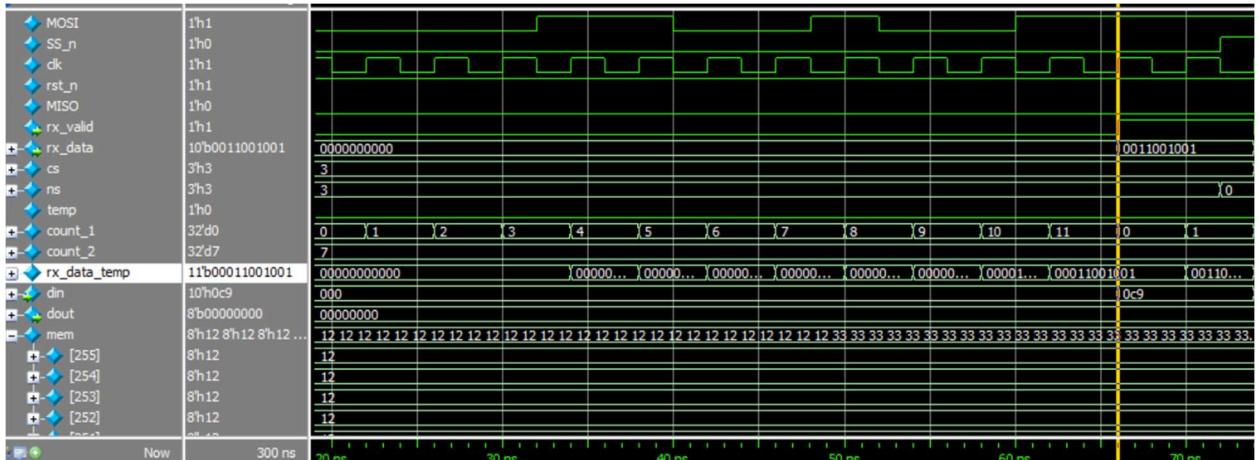
SS_n=0 and cs=CHK_CMD (1):



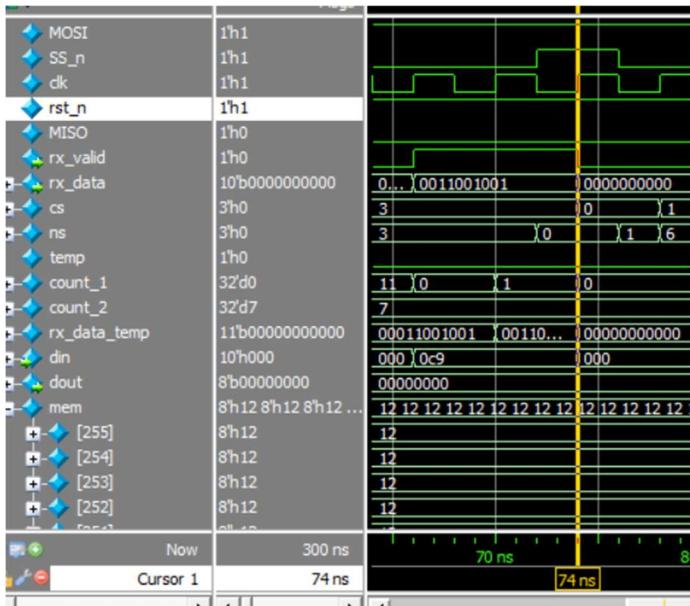
SS_n=0, MOSI=0 and cs=WRITE(3):



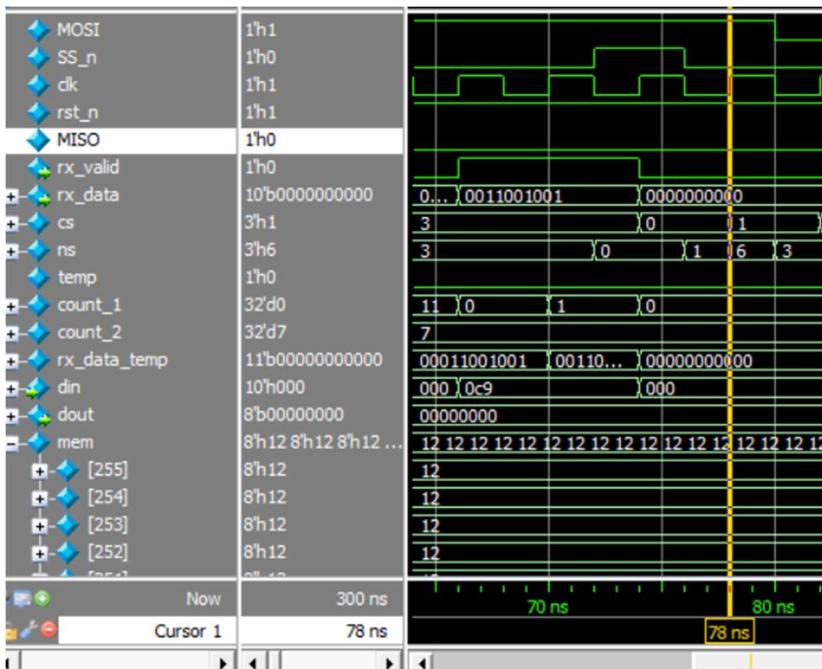
After 11 clock cycles (1 for 1st control signal and another 10 for data): rx_valid=1 and rx_data is loaded by the 10 bits address



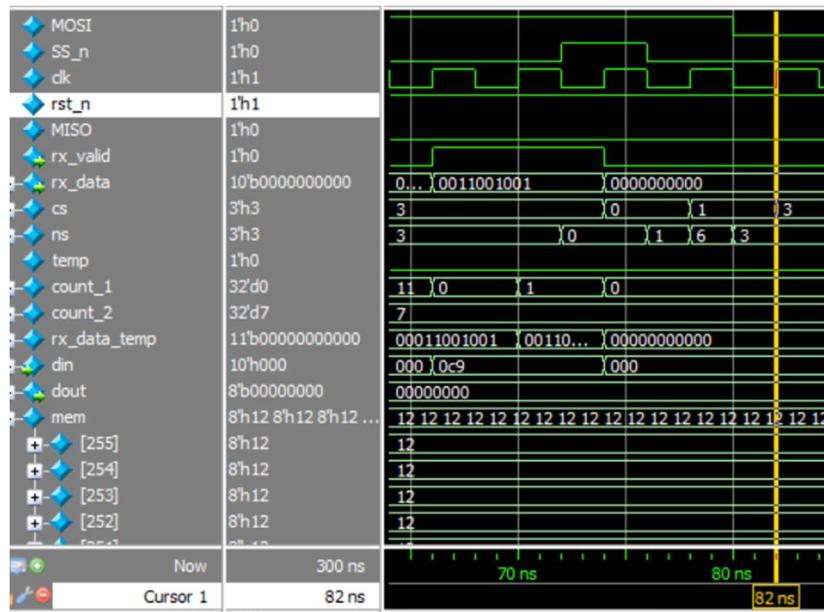
SS_n=1 and cs= IDLE:



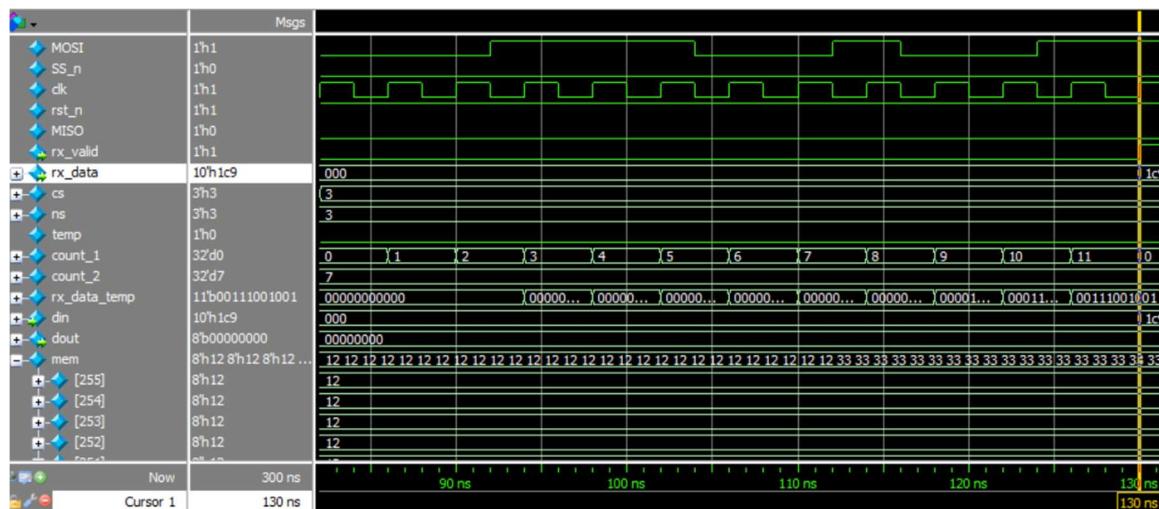
SS_n=0 and cs=CHK_CMD:



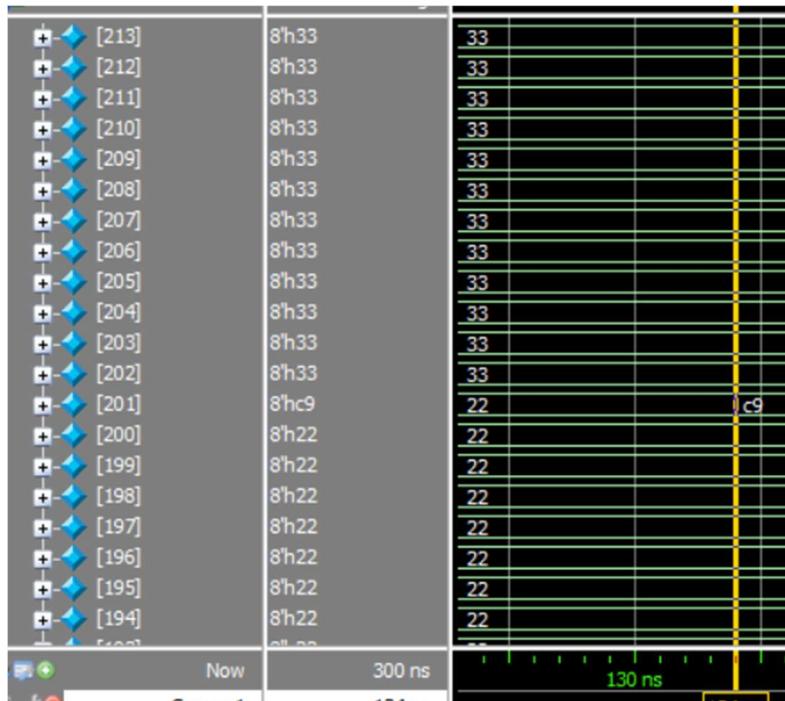
MOSI=1 and cs=WRITE:



After 11 clock cycles (1 for 1st control signal and another 10 for data): rx_valid=1 and rx_data is loaded by the 10 bits data

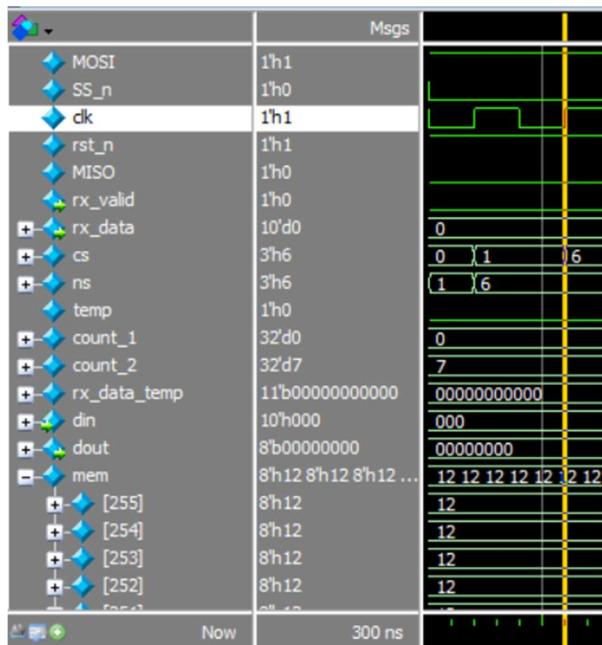


Memory loaded with data:

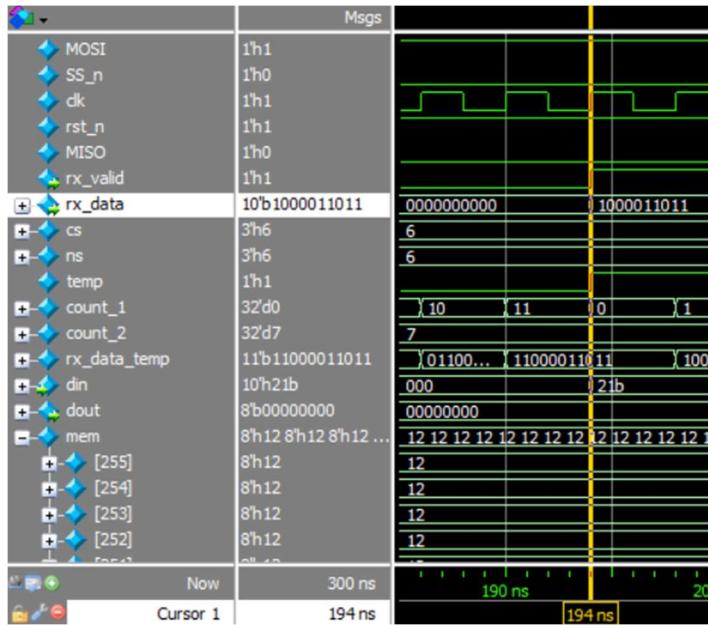


Then SS_n=1 so, cs=IDLE then SS_n=0 so, cs=CHK_CMD

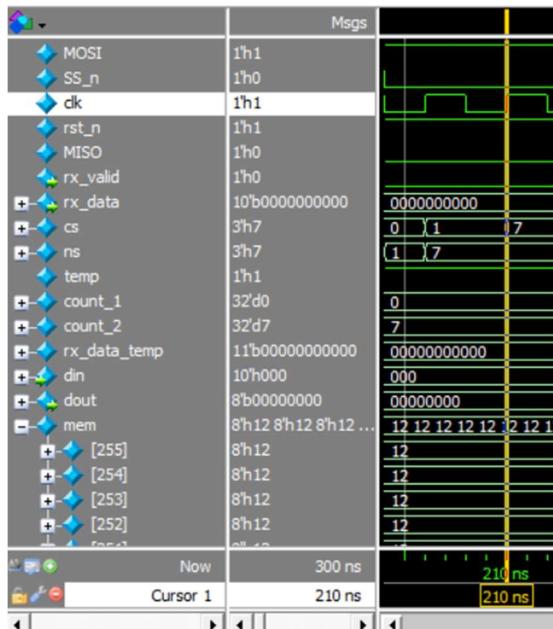
Then MOSI=1 and temp(internal signal)=0 so,
cs=READ_ADD:



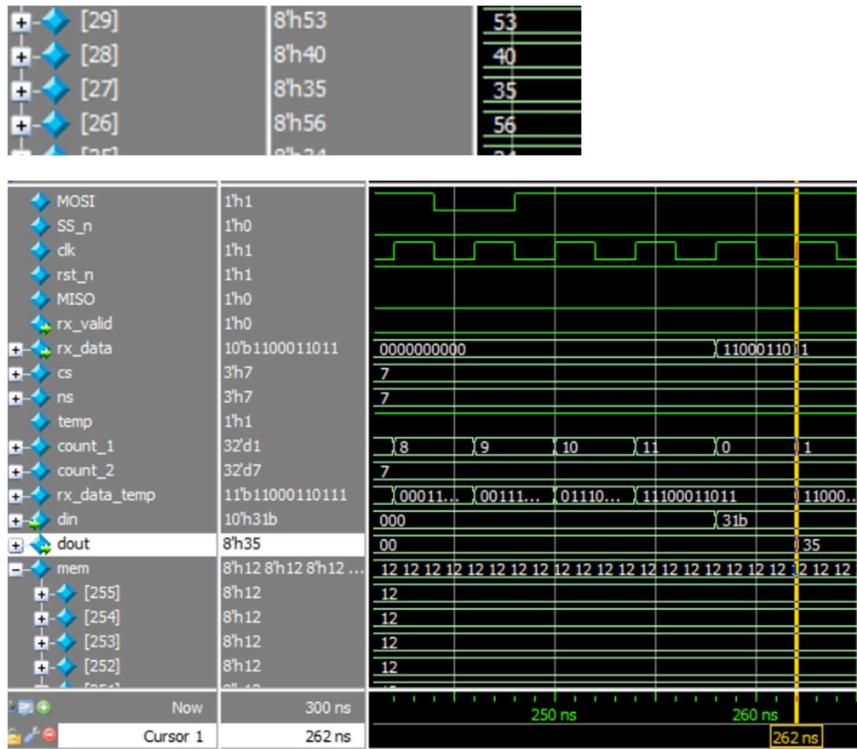
After 11 clock cycles (1 for 1st control signal and another 10 for data): rx_valid=1 and rx_data is loaded by the 10 bits address and we will take the memory address which is least significant 8 bits (27 in decimal) and temp will be 1



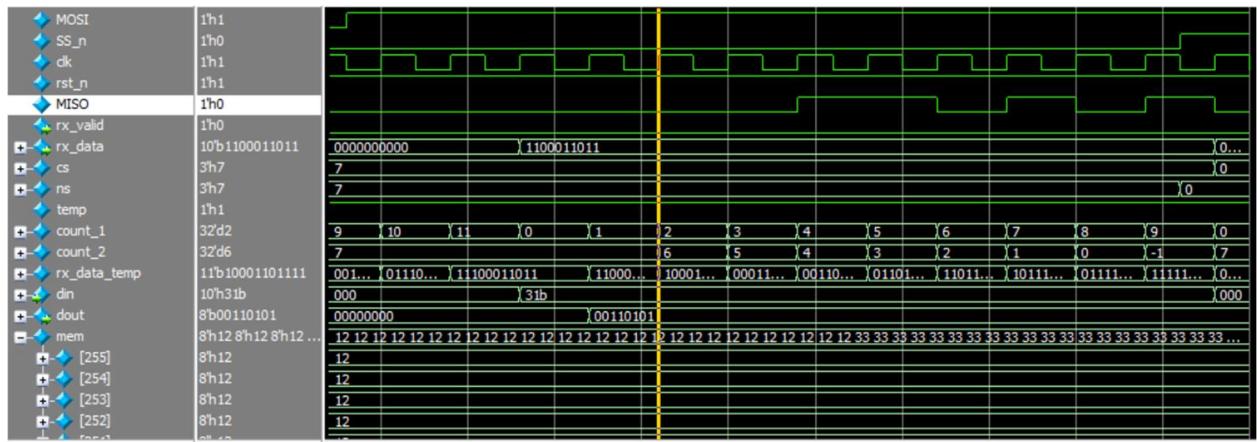
After that SS_n=1 so, cs=IDLE then SS_n=0 so, cs=CHK_CMD then MOSI=1 and temp=1 so, cs=READ_DATA:



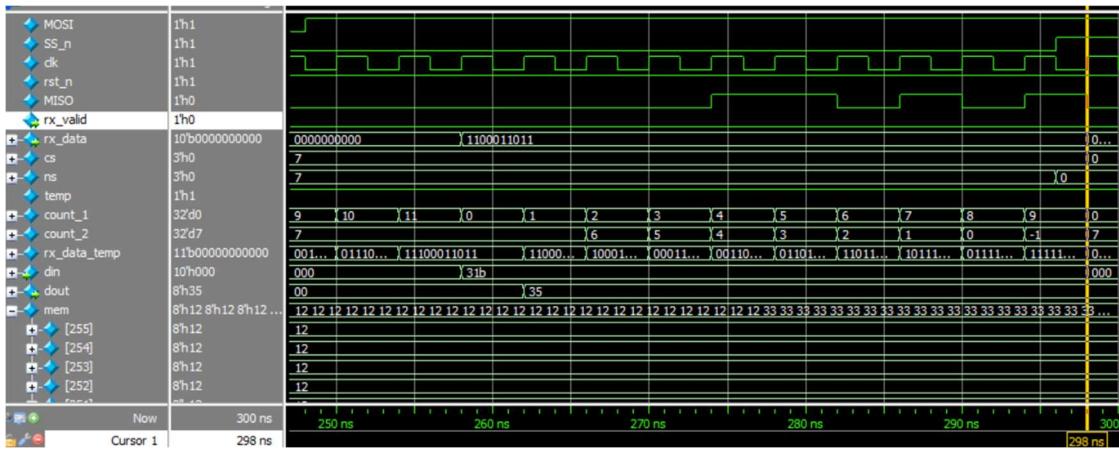
After 11 clock cycles (1 for control signal (read) and another 10 for data) since 2 most sig. bits are 11 memory will assert tx_valid and data from memory are sent on tx_data(dout):



Value in memory (35) will appear in MISO during 8 clock cycles:

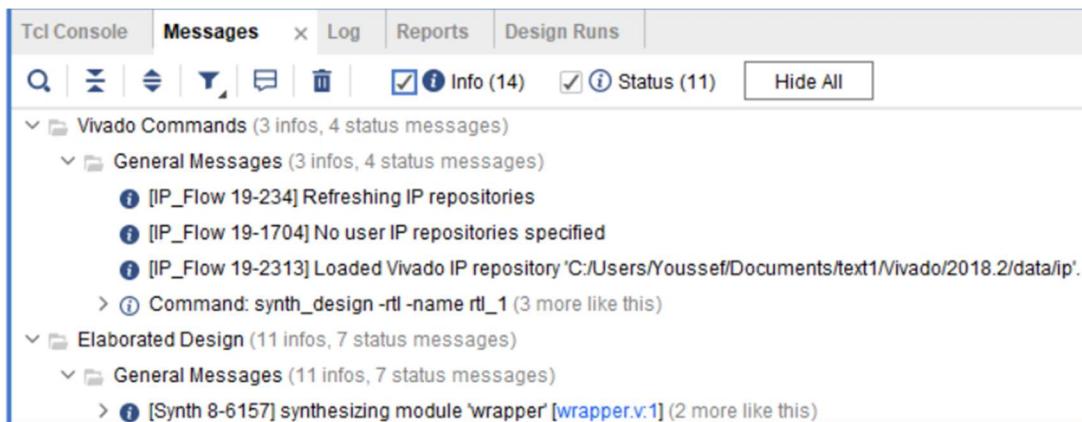
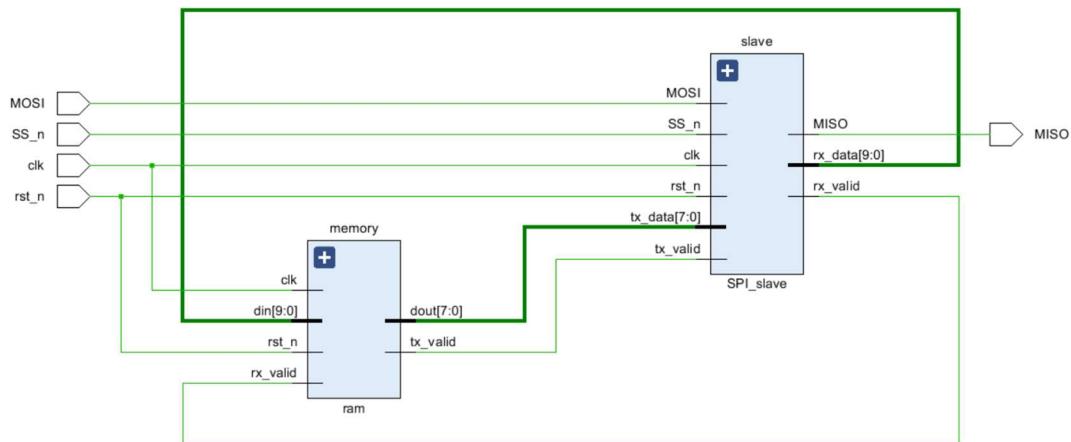


SS_n=1 so, cs=IDLE and communication ends:

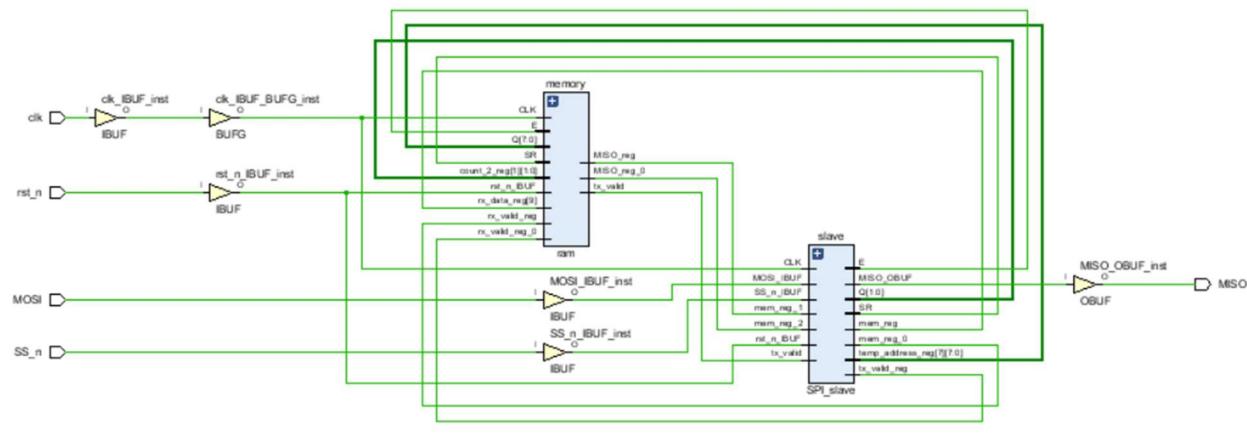


Vivado snippets:

Elaboration(gray):



Synthesis (gray):



State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	011
READ_DATA	010	111
READ_ADD	111	110

Design Timing Summary

Setup		Hold		Pulse Width			
Worst Negative Slack (WNS):	4.839 ns	Worst Hold Slack (WHS):	0.134 ns	Worst Pulse Width Slack (WPWS):	4.500 ns		
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns		
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0		
Total Number of Endpoints:	185	Total Number of Endpoints:	185	Total Number of Endpoints:	103		

All user specified timing constraints are met.

Name	Slack ^ 1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	4.839	6	7	11	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[0]/CE	4.779	2.099	2.680	10 ^
Path 2	4.839	6	7	11	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[10]/CE	4.779	2.099	2.680	10
Path 3	4.839	6	7	11	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[1]/CE	4.779	2.099	2.680	10
Path 4	4.839	6	7	11	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[2]/CE	4.779	2.099	2.680	10
Path 5	4.839	6	7	11	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[3]/CE	4.779	2.099	2.680	10
Path 6	4.839	6	7	11	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[4]/CE	4.779	2.099	2.680	10 ^

```
Synthesis (2 warnings, 37 infos, 11 status messages)
> ⓘ Command: synth_design -top wrapper -part xc7a35tcpg236-1L (10 more like this)
  ⓘ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35tI'
> ⓘ [Synth 8-6157] synthesizing module 'wrapper' [wrapper.v:1] (2 more like this)
  ⓘ [Synth 8-5534] Detected attribute (* fsm_encoding = "gray") [FSM.v:12]
> ⓘ [Synth 8-6155] done synthesizing module 'SPI_slave' (1#1) [FSM.v:1] (2 more like this)
  ⓘ [Device 21-403] Loading part xc7a35tcpg236-1L
  ⓘ [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/Youssef/Documents/digital course/project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xilf/wrapper_propimpl.xdc].
    Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  ⓘ [Synth 8-802] Inferred FSM for state register 'cs_reg' in module 'SPI_slave'
> ⓘ [Synth 8-5545] ROM "MISO" won't be mapped to RAM because address size (32) is larger than maximum supported(25) (5 more like this)
> ⓘ [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (4 more like this)
  ⓘ [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_slave'
  ⓘ [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [FSM.v:20]
> ⓘ [Synth 8-4480] The timing for the instance L_0/memory/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
  ⓘ [Project 1-571] Translating synthesized netlist
  ⓘ [Netlist 29-17] Analyzing 27 Unisim elements for replacement
  ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
> ⓘ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
> ⓘ [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed. (1 more like this)
  ⓘ [Common 17-83] Releasing license. Synthesis
  ⓘ [Constraints 18-5210] No constraint will be written out.
```

Implementation(gray):

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 4.412 ns	Worst Hold Slack (WHS): 0.070 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 185	Total Number of Endpoints: 185	Total Number of Endpoints: 103

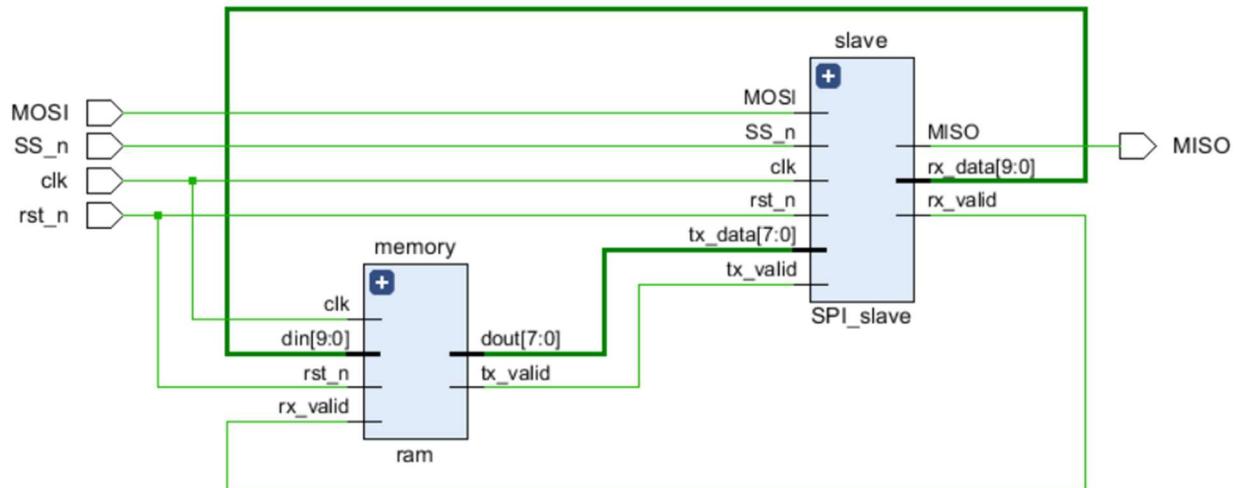
All user specified timing constraints are met.

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
wrapper		150	103	56	150	76	0.5	5	1
memory (ram)		3	9	5	3	0	0.5	0	0
slave (SPI_slave)		147	94	55	147	75	0	0	0

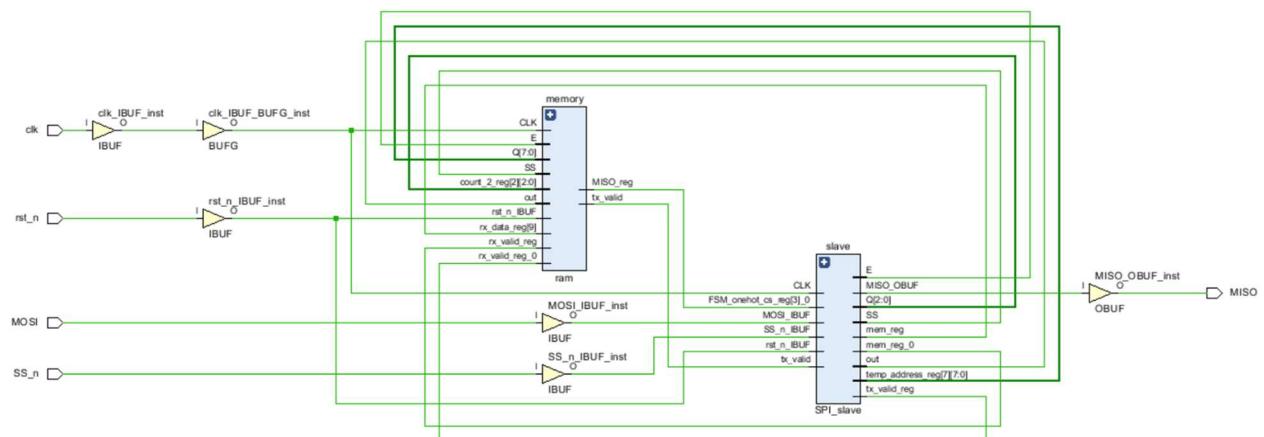
Implementation (98 infos, 228 status messages)

- Design Initialization (11 infos, 7 status messages)
 - Command: open_checkpoint {C:/Users/Youssef/Documents/digital course/project_4/project_4.runs/impl_1(wrapper.dcp)}
 - [Netlist 29-17] Analyzing 24 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35ticpg236-1L
 - [Project 1-570] Preparing netlist for logic optimization

Elaboration (one_hot):



Synthesis (one_hot):



State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	011
READ_DATA	01000	111
READ_ADD	10000	110

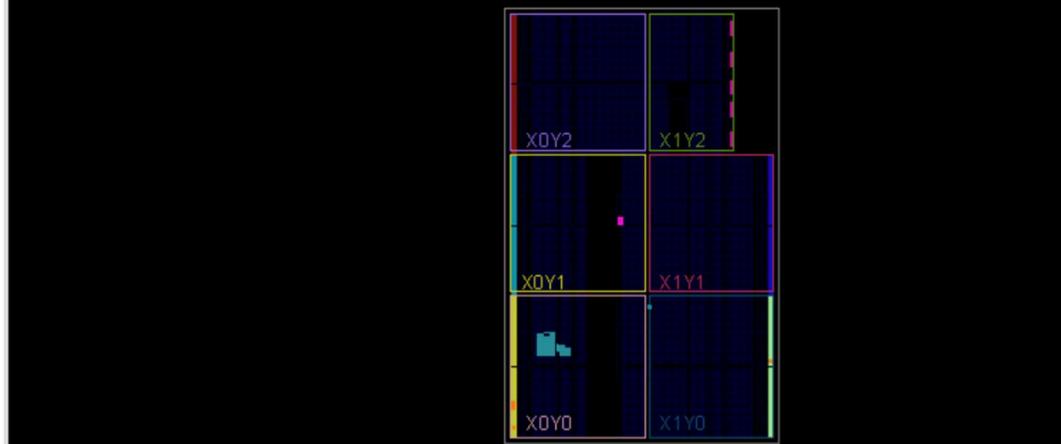
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.191 ns	Worst Hold Slack (WHS):	0.147 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	185	Total Number of Endpoints:	185	Total Number of Endpoints:	105

All user specified timing constraints are met.

Name	Slack ^ 1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source
Path 1	5.191	6	37	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[0]/CE	4.427	2.099	2.328	10.000	sys_c ^
Path 2	5.191	6	37	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[10]/CE	4.427	2.099	2.328	10.000	sys_c

Implementation(one_hot):



The screenshot shows the FPGA implementation of the design. A 4x4 grid of logic blocks is displayed, each labeled with a unique identifier: X0Y0, X0Y1, X0Y2, X1Y0, X1Y1, X1Y2. The blocks are colored in various shades of blue, green, and yellow, indicating different logic functions or resources. The interface includes toolbars for navigation and analysis, and a properties panel on the left.

Ports		Design Runs	Power	DRC	Methodology	Timing
						Design Timing Summary
						Worst Negative Slack (WNS): 4.244 ns
						Total Negative Slack (TNS): 0.000 ns
						Number of Failing Endpoints: 0
						Total Number of Endpoints: 185
						Worst Hold Slack (WHS): 0.067 ns
						Total Hold Slack (THS): 0.000 ns
						Number of Failing Endpoints: 0
						Total Number of Endpoints: 185
						Worst Pulse Width Slack (WPWS): 4.500 ns
						Total Pulse Width Negative Slack (TPWS): 0.000 ns
						Number of Failing Endpoints: 0
						Total Number of Endpoints: 105

All user specified timing constraints are met.

Tcl Console | **Messages** | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | ? | Hide All

Warning (2) Info (243) Status (489)

> ⓘ [Synth 8-6155] done synthesizing module 'SPI_slave' (1#1) [FSM.v:1] (2 more like this)
 ⓘ [Device 21-403] Loading part xc7a35tcpg236-1L
 ⓘ [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/Youssef/Documents/digital course/project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [xilrwrapper_proplmpl.xdc].
 Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
 ⓘ [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave'
 > ⓘ [Synth 8-5545] ROM "MISO" won't be mapped to RAM because address size (32) is larger than maximum supported(25) (5 more like this)
 > ⓘ [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (4 more like this)
 ⓘ [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module SPI_slave'
 ⓘ [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [FSM.v:20]
 > ⓘ [Synth 8-4480] The timing for the instance i_0/memory/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
 ⓘ [Project 1-571] Translating synthesized netlist
 ⓘ [Netlist 29-17] Analyzing 29 Unisim elements for replacement
 ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 > ⓘ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
 ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 > ⓘ [Project 1-111] Unisim Transformation Summary:
 No Unisim elements were transformed. (1 more like this)
 ⓘ [Common 17-83] Releasing license: Synthesis
 ⓘ [Constraints 18-5210] No constraint will be written out.
 ⓘ [Common 17-1381] The checkpoint 'C:/Users/Youssef/Documents/digital course/project/project_4/project_4.runs/synth_1/wrapper.dcp' has been generated.
 ⓘ [runrtl-4] Executing : report_utilization -file wrapper_utilization_synth.rpt -pb wrapper_utilization_synth.pb
 ⓘ [Common 17-206] Exiting Vivado at Mon Aug 5 20:11:55 2024...

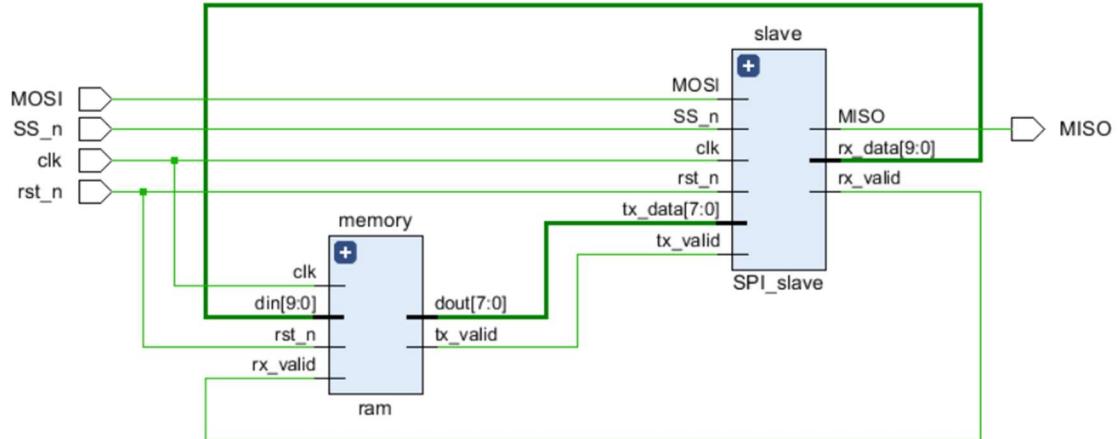
Implementation (96 infos, 231 status messages)

Design Initialization (7 infos, 7 status messages)

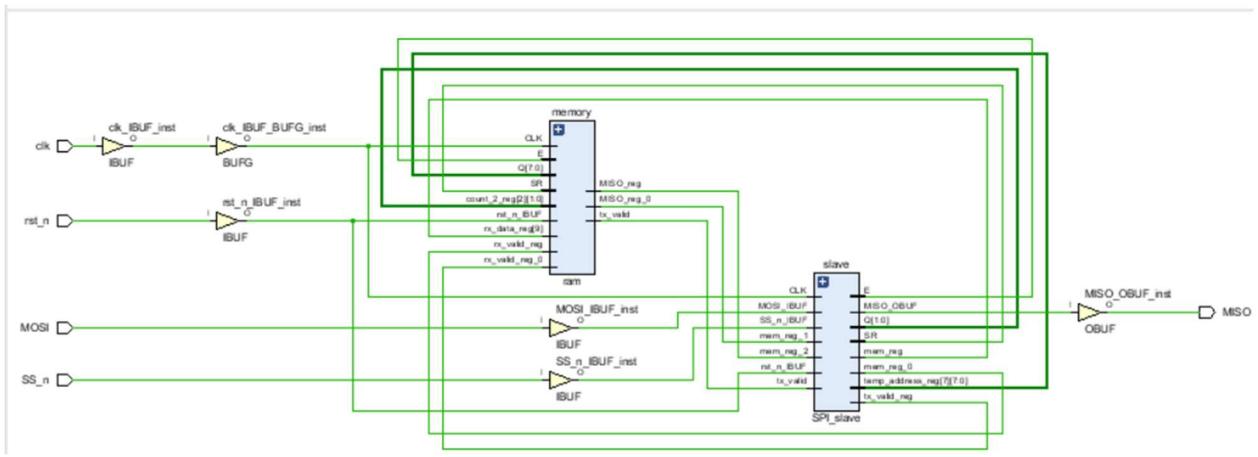
> ⓘ Command: link_design -top wrapper -part xc7a35tcpg236-1L (6 more like this)
 ⓘ [Netlist 29-17] Analyzing 24 Unisim elements for replacement

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
wrapper	151	107	55	151		79	0.5	5	1
memory (ram)	4	9	5	4		0	0.5	0	0
slave (SPI_slave)	147	98	53	147		77	0	0	0

Elaboration(sequential):



Synthesis(sequential):



State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	011
READ_DATA	011	111
READ_ADD	100	110

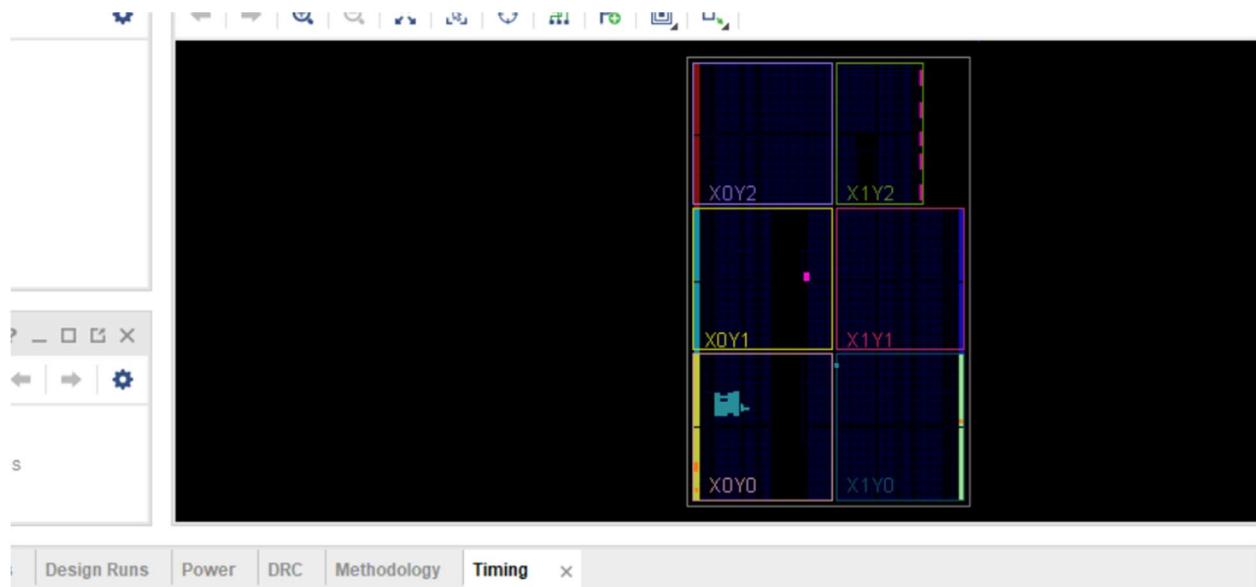
Design Timing Summary

Setup		Hold		Pulse Width			
Worst Negative Slack (WNS):	4.788 ns	Worst Hold Slack (WHS):	0.147 ns	Worst Pulse Width Slack (WPWS):	4.500 ns		
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns		
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0		
Total Number of Endpoints:	185	Total Number of Endpoints:	185	Total Number of Endpoints:	103		

All user specified timing constraints are met.

Name	Slack ^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source
Path 1	4.788	6	35	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[0]/CE	4.830	2.099	2.731	10.000	sys_c ^
Path 2	4.788	6	35	slave/count_1_reg[5]/C	slave/rx_data_temp_reg[10]/CE	4.830	2.099	2.731	10.000	sys_c

Implementation(sequential):



Setup		Hold		Pulse Width			
Worst Negative Slack (WNS):	5.034 ns	Worst Hold Slack (WHS):	0.134 ns	Worst Pulse Width Slack (WPWS):	4.500 ns		
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns		
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0		
Total Number of Endpoints:	185	Total Number of Endpoints:	185	Total Number of Endpoints:	103		

All user specified timing constraints are met.

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N wrapper		150	103	52	150	77	0.5	5	1
memory (ram)		3	9	3	3	0	0.5	0	0
slave (SPI_slave)		147	94	51	147	76	0	0	0

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization ? - ×

Q Warning (2) Info (247) Status (496) Hide All

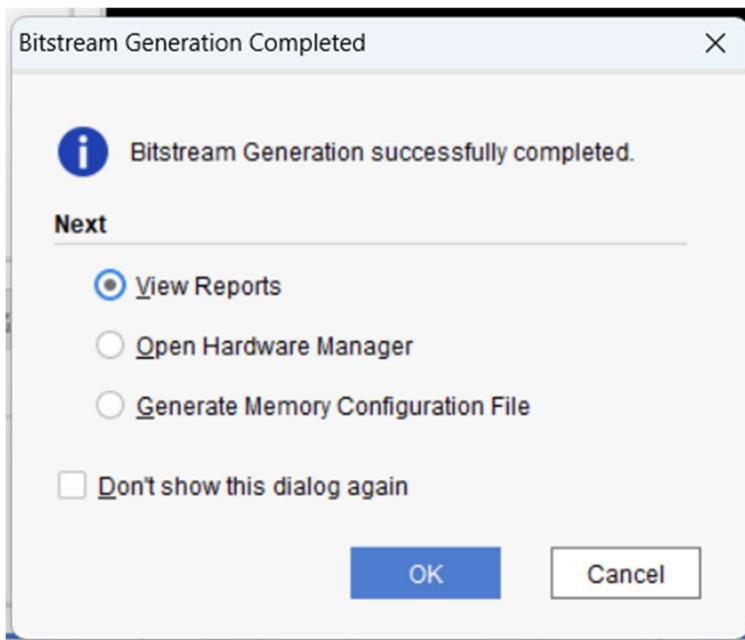
```

  ① [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential") [FSM.v:12]
  > ① [Synth 8-6155] done synthesizing module 'SPI_slave' (#1) [FSM.v:1] (2 more like this)
  ① [Device 21-403] Loading part xc7a35tcpg236-1L
  ① [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/Youssef/Documents/digital course/project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil/wrapper_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  ① [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave'
  > ① [Synth 8-5545] ROM "MISO" won't be mapped to RAM because address size (32) is larger than maximum supported(25) (5 more like this)
  > ① [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (4 more like this)
  ① [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_slave'
  ① [Synth 8-327] inferring latch for variable 'FSM_sequential_ns_reg' [FSM.v:20]
  > ① [Synth 8-4480] The timing for the instance I_0/memory/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
  ① [Project 1-571] Translating synthesized netlist
  ① [Netlist 29-17] Analyzing 27 Unisim elements for replacement
  ① [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  > ① [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  ① [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  > ① [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed. (1 more like this)
  ① [Common 17-83] Releasing license: Synthesis
  ① [Constraints 18-5210] No constraint will be written out
  ① [Common 17-1381] The checkpoint 'C:/Users/Youssef/Documents/digital course/project/project_4/project_4.runs/synth_1(wrapper.dcp)' has been generated.
  ① [runrtl-4] Executing : report_utilization -file wrapper_utilization_synth.rpt -pb wrapper_utilization_synth.pb
  ① [Common 17-206] Exiting Vivado at Mon Aug 5 20:27:49 2024...

```

Sequential is the best choice as it has the highest slack after implementation and according to the requirements we work at the highest frequency.

Bitstream generated successfully:

A screenshot of a software interface showing build logs. The top bar includes search, filter, and status indicators (Warning 4, Info 291, Status 538). The main area shows two sections: "Synthesis (2 warnings)" and "Implementation (1 warning)".

- Synthesis (2 warnings):**
 - [Synth 8-327] Inferring latch for variable 'FSM_sequential_ns_reg' [FSM.v:20]
 - [Constraints 18-5210] No constraint will be written out.
- Implementation (1 warning):**
 - Write Bitstream (1 warning)**
 - DRC (1 warning)**
 - Physical Configuration (1 warning)**
 - Chip Level (1 warning)**
 - [DRC PDRC-153] Gated clock check: Net slave/FSM_sequential_ns_reg[2]_i_2_n_0 is a gated clock net sourced by a combinational pin slave/FSM_sequential_ns_reg[2]_i_2/O, cell slave/FSM_sequential_ns_reg[2]_i_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

Debug core created:

```
160
161 create_debug_core u_ila_0 ila
162 set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
163 set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
164 set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
165 set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
166 set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
167 set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
168 set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
169 set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
170 set_property port_width 1 [get_debug_ports u_ila_0/clk]
171 connect_debug_port u_ila_0/clk [get_nets [list clk_IBUF_BUFG]]
172 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
173 set_property port_width 1 [get_debug_ports u_ila_0/probe0]
174 connect_debug_port u_ila_0/probe0 [get_nets [list clk_IBUF]]
175 create_debug_port u_ila_0 probe
176 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
177 set_property port_width 1 [get_debug_ports u_ila_0/probe1]
178 connect_debug_port u_ila_0/probe1 [get_nets [list MISO_OBUF]]
179 create_debug_port u_ila_0 probe
180 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
181 set_property port_width 1 [get_debug_ports u_ila_0/probe2]
182 connect_debug_port u_ila_0/probe2 [get_nets [list MOSI_IBUF]]
183 create_debug_port u_ila_0 probe
184 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
185 set_property port_width 1 [get_debug_ports u_ila_0/probe3]
186 connect_debug_port u_ila_0/probe3 [get_nets [list rst_n_IBUF]]
187 create_debug_port u_ila_0 probe
188 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
189 set_property port_width 1 [get_debug_ports u_ila_0/probe4]
190 connect_debug_port u_ila_0/probe4 [get_nets [list SS_n_IBUF]]
191 set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
192 set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
193 set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
194 connect_debug_port dbg_hub/clk [get_nets clk_IBUF_BUFG]
195
```