Mini project

The code:

C: > Users > lenovo > Desktop > assignments digital > project 1 > flipflop_mux.v

```
1   module combine (in,clk,CE,RST,out);
2   parameter sel =0;
3   parameter size=18;
4   parameter rsttype="sync";
5   input [size-1:0] in;
6   input clk,RST,CE;
7   output [size-1:0] out;
8   reg [size-1:0] outflip,outflip1;
9   wire [size-1:0] outfinal;
10  always @ (posedge clk) begin
11      if(CE) begin
12      if (RST)
13      outflip<=0;
14      else
15  outflip<=in;
16      end
17     // else
18       //outflip<=0;
19  end
20  always @ (posedge clk,posedge RST) begin
21      if (RST)
22      outflip1<=0;
23      else
24      if (CE)
25  outflip1<=in;
26  //else outflip1<=0;
27  end
28  assign outfinal =(rsttype=="sync")? (outflip): (outflip1);
29  assign out= (sel==0)?in:outfinal;
30  endmodule
31
```

C: > Users > lenovo > Desktop > assignments digital > project 1 > mux_2to1.v

```
1   module mux2 (a,b,out1);
2   parameter size=18;
3   parameter sel1="DIRECT";
4   input [size-1:0] a,b;
5
6   output reg [size-1:0] out1;
7   always @ (*) begin
8       if (sel1=="DIRECT")
9       out1=a;
10      else if (sel1=="CASCADE")
11      out1=b;
12      else out1=0;
13
14  end
15
16  endmodule
17
```

C: > Users > lenovo > Desktop > assignments digital > project 1 > mux_4to1.v

```
1   module mux4 (a,b,c,d,sel2,out2);
2   parameter size=48;
3
4   input [size-1:0] a,b,c,d;
5   input [1:0] sel2;
6   output reg [size-1:0] out2;
7   always @ (*) begin
8       case(sel2)
9       0:out2=a;
10      1:out2=b;
11      2:out2=c;
12      default:out2=d;
13      endcase
14  end
15
16  endmodule
```

C: > Users > lenovo > Desktop > assignments digital > project 1 > project1.v

```
module DSP (A,B,D,C,clk,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,
CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
parameter A0REG=0;
parameter A1REG=1;
parameter B0REG=0;
parameter B1REG=1;
parameter CREG=1;
parameter DREG=1;
parameter MREG=1;
parameter PREG=1;
parameter CARRYINREG=1;
parameter CARRYOUTREG=1;
parameter OPMODEREG=1;
parameter CARRYINSEL="OPMODE5";
parameter B_INPUT="DIRECT";
parameter rsttype="sync";
input [17:0] A,B,D,BCIN;
input [47:0] C,PCIN;
input [7:0] OPMODE;
input clk,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
output [17:0] BCOUT;
output [47:0] PCOUT,P;
output [35:0] M;
output CARRYOUT,CARRYOUTF;
wire [17:0] d_out,b0_out,a0_out,pre_out,b1_out,a1_out;
wire [17:0] b_before,pre_op;
wire [47:0] c_out;
wire [47:0] X_;
wire [35:0] mult_out;
wire [35:0] m_out;
wire [47:0] M_OUT;
wire [47:0] x_out,z_out;
wire cyi_out;
reg cascade_out;
reg [1:0] flag;
wire [47:0]post_out,post_out1,post_out2;
wire [7:0] OPMODE_OUT;
wire cout,cout1,cout2;

```

```
41  combine #(1,8,"sync") OPMODE_REG (OPMODE,clk,CEOPMODE,RSTOPMODE,OPMODE_OUT);
42  combine #(1,18,"sync") d_reg (D,clk,CED,RSTD,d_out);
43  mux2 #(18,"DIRECT") multiplexer (B,BCIN,b_before);
44  combine #(0,18,"sync") b0_reg (b_before,clk,CEB,RSTB,b0_out);
45  combine #(0,18,"sync") a0_reg (A,clk,CEA,RSTA,a0_out);
46  combine #(1,48,"sync") c_reg (C,clk,CEC,RSTC,c_out);
47  assign pre_op=(OPMODE_OUT[6]==0)?(d_out+b0_out):(d_out-b0_out);
48  assign pre_out=(OPMODE_OUT[4]==0)?b0_out:pre_op;
49  combine #(1,18,"sync") b1_reg  (pre_out,clk,CEB,RSTB,b1_out);
50  combine #(1,18,"sync") a1_reg(a0_out,clk,CEA,RSTA,a1_out);
51  assign BCOUT=b1_out;
52  assign X_={d_out[11:0],a1_out[17:0],b1_out[17:0]};
53  assign mult_out=a1_out*b1_out;
54
55
56  combine #(1,36,"sync") m_reg (mult_out,clk,CEM,RSTM,m_out);
57  assign M=m_out;
58  assign M_OUT=(m_out)&(48'h000fffffffff);
59  always @ (*) begin
60      if (CARRYINSEL=="OPMODE5") begin
61      flag=1;
62      cascade_out=OPMODE[5];
63      end
64      else if (CARRYINSEL=="CARRYIN") begin
65          flag=2;
66      cascade_out= CARRYIN;
67      end
68      else begin
69      cascade_out=0;
70      flag=3;
71      end
72  end
73  combine #(1,1,"sync") CYI(cascade_out,clk,CECARRYIN,RSTCARRYIN,cyi_out);
74  mux4 #(48) x_mult (48'b0,M_OUT,P,X_,OPMODE_OUT [1:0],x_out);
75  mux4 #(48) z_mult (48'b0,PCIN,P,c_out,OPMODE_OUT [3:2],z_out);
76  assign {cout1,post_out1}=x_out+z_out+cyi_out;
77  assign {cout2,post_out2}=z_out-(x_out+cyi_out);
78  assign cout =(OPMODE_OUT [7]==0)?cout1:cout2;
79  assign post_out =(OPMODE_OUT [7]==0)?post_out1:post_out2;
```

```
84
85    combine #(1,1,"sync") C_cas(cout,clk,CECARRYIN,RSTCARRYIN,CARRYOUT);
86    assign CARRYOUTF=CARRYOUT;
87    combine  #(1,48,"sync") P_REG (post_out,clk,CEP,RSTP,P);
88    assign PCOUT=P;
89
90
91
92
93
94    endmodule
```

The testbench

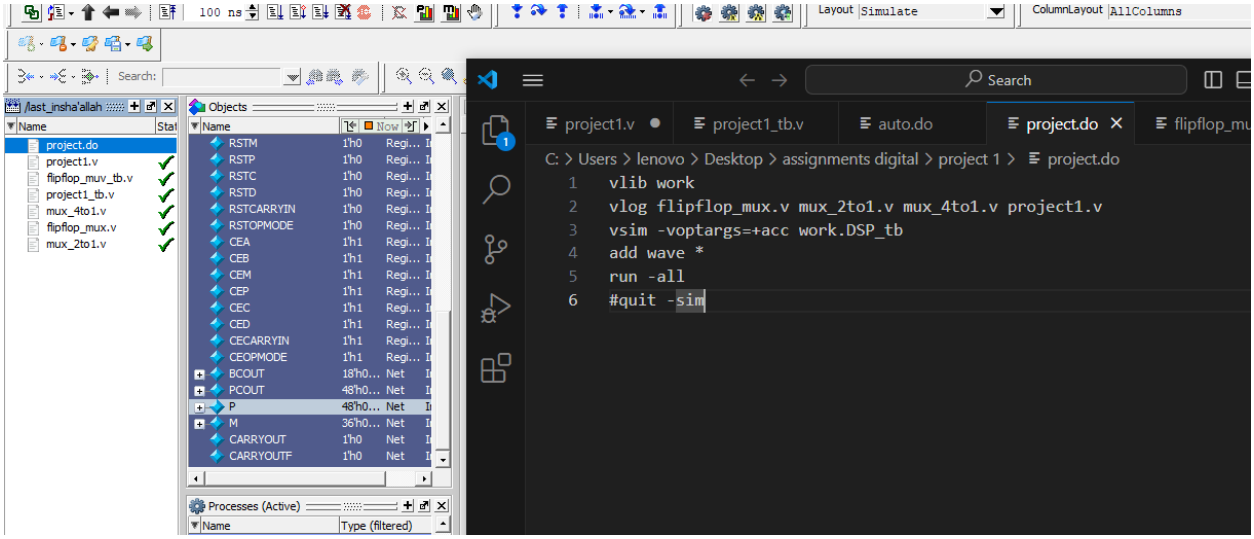
C: > Users > lenovo > Desktop > assignments digital > project 1 > project1_tb.v

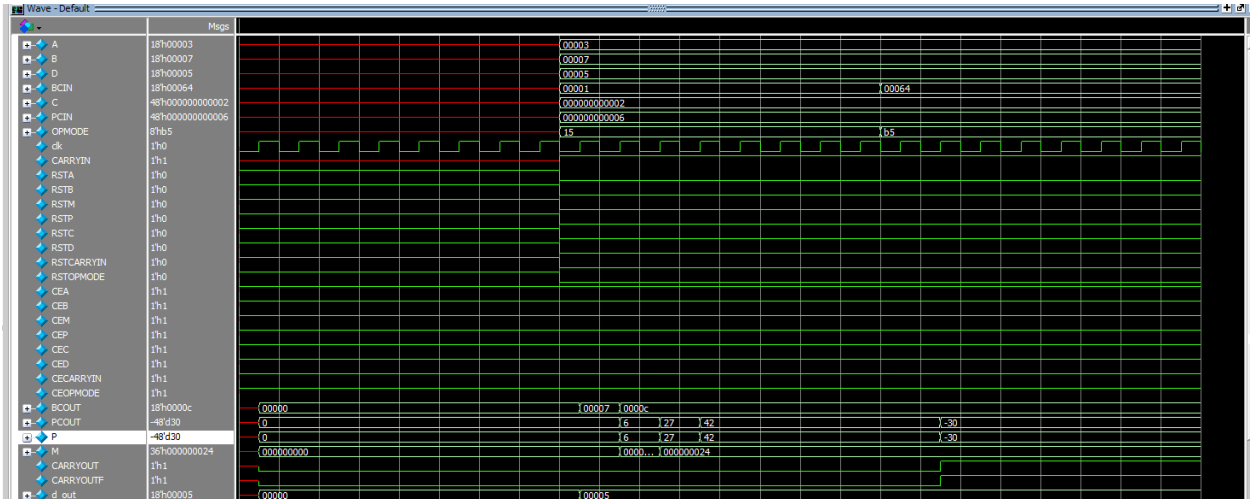
```
1   module DSP_tb ();
2   parameter A0REG=0;
3   parameter A1REG=1;
4   parameter B0REG=0;
5   parameter B1REG=1;
6   parameter CREG=1;
7   parameter DREG=1;
8   parameter MREG=1;
9   parameter PREG=1;
10  parameter CARRYINREG=1;
11  parameter CARRYOUTREG=1;
12  parameter OPMODEREG=1;
13  parameter CARRYINSEL="OPMODE5";
14  parameter B_INPUT="DIRECT";
15  parameter rsttype="sync";
16  reg [17:0] A,B,D,BCIN;
17  reg [47:0] C,PCIN;
18  reg [7:0] OPMODE;
19  reg clk,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
20  wire [17:0] BCOUT;
21  wire [47:0] PCOUT,P;
22  wire [35:0] M;
23  wire CARRYOUT,CARRYOUTF;
24  DSP #(A0REG,A1REG,B0REG,B1REG,CREG,DREG,MREG,PREG,CARRYINREG,CARRYOUTREG,OPMODEREG,CARRYINSEL,B_INPUT,rsttype) dut (A,B,D,C,clk,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,
25  CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
26  initial begin
27      clk=0;
28      forever begin
29          #1 clk=~clk;
30      end
31  end
```

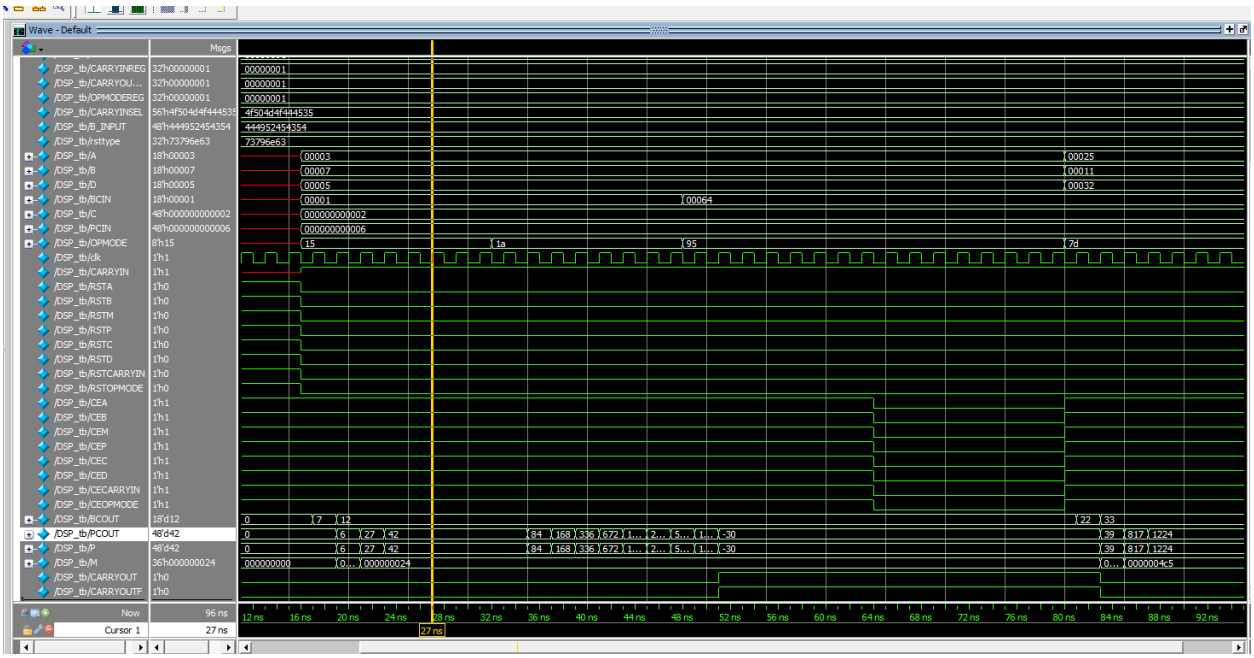
C: > Users > lenovo > Desktop > assignments digital > project 1 > project1_tb.v

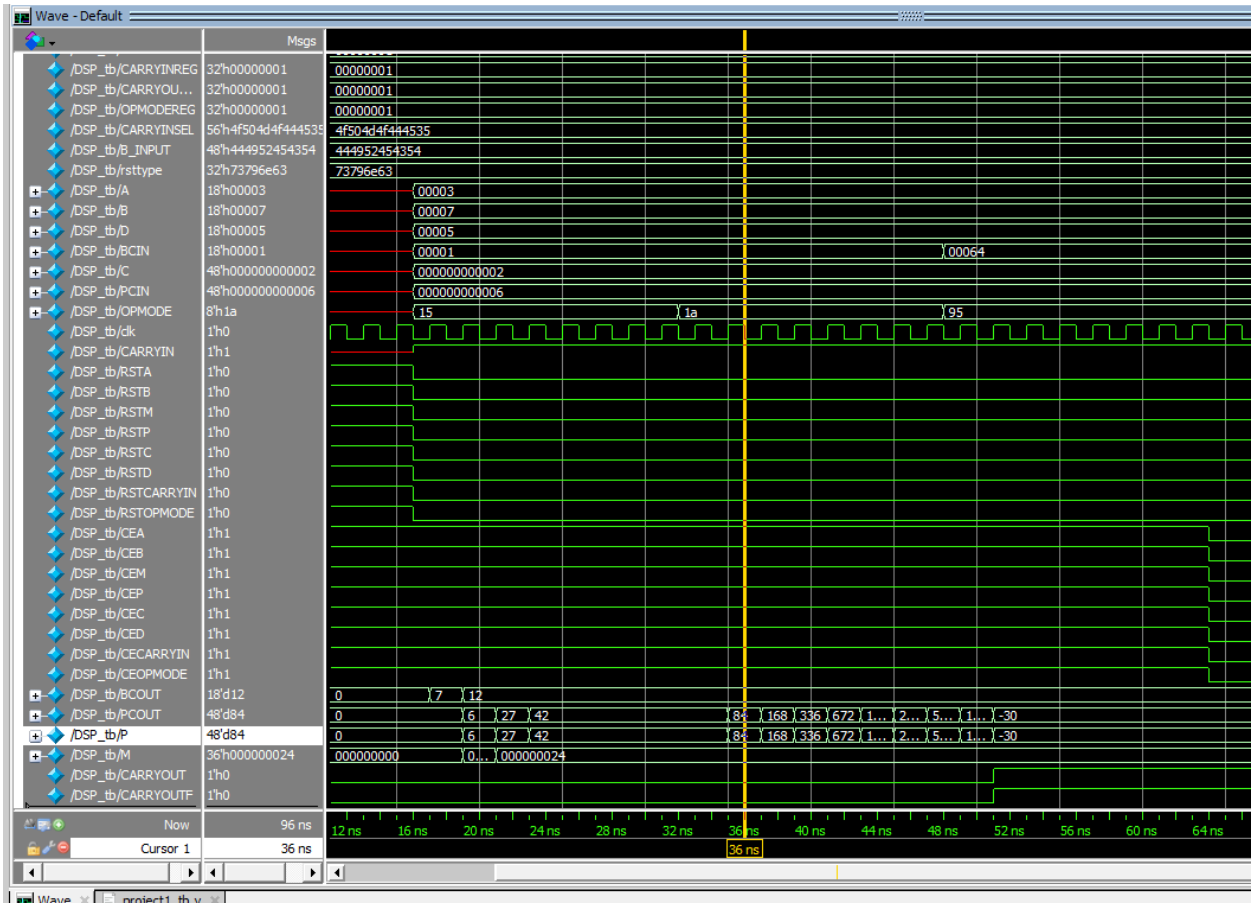
```
initial begin
    RSTA=1;RSTB=1;RSTM=1;RSTP=1;RSTC=1;RSTD=1;RSTCARRYIN=1;RSTOPMODE=1;
    CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;
    repeat (8)begin
        @(negedge clk);
    end
        RSTA=0;RSTB=0;RSTM=0;RSTP=0;RSTC=0;RSTD=0;RSTCARRYIN=0;RSTOPMODE=0;
        D=5;B=7;A=3;C=2;
        OPMODE=8'b00010101;PCIN=6;BCIN=1;CARRYIN=1;
         repeat (8)begin
        @(negedge clk);
    end
    // the expected p=42 ,bcout=12,carryout=0,
    OPMODE=8'b00011010;
     repeat (8)begin
        @(negedge clk);
     end
     // the expected p=84 ,bcout=12,carryout=0,

        D=5;B=7;A=3;C=2;
        OPMODE=8'b10010101;PCIN=6;BCIN=100;CARRYIN=1;
         repeat (8)begin
        @(negedge clk);
    end
// the expected p=-30
CEA=0;CEB=0;CEM=0;CEP=0;CEC=0;CED=0;CECARRYIN=0;CEOPMODE=0;
         repeat (8)begin
        @(negedge clk);
    end

   CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;
D=50; B=17; A=37;C=2;
    OPMODE=8'b01111101;PCIN=6;BCIN=100;CARRYIN=1;
         repeat (8)begin
        @(negedge clk);
    end
    // the expected p=1224
$stop;
end
endmodule
```

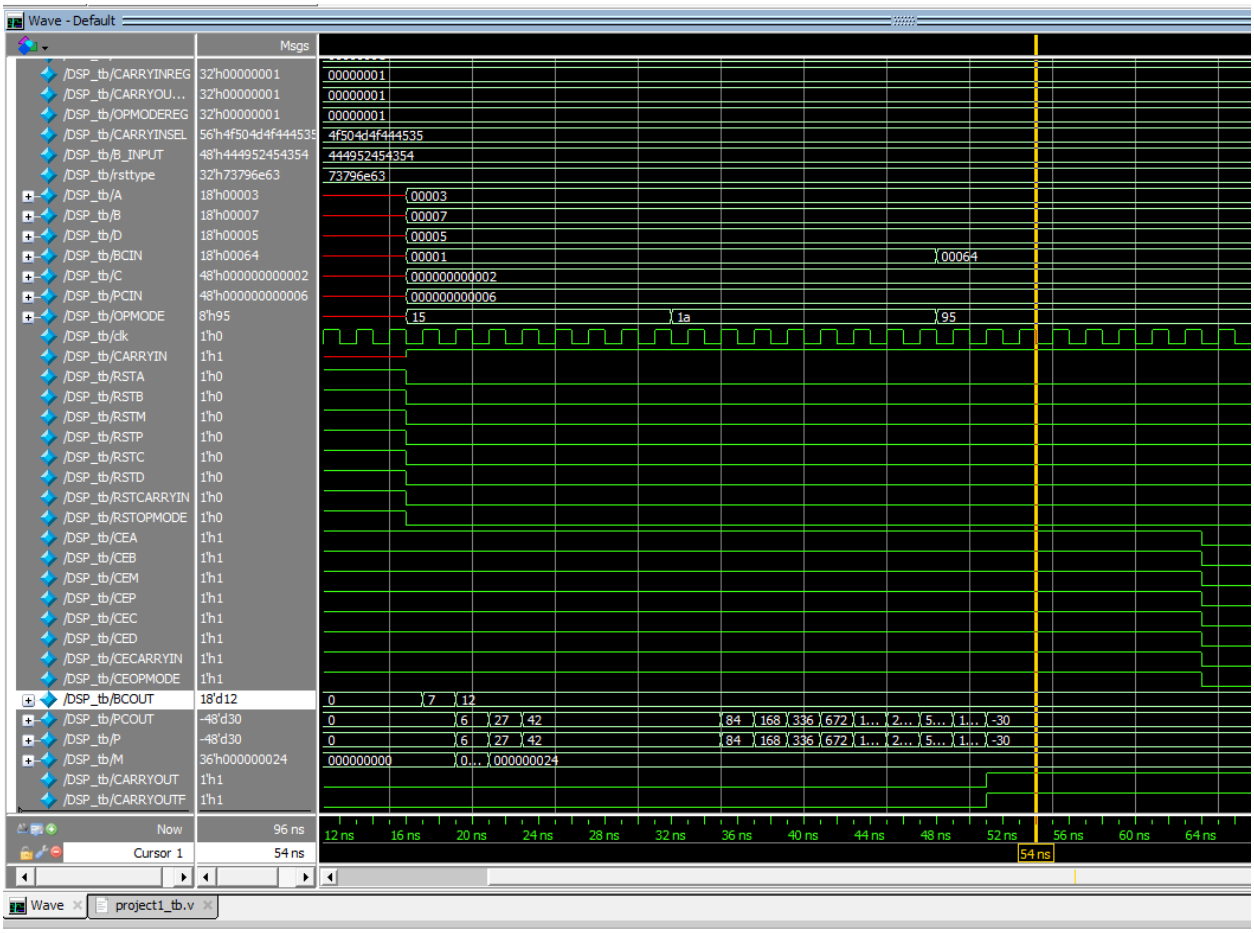
The do file

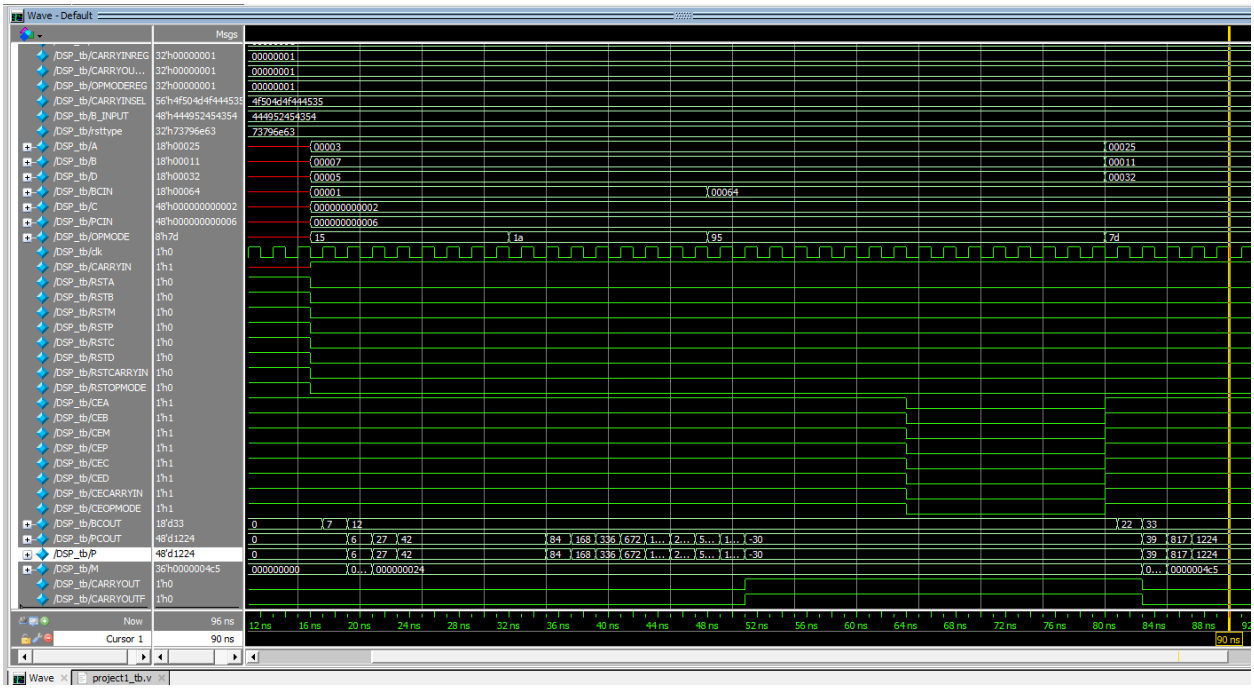

project1.v
project1_tb.v
auto.do
project.do
flipflop_mu
C: > Users > lenovo > Desktop > assignments digital > project 1 > project.do
1 vlib work
2 vlog flipflop_mux.v mux_2to1.v mux_4to1.v project1.v
3 vsim -voptargs=+acc work.DSP_tb
4 add wave *
5 run -all
6 #quit -sim




Wave - Default
Msgs
/DSP_tb/CARRYINREG 32'h00000001
/DSP_tb/CARRYOU... 32'h00000001
/DSP_tb/OPMODEREG 32'h00000001
/DSP_tb/CARRYINSEL 56'h4f504d4f444535
/DSP_tb/B_INPUT 48'h444952454354
/DSP_tb/rsttype 32'h73796e63
/DSP_tb/A 18'h00003
/DSP_tb/B 18'h00007
/DSP_tb/D 18'h00005
/DSP_tb/BCIN 18'h00001
/DSP_tb/C 48'h000000000002
/DSP_tb/PCIN 48'h000000000006
/DSP_tb/OPMODE 8'h15
/DSP_tb/clk 1'h1
/DSP_tb/CARRYIN 1'h1
/DSP_tb/RSTA 1'h0
/DSP_tb/RSTB 1'h0
/DSP_tb/RSTM 1'h0
/DSP_tb/RSTP 1'h0
/DSP_tb/RSTC 1'h0
/DSP_tb/RSTD 1'h0
/DSP_tb/RSTCARRYIN 1'h0
/DSP_tb/RSTOPMODE 1'h0
/DSP_tb/CEA 1'h1
/DSP_tb/CEB 1'h1
/DSP_tb/CEM 1'h1
/DSP_tb/CEP 1'h1
/DSP_tb/CEC 1'h1
/DSP_tb/CED 1'h1
/DSP_tb/CECARRYIN 1'h1
/DSP_tb/CEOPMODE 1'h1
/DSP_tb/BCOUT 18'd12
/DSP_tb/PCOUT 48'd42
/DSP_tb/P 48'd42
/DSP_tb/M 36'h000000024
/DSP_tb/CARRYOUT 1'h0
/DSP_tb/CARRYOUTF 1'h0
00000001
4f504d4f444535
444952454354
73796e63
00003
00007
00005
00001
000000000002
000000000006
15
00025
00011
00032
00064
1a
95
7d
0
7
12
22
33
6
27
42
84
168
336
672
1...
2...
5...
1...
-30
39
817
1224
000000000
0...
000000024
0...
0000004c5
Now
96 ns
Cursor 1
27 ns
12 ns
16 ns
20 ns
24 ns
28 ns
32 ns
36 ns
40 ns
44 ns
48 ns
52 ns
56 ns
60 ns
64 ns
68 ns
72 ns
76 ns
80 ns
84 ns
88 ns
92 ns


Wave - Default
Msgs
/DSP_tb/CARRYINREG 32'h00000001
/DSP_tb/CARRYOU... 32'h00000001
/DSP_tb/OPMODEREG 32'h00000001
/DSP_tb/CARRYINSEL 56'h4f504d4f444535
/DSP_tb/B_INPUT 48'h444952454354
/DSP_tb/rsttype 32'h73796e63
/DSP_tb/A 18'h00003
/DSP_tb/B 18'h00007
/DSP_tb/D 18'h00005
/DSP_tb/BCIN 18'h00001
/DSP_tb/C 48'h000000000002
/DSP_tb/PCIN 48'h000000000006
/DSP_tb/OPMODE 8'h1a
/DSP_tb/clk 1'h0
/DSP_tb/CARRYIN 1'h1
/DSP_tb/RSTA 1'h0
/DSP_tb/RSTB 1'h0
/DSP_tb/RSTM 1'h0
/DSP_tb/RSTP 1'h0
/DSP_tb/RSTC 1'h0
/DSP_tb/RSTD 1'h0
/DSP_tb/RSTCARRYIN 1'h0
/DSP_tb/RSTOPMODE 1'h0
/DSP_tb/CEA 1'h1
/DSP_tb/CEB 1'h1
/DSP_tb/CEM 1'h1
/DSP_tb/CEP 1'h1
/DSP_tb/CEC 1'h1
/DSP_tb/CED 1'h1
/DSP_tb/CECARRYIN 1'h1
/DSP_tb/CEOPMODE 1'h1
/DSP_tb/BCOUT 18'd12
/DSP_tb/PCOUT 48'd84
/DSP_tb/P 48'd84
/DSP_tb/M 36'h000000024
/DSP_tb/CARRYOUT 1'h0
/DSP_tb/CARRYOUTF 1'h0
00000001
00000001
00000001
4f504d4f444535
444952454354
73796e63
00003
00007
00005
00001
00064
000000000002
000000000006
15
1a
95
Now
96 ns
Cursor 1
36 ns
12 ns
16 ns
20 ns
24 ns
28 ns
32 ns
36 ns
40 ns
44 ns
48 ns
52 ns
56 ns
60 ns
64 ns
Wave
project1_tb.v


Wave - Default
Msgs
/DSP_tb/CARRYINREG 32'h00000001
/DSP_tb/CARRYOU... 32'h00000001
/DSP_tb/OPMODEREG 32'h00000001
/DSP_tb/CARRYINSEL 56'h4f504d4f444535
/DSP_tb/B_INPUT 48'h444952454354
/DSP_tb/rsttype 32'h73796e63
/DSP_tb/A 18'h00003
/DSP_tb/B 18'h00007
/DSP_tb/D 18'h00005
/DSP_tb/BCIN 18'h00064
/DSP_tb/C 48'h000000000002
/DSP_tb/PCIN 48'h000000000006
/DSP_tb/OPMODE 8'h95
/DSP_tb/clk 1'h0
/DSP_tb/CARRYIN 1'h1
/DSP_tb/RSTA 1'h0
/DSP_tb/RSTB 1'h0
/DSP_tb/RSTM 1'h0
/DSP_tb/RSTP 1'h0
/DSP_tb/RSTC 1'h0
/DSP_tb/RSTD 1'h0
/DSP_tb/RSTCARRYIN 1'h0
/DSP_tb/RSTOPMODE 1'h0
/DSP_tb/CEA 1'h1
/DSP_tb/CEB 1'h1
/DSP_tb/CEM 1'h1
/DSP_tb/CEP 1'h1
/DSP_tb/CEC 1'h1
/DSP_tb/CED 1'h1
/DSP_tb/CECARRYIN 1'h1
/DSP_tb/CEOPMODE 1'h1
/DSP_tb/BCOUT 18'd12
/DSP_tb/PCOUT -48'd30
/DSP_tb/P -48'd30
/DSP_tb/M 36'h000000024
/DSP_tb/CARRYOUT 1'h1
/DSP_tb/CARRYOUTF 1'h1
Now 96 ns
Cursor 1 54 ns
12 ns 16 ns 20 ns 24 ns 28 ns 32 ns 36 ns 40 ns 44 ns 48 ns 52 ns 56 ns 60 ns 64 ns
54 ns
Wave
project1_tb.v


Wave - Default
Msgs
/DSP_tb/CARRYINREG 32'h00000001
/DSP_tb/CARRYOU... 32'h00000001
/DSP_tb/OPMODEREG 32'h00000001
/DSP_tb/CARRYINSEL 56'h4f504d4f444535
/DSP_tb/B_INPUT 48'h444952454354
/DSP_tb/rsttype 32'h73796e63
/DSP_tb/A 18'h00025
/DSP_tb/B 18'h00011
/DSP_tb/D 18'h00032
/DSP_tb/BCIN 18'h00064
/DSP_tb/C 48'h000000000002
/DSP_tb/PCIN 48'h000000000006
/DSP_tb/OPMODE 8'h7d
/DSP_tb/clk 1'h0
/DSP_tb/CARRYIN 1'h1
/DSP_tb/RSTA 1'h0
/DSP_tb/RSTB 1'h0
/DSP_tb/RSTM 1'h0
/DSP_tb/RSTP 1'h0
/DSP_tb/RSTC 1'h0
/DSP_tb/RSTD 1'h0
/DSP_tb/RSTCARRYIN 1'h0
/DSP_tb/RSTOPMODE 1'h0
/DSP_tb/CEA 1'h1
/DSP_tb/CEB 1'h1
/DSP_tb/CEM 1'h1
/DSP_tb/CEP 1'h1
/DSP_tb/CEC 1'h1
/DSP_tb/CED 1'h1
/DSP_tb/CECARRYIN 1'h1
/DSP_tb/CEOPMODE 1'h1
/DSP_tb/BCOUT 18'd33
/DSP_tb/PCOUT 48'd1224
/DSP_tb/P 48'd1224
/DSP_tb/M 36'h0000004c5
/DSP_tb/CARRYOUT 1'h0
/DSP_tb/CARRYOUTF 1'h0
Now 96 ns
Cursor 1 90 ns
12 ns 16 ns 20 ns 24 ns 28 ns 32 ns 36 ns 40 ns 44 ns 48 ns 52 ns 56 ns 60 ns 64 ns 68 ns 72 ns 76 ns 80 ns 84 ns 88 ns
90 ns
Wave
project1_tb.v

C: > Users > lenovo > Desktop > assignments digital > assignmnet 5 > q3 > project_constrain.xdc

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

##Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock  -period 10.00 -name sys_clk_pin  -waveform {0 5} -add [get_ports clk]


## Switches
#set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports {sw[0]}]
#set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports {sw[1]}]
#set_property -dict { PACKAGE_PIN W16   IOSTANDARD LVCMOS33 } [get_ports {sw[2]}]
#set_property -dict { PACKAGE_PIN W17   IOSTANDARD LVCMOS33 } [get_ports {sw[3]}]
#set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 } [get_ports {sw[4]}]
#set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports {sw[5]}]
#set_property -dict { PACKAGE_PIN W14   IOSTANDARD LVCMOS33 } [get_ports {sw[6]}]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports {sw[7]}]
#set_property -dict { PACKAGE_PIN V2    IOSTANDARD LVCMOS33 } [get_ports {sw[8]}]
#set_property -dict { PACKAGE_PIN T3    IOSTANDARD LVCMOS33 } [get_ports {sw[9]}]
#set_property -dict { PACKAGE_PIN T2    IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
#set_property -dict { PACKAGE_PIN R3    IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
#set_property -dict { PACKAGE_PIN W2    IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
#set_property -dict { PACKAGE_PIN U1    IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
#set_property -dict { PACKAGE_PIN T1    IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
#set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]


## LEDs
#set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports {led[0]}]
#set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports {led[1]}]
#set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports {led[2]}]
#set_property -dict { PACKAGE_PIN V19   IOSTANDARD LVCMOS33 } [get_ports {led[3]}]
#set_property -dict { PACKAGE_PIN W18   IOSTANDARD LVCMOS33 } [get_ports {led[4]}]
#set_property -dict { PACKAGE_PIN U15   IOSTANDARD LVCMOS33 } [get_ports {led[5]}]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports {led[6]}]
#set_property -dict { PACKAGE_PIN V14   IOSTANDARD LVCMOS33 } [get_ports {led[7]}]
#set_property -dict { PACKAGE_PIN V13   IOSTANDARD LVCMOS33 } [get_ports {led[8]}]
```

C: > Users > lenovo > Desktop > assignments digital > assignmnet 5 > q3 > project_constrain.xdc

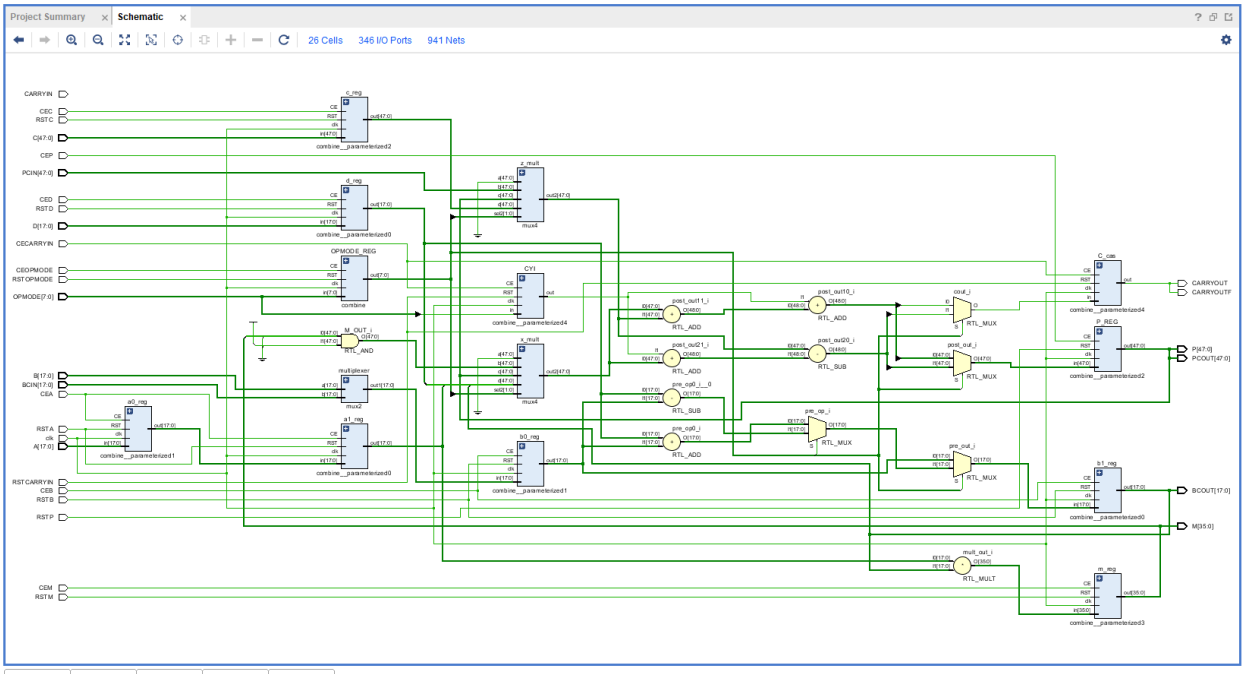
```
#set_property -dict { PACKAGE_PIN V13    IOSTANDARD LVCMOS33 } [get_ports {led[8]}]
#set_property -dict { PACKAGE_PIN V3     IOSTANDARD LVCMOS33 } [get_ports {led[9]}]
#set_property -dict { PACKAGE_PIN W3     IOSTANDARD LVCMOS33 } [get_ports {led[10]}]
#set_property -dict { PACKAGE_PIN U3     IOSTANDARD LVCMOS33 } [get_ports {led[11]}]
#set_property -dict { PACKAGE_PIN P3     IOSTANDARD LVCMOS33 } [get_ports {led[12]}]
#set_property -dict { PACKAGE_PIN N3     IOSTANDARD LVCMOS33 } [get_ports {led[13]}]
#set_property -dict { PACKAGE_PIN P1     IOSTANDARD LVCMOS33 } [get_ports {led[14]}]
#set_property -dict { PACKAGE_PIN L1     IOSTANDARD LVCMOS33 } [get_ports {led[15]}]


##7 Segment Display
#set_property -dict { PACKAGE_PIN W7   IOSTANDARD LVCMOS33 } [get_ports {seg[0]}]
#set_property -dict { PACKAGE_PIN W6   IOSTANDARD LVCMOS33 } [get_ports {seg[1]}]
#set_property -dict { PACKAGE_PIN U8   IOSTANDARD LVCMOS33 } [get_ports {seg[2]}]
#set_property -dict { PACKAGE_PIN V8   IOSTANDARD LVCMOS33 } [get_ports {seg[3]}]
#set_property -dict { PACKAGE_PIN U5   IOSTANDARD LVCMOS33 } [get_ports {seg[4]}]
#set_property -dict { PACKAGE_PIN V5   IOSTANDARD LVCMOS33 } [get_ports {seg[5]}]
#set_property -dict { PACKAGE_PIN U7   IOSTANDARD LVCMOS33 } [get_ports {seg[6]}]

#set_property -dict { PACKAGE_PIN V7   IOSTANDARD LVCMOS33 } [get_ports dp]

#set_property -dict { PACKAGE_PIN U2   IOSTANDARD LVCMOS33 } [get_ports {an[0]}]
#set_property -dict { PACKAGE_PIN U4   IOSTANDARD LVCMOS33 } [get_ports {an[1]}]
#set_property -dict { PACKAGE_PIN V4   IOSTANDARD LVCMOS33 } [get_ports {an[2]}]
#set_property -dict { PACKAGE_PIN W4   IOSTANDARD LVCMOS33 } [get_ports {an[3]}]


##Buttons
#set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports ]
#set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports btnU]
#set_property -dict { PACKAGE_PIN W19   IOSTANDARD LVCMOS33 } [get_ports btnL]
#set_property -dict { PACKAGE_PIN T17   IOSTANDARD LVCMOS33 } [get_ports btnR]
#set_property -dict { PACKAGE_PIN U17   IOSTANDARD LVCMOS33 } [get_ports btnD]


##Pmod Header JA
#set_property -dict { PACKAGE_PIN J1   IOSTANDARD LVCMOS33 } [get_ports {JA[0]}];#Sch name = JA1
#set_property -dict { PACKAGE_PIN L2   IOSTANDARD LVCMOS33 } [get_ports {JA[1]}];#Sch name = JA2
#set_property -dict { PACKAGE_PIN J2   IOSTANDARD LVCMOS33 } [get_ports {JA[2]}];#Sch name = JA3
```

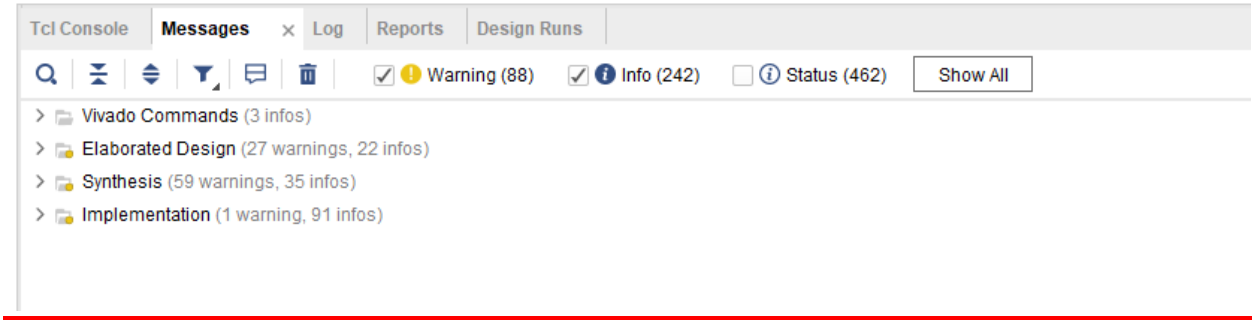
```
78   #set_property -dict { PACKAGE_PIN G2   IOSTANDARD LVCMOS33 } [get_ports {JA[3]}];#Sch name = JA4
79   #set_property -dict { PACKAGE_PIN H1   IOSTANDARD LVCMOS33 } [get_ports {JA[4]}];#Sch name = JA7
80   #set_property -dict { PACKAGE_PIN K2   IOSTANDARD LVCMOS33 } [get_ports {JA[5]}];#Sch name = JA8
81   #set_property -dict { PACKAGE_PIN H2   IOSTANDARD LVCMOS33 } [get_ports {JA[6]}];#Sch name = JA9
82   #set_property -dict { PACKAGE_PIN G3   IOSTANDARD LVCMOS33 } [get_ports {JA[7]}];#Sch name = JA10
83
84   ##Pmod Header JB
85   #set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33 } [get_ports {JB[0]}];#Sch name = JB1
86   #set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33 } [get_ports {JB[1]}];#Sch name = JB2
87   #set_property -dict { PACKAGE_PIN B15   IOSTANDARD LVCMOS33 } [get_ports {JB[2]}];#Sch name = JB3
88   #set_property -dict { PACKAGE_PIN B16   IOSTANDARD LVCMOS33 } [get_ports {JB[3]}];#Sch name = JB4
89   #set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33 } [get_ports {JB[4]}];#Sch name = JB7
90   #set_property -dict { PACKAGE_PIN A17   IOSTANDARD LVCMOS33 } [get_ports {JB[5]}];#Sch name = JB8
91   #set_property -dict { PACKAGE_PIN C15   IOSTANDARD LVCMOS33 } [get_ports {JB[6]}];#Sch name = JB9
92   #set_property -dict { PACKAGE_PIN C16   IOSTANDARD LVCMOS33 } [get_ports {JB[7]}];#Sch name = JB10
93
94   ##Pmod Header JC
95   #set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports {JC[0]}];#Sch name = JC1
96   #set_property -dict { PACKAGE_PIN M18   IOSTANDARD LVCMOS33 } [get_ports {JC[1]}];#Sch name = JC2
97   #set_property -dict { PACKAGE_PIN N17   IOSTANDARD LVCMOS33 } [get_ports {JC[2]}];#Sch name = JC3
98   #set_property -dict { PACKAGE_PIN P18   IOSTANDARD LVCMOS33 } [get_ports {JC[3]}];#Sch name = JC4
99   #set_property -dict { PACKAGE_PIN L17   IOSTANDARD LVCMOS33 } [get_ports {JC[4]}];#Sch name = JC7
100  #set_property -dict { PACKAGE_PIN M19   IOSTANDARD LVCMOS33 } [get_ports {JC[5]}];#Sch name = JC8
101  #set_property -dict { PACKAGE_PIN P17   IOSTANDARD LVCMOS33 } [get_ports {JC[6]}];#Sch name = JC9
102  #set_property -dict { PACKAGE_PIN R18   IOSTANDARD LVCMOS33 } [get_ports {JC[7]}];#Sch name = JC10
103
104  ##Pmod Header JXADC
105  #set_property -dict { PACKAGE_PIN J3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[0]}];#Sch name = XA1_P
106  #set_property -dict { PACKAGE_PIN L3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[1]}];#Sch name = XA2_P
107  #set_property -dict { PACKAGE_PIN M2   IOSTANDARD LVCMOS33 } [get_ports {JXADC[2]}];#Sch name = XA3_P
108  #set_property -dict { PACKAGE_PIN N2   IOSTANDARD LVCMOS33 } [get_ports {JXADC[3]}];#Sch name = XA4_P
109  #set_property -dict { PACKAGE_PIN K3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[4]}];#Sch name = XA1_N
110  #set_property -dict { PACKAGE_PIN M3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[5]}];#Sch name = XA2_N
111  #set_property -dict { PACKAGE_PIN M1   IOSTANDARD LVCMOS33 } [get_ports {JXADC[6]}];#Sch name = XA3_N
112  #set_property -dict { PACKAGE_PIN N1   IOSTANDARD LVCMOS33 } [get_ports {JXADC[7]}];#Sch name = XA4_N
113
```

```
##VGA Connector
#set_property -dict { PACKAGE_PIN G19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[0]}]
#set_property -dict { PACKAGE_PIN H19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[1]}]
#set_property -dict { PACKAGE_PIN J19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[2]}]
#set_property -dict { PACKAGE_PIN N19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[3]}]
#set_property -dict { PACKAGE_PIN N18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[0]}]
#set_property -dict { PACKAGE_PIN L18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[1]}]
#set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[2]}]
#set_property -dict { PACKAGE_PIN J18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[3]}]
#set_property -dict { PACKAGE_PIN J17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[0]}]
#set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[1]}]
#set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[2]}]
#set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[3]}]
#set_property -dict { PACKAGE_PIN P19   IOSTANDARD LVCMOS33 } [get_ports Hsync]
#set_property -dict { PACKAGE_PIN R19   IOSTANDARD LVCMOS33 } [get_ports Vsync]


##USB-RS232 Interface
#set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 } [get_ports RsRx]
#set_property -dict { PACKAGE_PIN A18   IOSTANDARD LVCMOS33 } [get_ports RsTx]


##USB HID (PS/2)
#set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33   PULLUP true } [get_ports PS2Clk]
#set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33   PULLUP true } [get_ports PS2Data]


##Quad SPI Flash
##Note that CCLK_0 cannot be placed in 7 series devices. You can access it using the
##STARTUPE2 primitive.
#set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[0]}]
#set_property -dict { PACKAGE_PIN D19   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[1]}]
#set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[2]}]
#set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[3]}]
#set_property -dict { PACKAGE_PIN K19   IOSTANDARD LVCMOS33 } [get_ports QspiCSn]
```

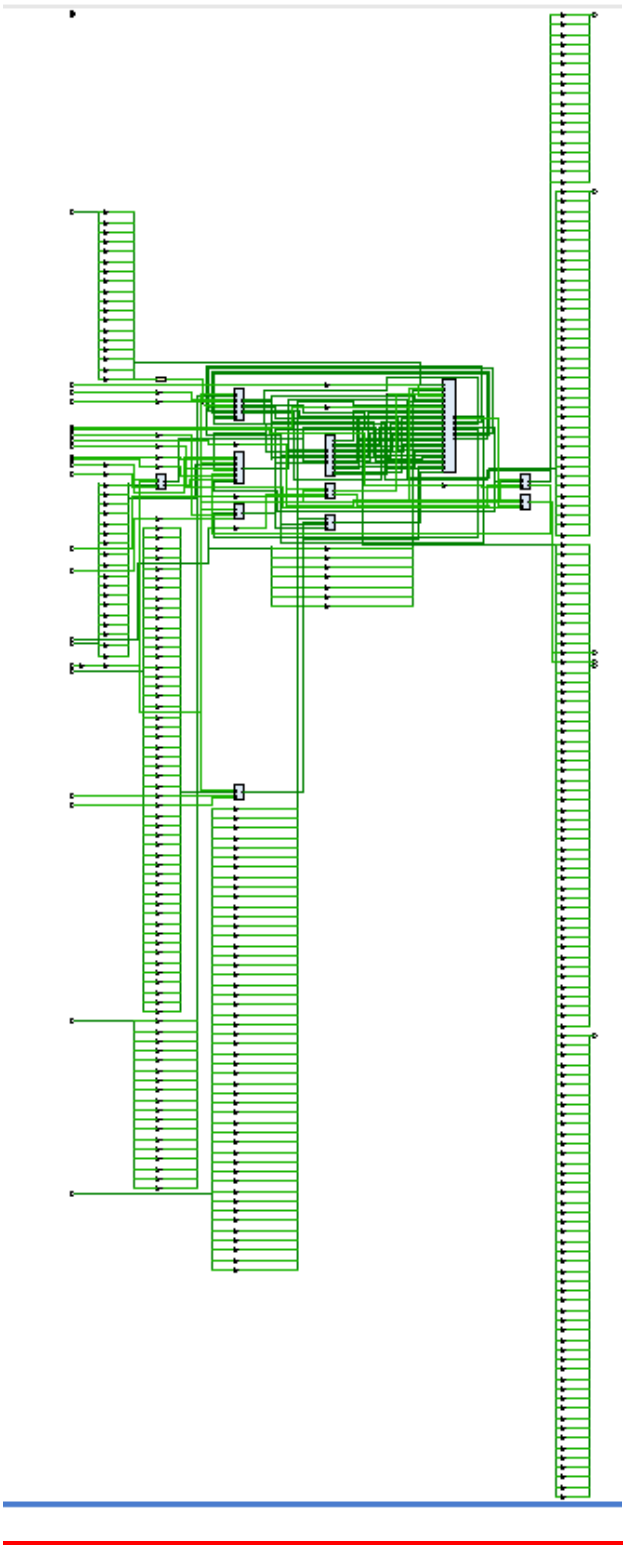
```
## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
```

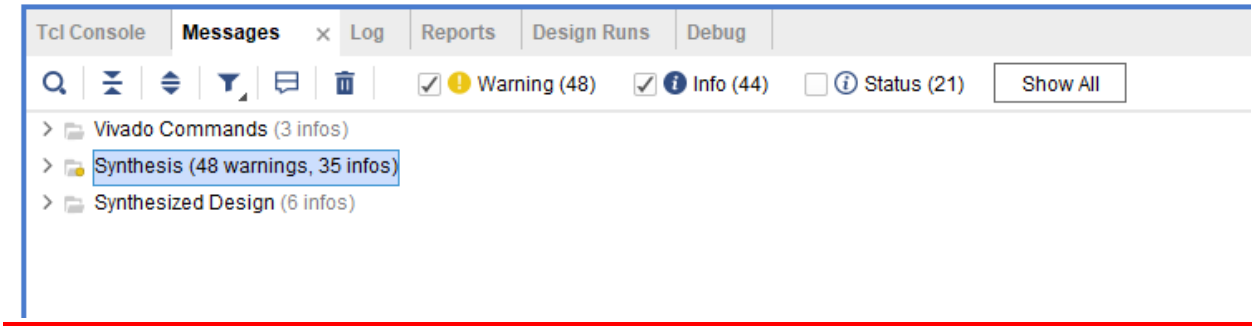
Elaboration

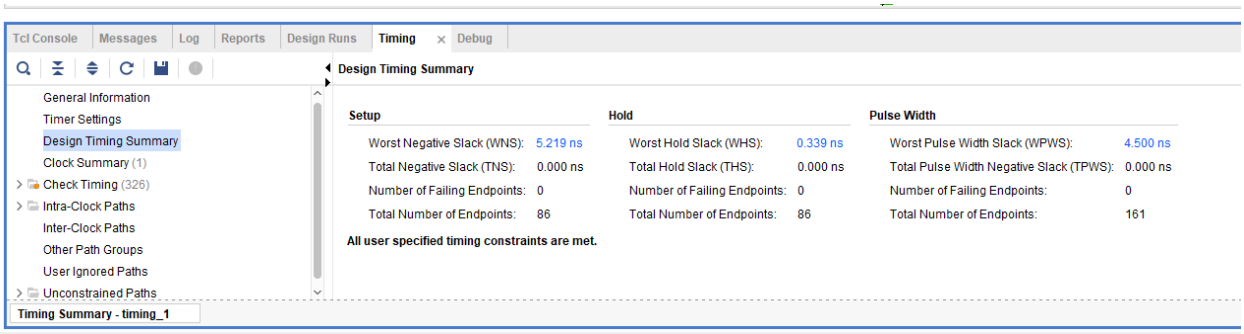


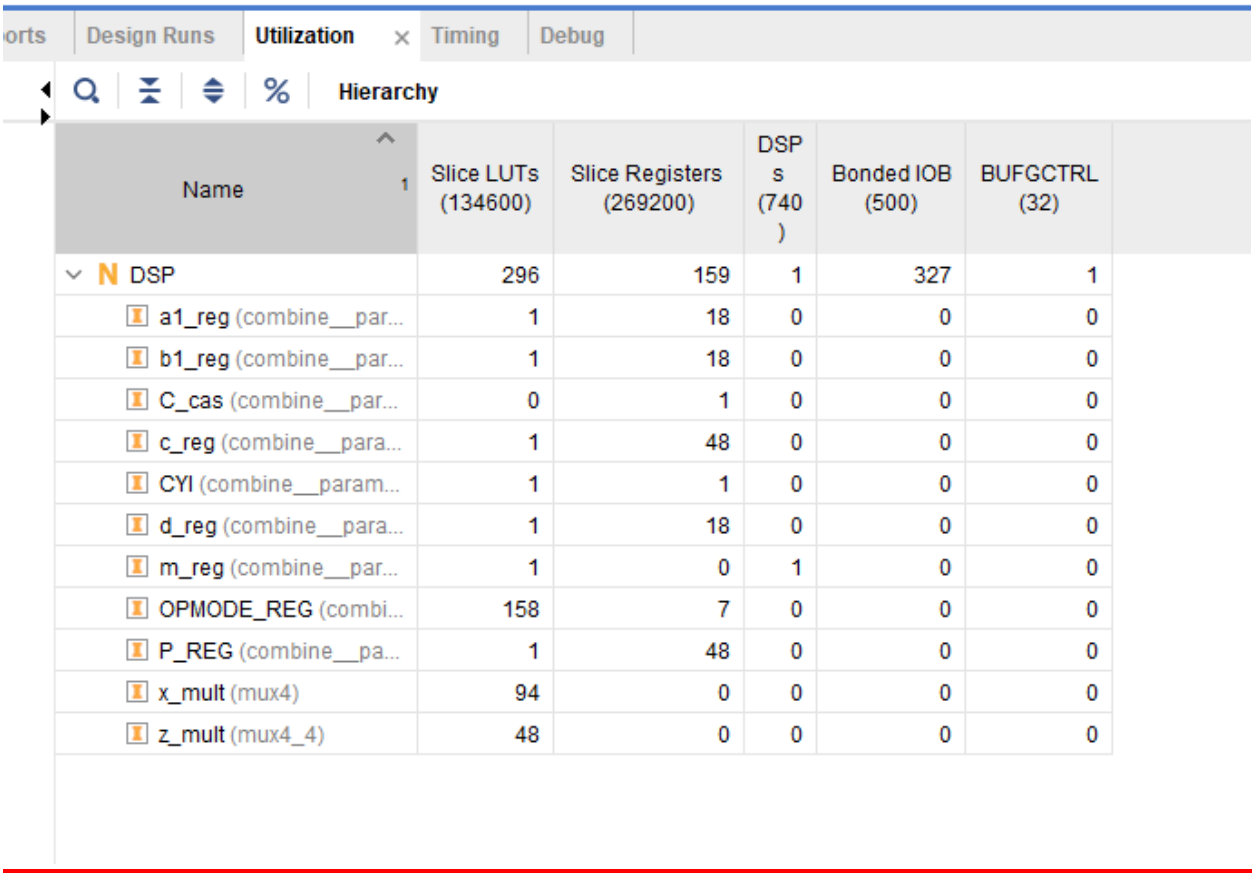


Synthesis

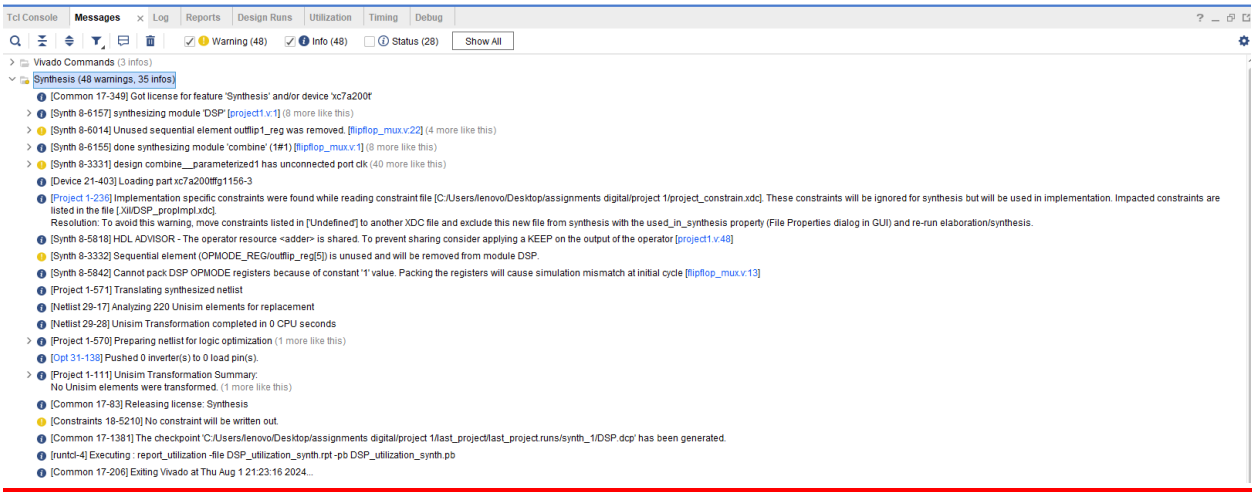




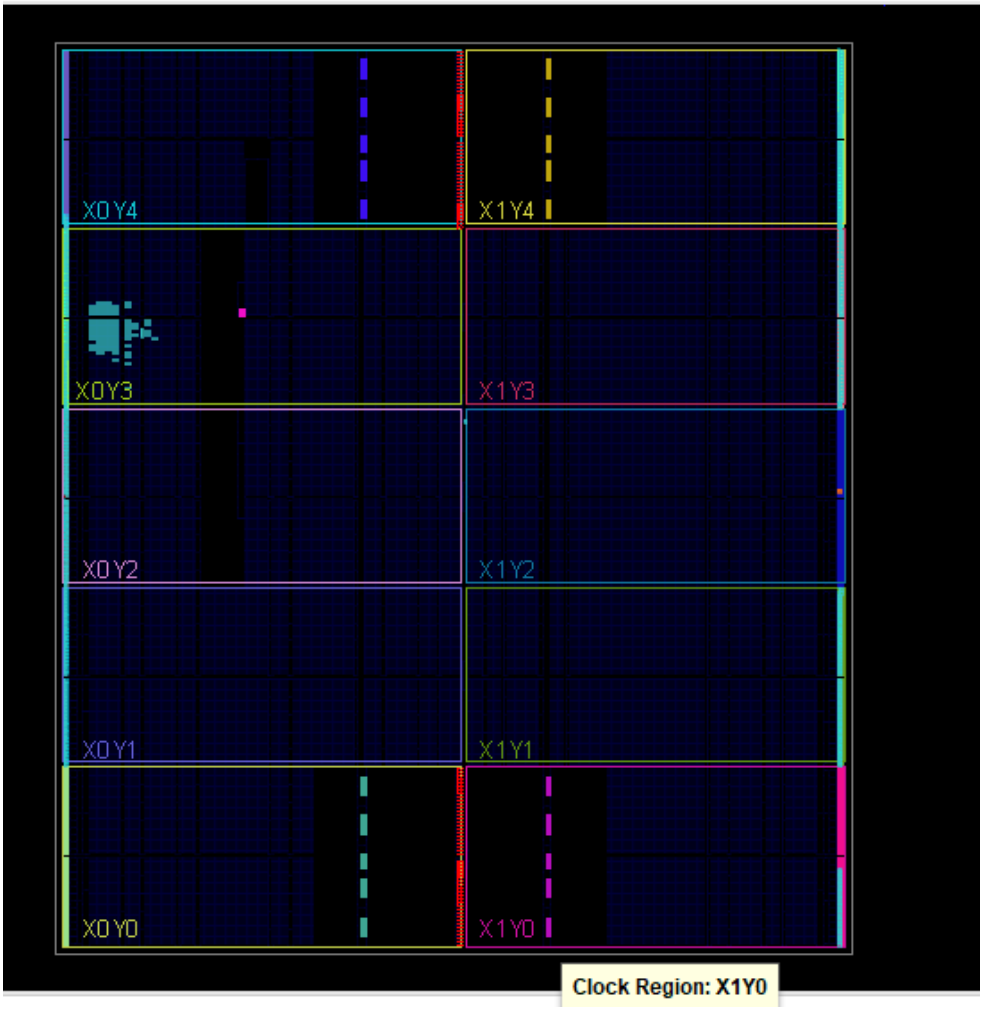


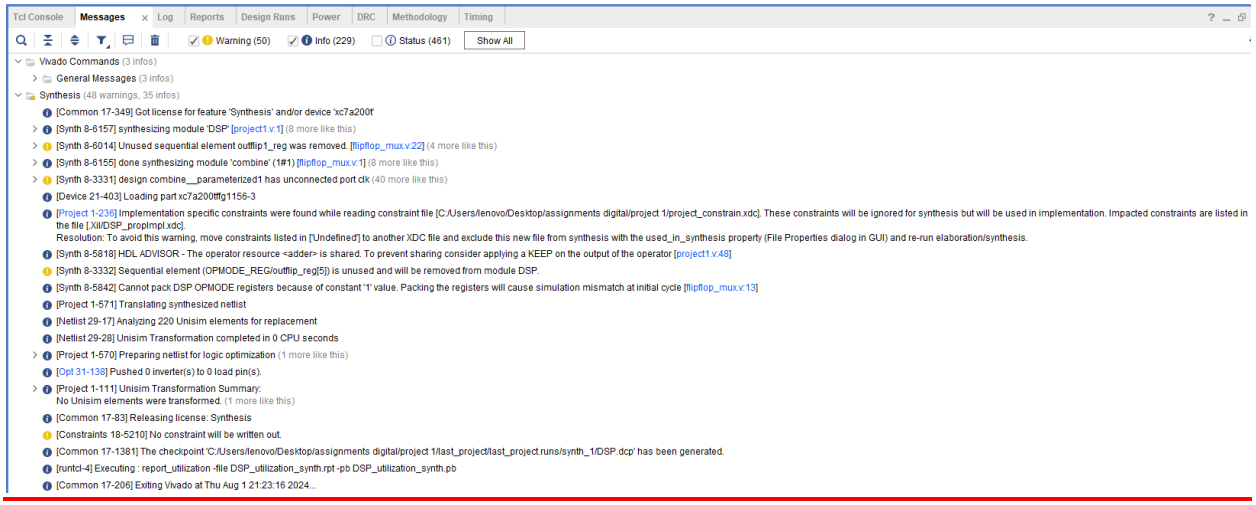


Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP	296	159	1	327	1
a1_reg (combine__par...	1	18	0	0	0
b1_reg (combine__par...	1	18	0	0	0
C_cas (combine__par...	0	1	0	0	0
c_reg (combine__para...	1	48	0	0	0
CYI (combine__param...	1	1	0	0	0
d_reg (combine__para...	1	18	0	0	0
m_reg (combine__par...	1	0	1	0	0
OPMODE_REG (combi...	158	7	0	0	0
P_REG (combine__pa...	1	48	0	0	0
x_mult (mux4)	94	0	0	0	0
z_mult (mux4_4)	48	0	0	0	0



Implementation




Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Warning (50)
Info (229)
Status (461)
Show All
Vivado Commands (3 infos)
General Messages (3 infos)
Synthesis (48 warnings, 35 infos)
[Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
[Synth 8-6157] synthesizing module 'DSP' [project1.v:1] (8 more like this)
[Synth 8-6014] Unused sequential element outflip1_reg was removed. [flipflop_mux.v:22] (4 more like this)
[Synth 8-6155] done synthesizing module 'combine' (1#1) [flipflop_mux.v:1] (8 more like this)
[Synth 8-3331] design combine__parameterized1 has unconnected port clk (40 more like this)
[Device 21-403] Loading part xc7a200tfg1156-3
[Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/lenovo/Desktop/assignments digital/project 1/project_constrain.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/DSP_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
[Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [project1.v:48]
[Synth 8-3332] Sequential element (OPMODE_REG/outflip_reg[5]) is unused and will be removed from module DSP.
[Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [flipflop_mux.v:13]
[Project 1-571] Translating synthesized netlist
[Netlist 29-17] Analyzing 220 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-570] Preparing netlist for logic optimization (1 more like this)
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
[Common 17-83] Releasing license: Synthesis
[Constraints 18-5210] No constraint will be written out.
[Common 17-1381] The checkpoint 'C:/Users/lenovo/Desktop/assignments digital/project 1/last_project/last_project.runs/synth_1/DSP.dcp' has been generated.
[runtcl-4] Executing : report_utilization -file DSP_utilization_synth.rpt -pb DSP_utilization_synth.pb
[Common 17-206] Exiting Vivado at Thu Aug 1 21:23:16 2024...