Sequential Logic Design

Design the following circuits using Verilog **and create a testbench** for each design to check its functionality.

1) Implement the following latch as specified below.

Parameters

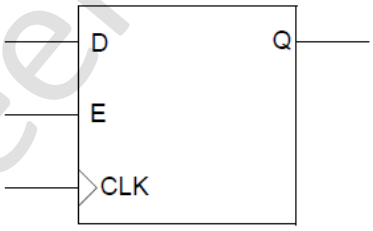
LAT_WIDTH: Determine the width of input data and output q

Ports

Name	Type	Description
aset	Input	Asynchronous set input. Sets q[] output to 1.
data[]		Data Input to the D-type latch with width LAT_WIDTH
gate		Latch enable input
aclr		Asynchronous clear input. Sets q[] output to 0.
q[]	Output	Data output from the latch with with LAT_WIDTH

If both aset and aclr are both asserted, aclr is dominant.

2) Implement D-Type Flip-Flop with active high Enable

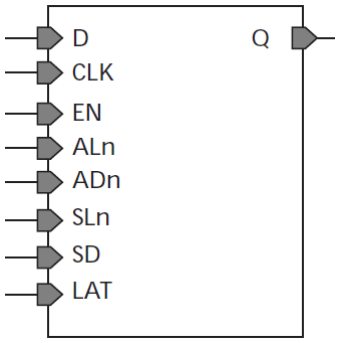


Input	Output
D, E, CLK	Q

Truth Table

E	CLK	D	Q_{n+1}
0	X	X	Q_n
1	not Rising	X	Q_n
1	↑	D	D

3) Implement the following SLE (sequential logic element)



Input		Output
Name	**Function**	
D	Data	
CLK	Clock	
EN	Enable	
ALn	Asynchronous Load (Active Low)	Q
ADn*	Asynchronous Data (Active Low)	
SLn	Synchronous Load (Active Low)	
SD*	Synchronous Data	
LAT*	Latch Enable	

***Note**: ADn, SD and LAT are static signals defined at design time and need to be tied to 0 or 1.

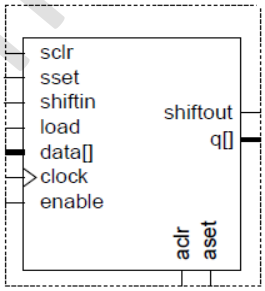
Truth Table

ALn	ADn	LAT	CLK	EN	SLn	SD	D	Q_{n+1}
0	ADn	X	X	X	X	X	X	!ADn
1	X	0	Not rising	X	X	X	X	Qn
1	X	0	↑	0	X	X	X	Qn
1	X	0	↑	1	0	SD	X	SD
1	X	0	↑	1	1	X	D	D
1	X	1	0	X	X	X	X	Qn
1	X	1	1	0	X	X	X	Qn
1	X	1	1	1	0	SD	X	SD
1	X	1	1	1	1	X	D	D

4) Implement the following Parameterized Shift register

- Parameters

Name	Value	Description
LOAD_AVALUE	Integer > 0	Value loaded with aset is high
SHIFT_DIRECTION	"LEFT" or "RIGHT"	Direction of the shift register. Default = "LEFT"
LOAD_SVALUE	Integer > 0	Value loaded with sset is high with the rising clock edge
SHIFT_WIDTH	Integer > 0	Width of data[] and q[] ports



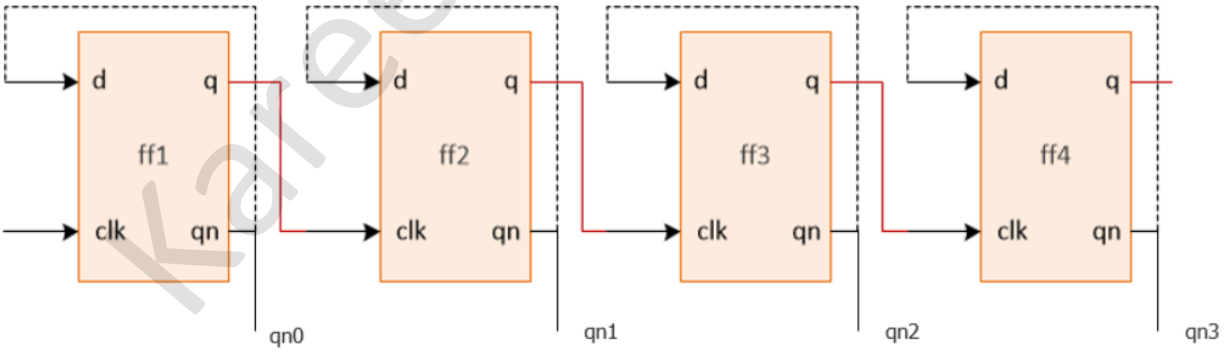
- Ports

Name	Type	Description
sclr	Input	Synchronous clear input. If both sclr and sset are asserted, sclr is dominant.
sset		Synchronous set input that sets q[] output with the value specified by LOAD_SVALUE. If both sclr and sset are asserted, sclr is dominant.
shiftin		Serial shift data input
load		Synchronous parallel load. High: Load operation with data[], Low: Shift operation
data[]		Data input to the shift register. This port is SHIFT_WIDTH wide
clock		Clock Input
enable		Clock enable input
aclr		Asynchronous clear input. If both aclr and aset are asserted, aclr is dominant.
aset		Asynchronous set input that sets q[] output with the value specified by LOAD_AVALUE. If both aclr and aset are asserted, aclr is dominant.
shiftout	Output	Serial Shift data output
q[]		Data output from the shift register. This port is SHIFT_WIDTH wide

- Note that the synchronous control signals "sclr and sset" have dominance over the enable signal but the enable signal is dominant over the load signal.

5)

1. Implement 4-bit Ripple counter with asynchronous active low set using behavioral modelling that increment from 0 to 15
    a. Inputs: set, clk;
    b. outputs: [3:0] out;
2. Implement Asynchronous D Flip-Flop with Active low reset
    a. Inputs: d, rstn, clk
    b. Outputs: q, qbar
3. Implement the below 4-bit Ripple counter using structural modelling (use Dff in step 2 where the output is taken from the qn as shown below)
    a. Inputs: clk, rstn;
    b. Outputs: [3:0] out;
4. Test the above structural design using a testbench
    — Testbench should instantiate the previous two designs
    — Consider the behavioral design as the golden model and check the functionality of the structural design.



Deliverables:

1) The assignment should be submitted as a PDF file with this format <your_name>_Assignment2 for example Kareem_Waseem_Assignment2
2) Snippets from the waveforms captured from QuestaSim for each design with inputs assigned values and output values visible

Note that your document should be organized as 5 sections corresponding to each design above, and in each section, I am expecting the Verilog code, and the waveforms snippets