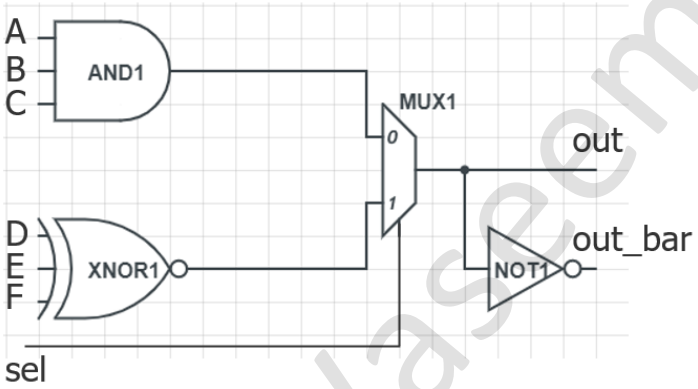
Combinational Circuit Design

Design the following circuits using Verilog **and create a testbench (directed or randomized)** for each design to check its functionality

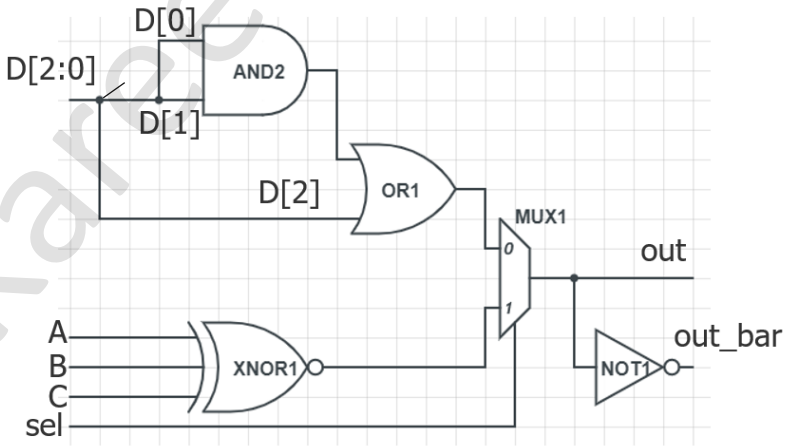
1)

- The design has 7 inputs and 2 outputs
- Use assign statements (structural coding style) to design the following



2)

- The design has 5 inputs and 2 outputs
- Use Behavioral coding style to implement the basic gates



3) Design a 4-bit priority encoder, the following truth table is provided where x is 4-bit input and y is a 2-bit output

x3	x2	x1	x0	y1	y0
1	X	X	X	1	1
0	1	X	X	1	0
0	0	1	X	0	1
0	0	0	X	0	0

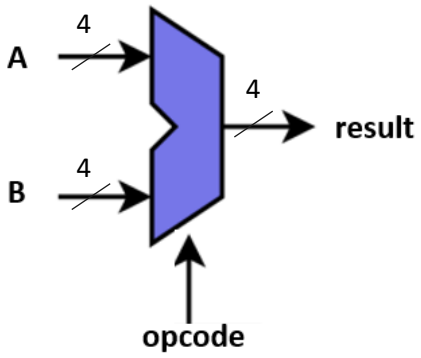
4) Implement N-bit adder using Dataflow modeling style

- The design takes 2 inputs (A, B) and the summation is assigned to output (C) ignoring the carry

5) Design N-bit ALU that perform the following operations

- The design has 3 inputs and 1 output
- Instantiate the half adder from the previous design
- For the subtraction, subtract B from A "A – B"

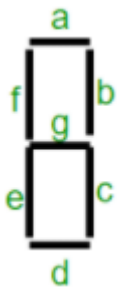
Inputs		Outputs
opcode		Operation
0	0	Addition
1	0	Subtraction
0	1	OR
1	1	XOR

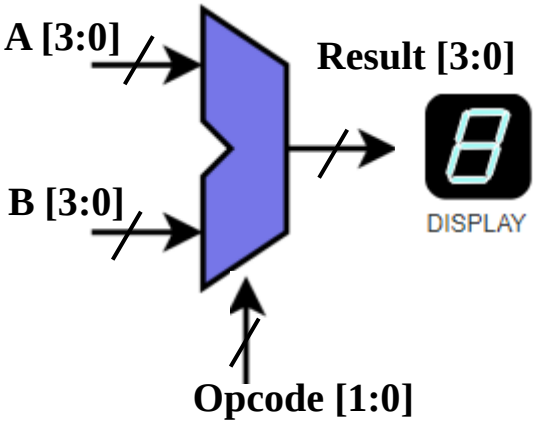


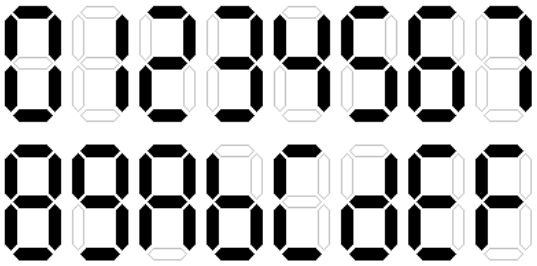
6) Implement 4-bit ALU display on 7 Segment LED Display

- The design has 4 inputs: A, B, opcode, enable.
- The design has 7 outputs (a-g)
- Instantiate the N-bit ALU designed in the previous design with parameter N = 4
- ALU should execute the operation on A and B depending on the input opcode
- ALU output should be considered as the digit to be displayed on the 7 segment LED display
- Below the truth table of the 7-segment decoder

	Input	Output						
Digit	enable	a	b	c	d	e	f	g
0	1	1	1	1	1	1	1	0
1	1	0	1	1	0	0	0	0
2	1	1	1	0	1	1	0	1
3	1	1	1	1	1	0	0	1
4	1	0	1	1	0	0	1	1
5	1	1	0	1	1	0	1	1
6	1	1	0	1	1	1	1	1
7	1	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1	1
9	1	1	1	1	1	0	1	1
A	1	1	1	1	0	1	1	1
b	1	0	0	1	1	1	1	1
C	1	1	0	0	1	1	1	0
d	1	0	1	1	1	1	0	1
E	1	1	0	0	1	1	1	1
F	1	1	0	0	0	1	1	1
x	0	0	0	0	0	0	0	0







7-segment decoder

Deliverables:

1) The assignment should be submitted as a PDF file with this format <your_name>_Assignment1 for example Kareem_Waseem_Assignment1
2) Snippets from the waveforms captured from Modelsim for each design with inputs assigned values and output values visible

Note that your document should be organized as 6 sections corresponding to each design above, and in each section, I am expecting the Verilog code and the waveforms snippets