بسم الله الرحمن الرحيم

Project Title: Transistor-Level BUFFER Gate Design

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17 ذو القعدة، 1446

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1. Abstraction

This report presents the design and implementation of a BUFF gate at the transistor level, leveraging 130nm MOSFET technology. The circuit was meticulously developed and simulated using Cadence Virtuoso.

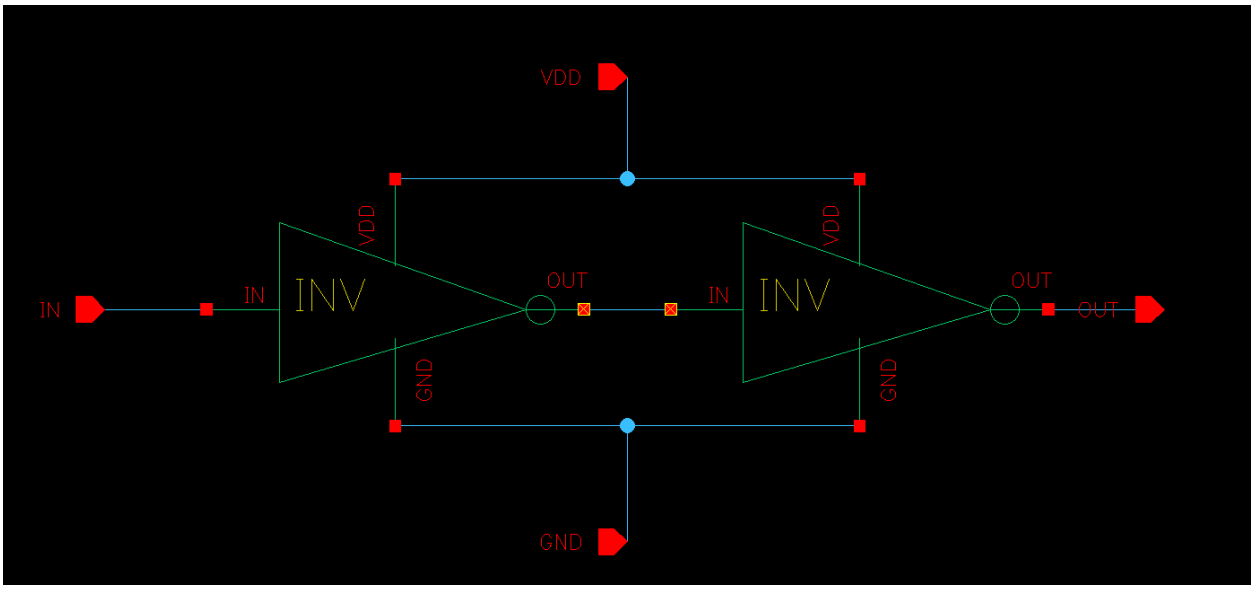
2. Logic Function and Truth Table

Y = IN

IN	Y (BUFF)
0	0
1	1

3. Circuit Design

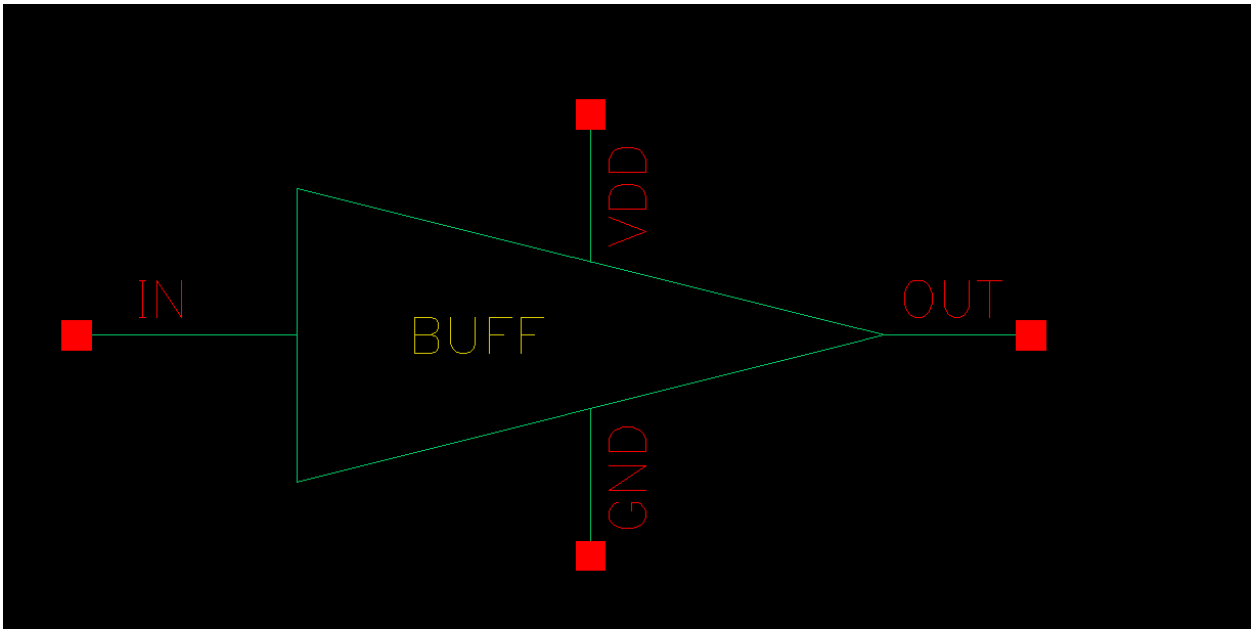
3.1. Schematic



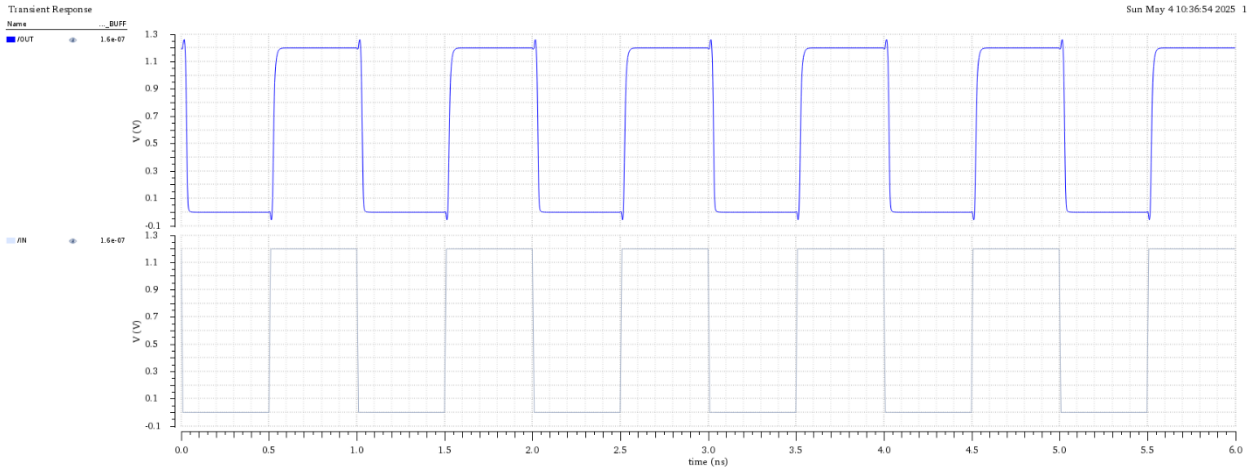
3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: IN
- OUTPUT: OUT
- Input Parameter: WN_BUFF
- Sizes: the NMOS has dimension WN_BUFF, while the PMOS has dimension 1.8* WN_BUFF
- why 1.8? (came from simulation of the basic INV) therefore MIN T_{PO} INV.

3.3. Symbol



4. Simulation and Results



Note: the simulation result is performed with an input f = 1.25GHZ for IN.