بسم الله الرحمن الرحيم

Project Title: Transistor-Level INV Gate Design

- Author: Ahmed Assem Mohamed

17 ذو القعدة، 1446

MAY 14, 2025

1. Abstraction

This report presents the design and implementation of a INV gate at the transistor level, leveraging 130nm MOSFET technology. The circuit was meticulously developed and simulated using Cadence Virtuoso.

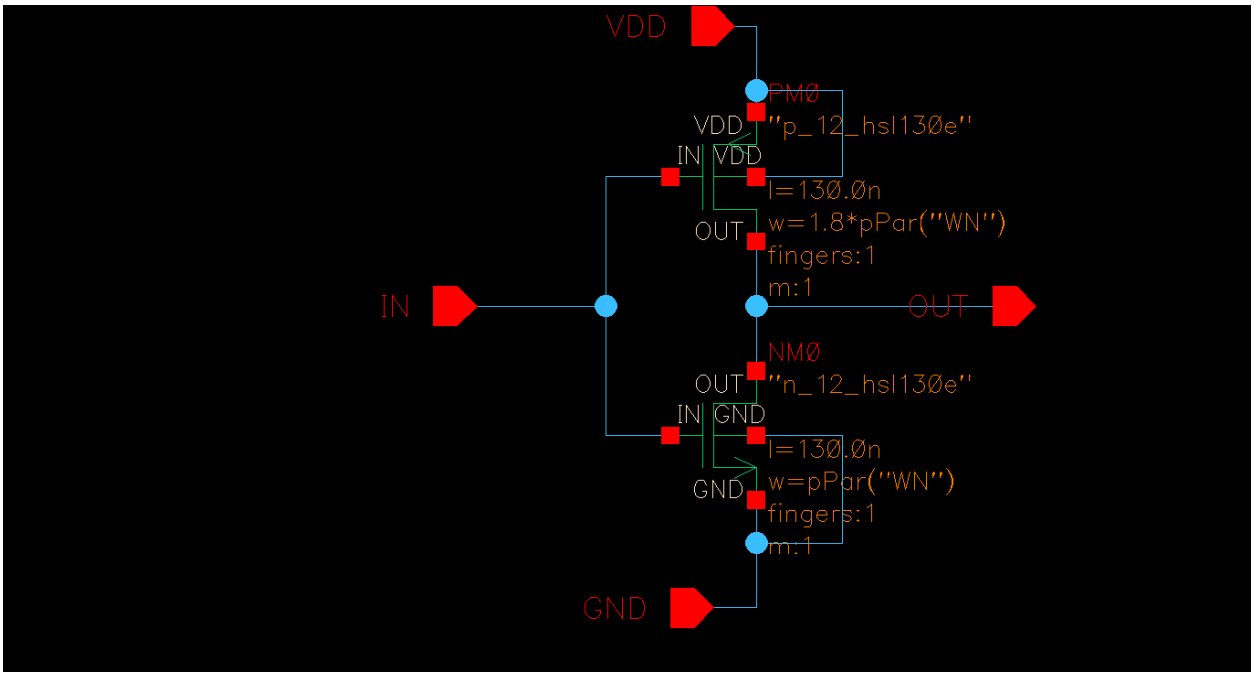
2. Logic Function and Truth Table

Y = ~(IN)

IN	Y (INV)
0	1
1	0

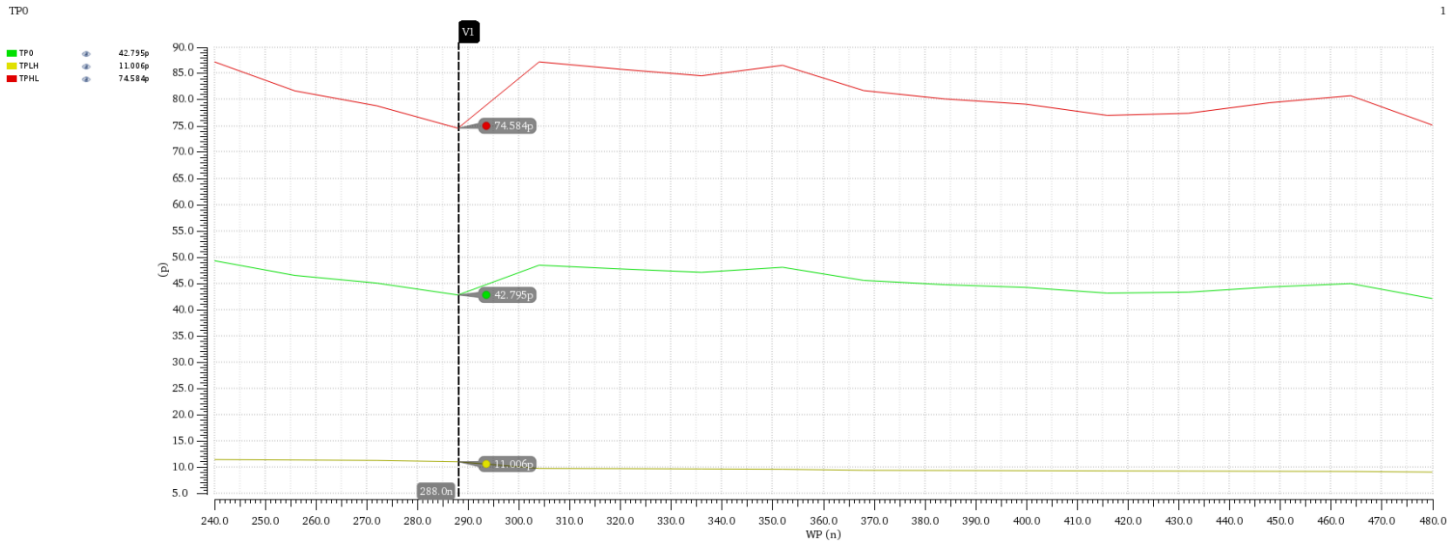
3. Circuit Design

3.1. Schematic



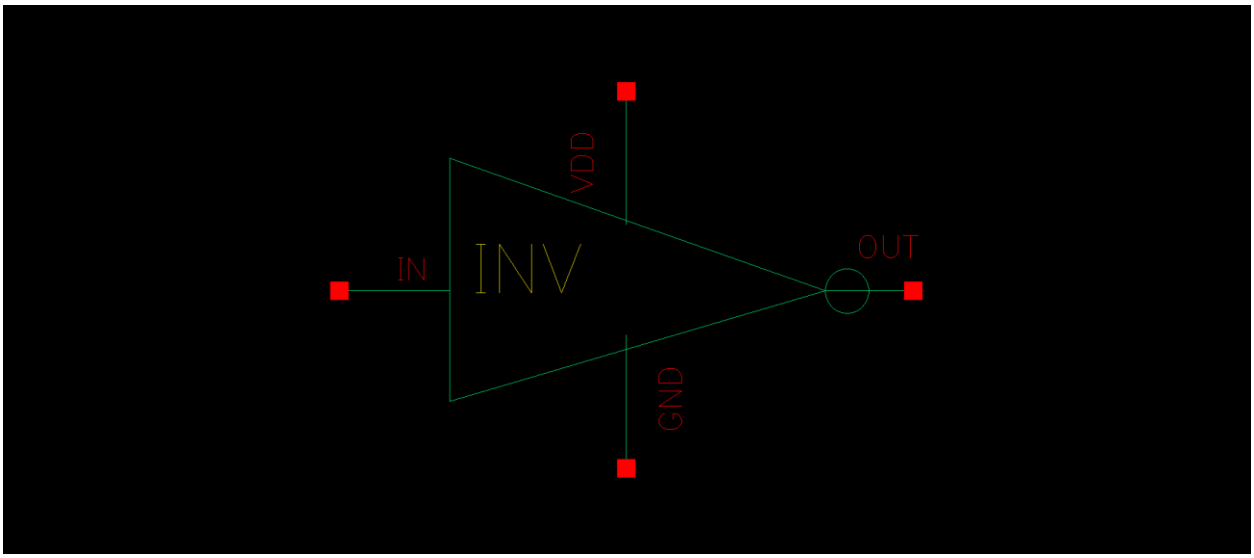
3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: IN
- OUTPUT: OUT
- Input Parameter: WN_INV
- Sizes: the NMOS has dimension WN_INV, while the two PMOS has dimension 1.8* WN_INV
- why 1.8? (came from simulation) therefore min T_{po} INV.

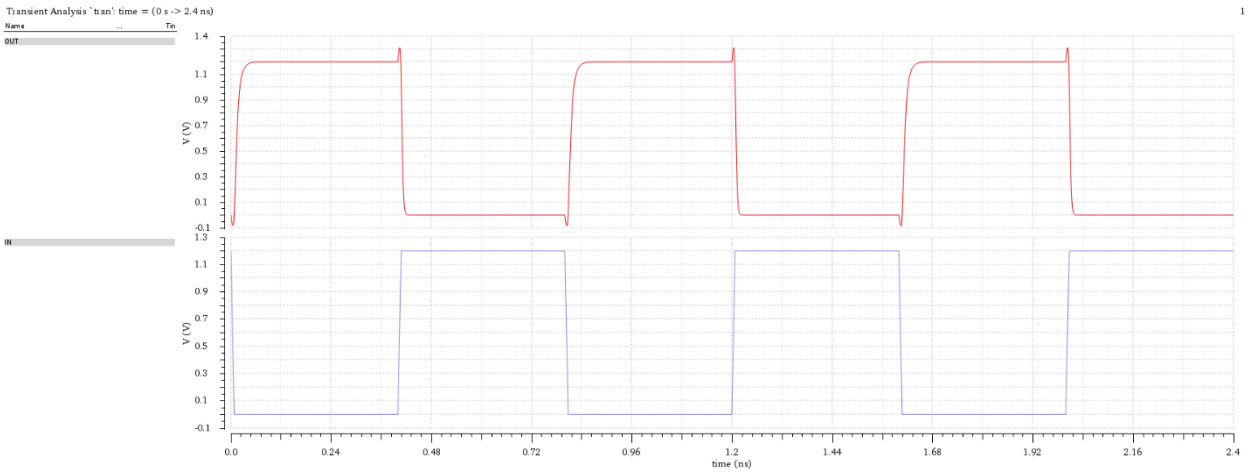


- The previous graph is simulation of (T_{PLH}, T_{PHL}, T_{P0}) VS WP at const WN = 160nm. therefore WP = 288nm (WP/WN = 288/160 = 1.8)
  note: T_{P0} is the average

3.3. Symbol



4. Simulation and Results



Note: the simulation result is performed with an input f = 1.25GHZ for IN.