بسم الله الرحمن الرحيم

Project Title: Transistor-Level 4-BIT ALU DESIGN

Module: 4-BIT MULTPLIER UNIT
Design

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21 ذو القعدة، 1446

1. Abstraction

This report presents the design and implementation of a **4-bit signed multiplier**— a key sub-module in the ALU architecture, implemented at the transistor level using **130nm CMOS technology.** The multiplier accepts two 4-bit signed inputs (A and B) and produces an 8-bit signed output (P = A × B), supporting two's complement representation. The circuit was meticulously developed and simulated using Cadence Virtuoso.

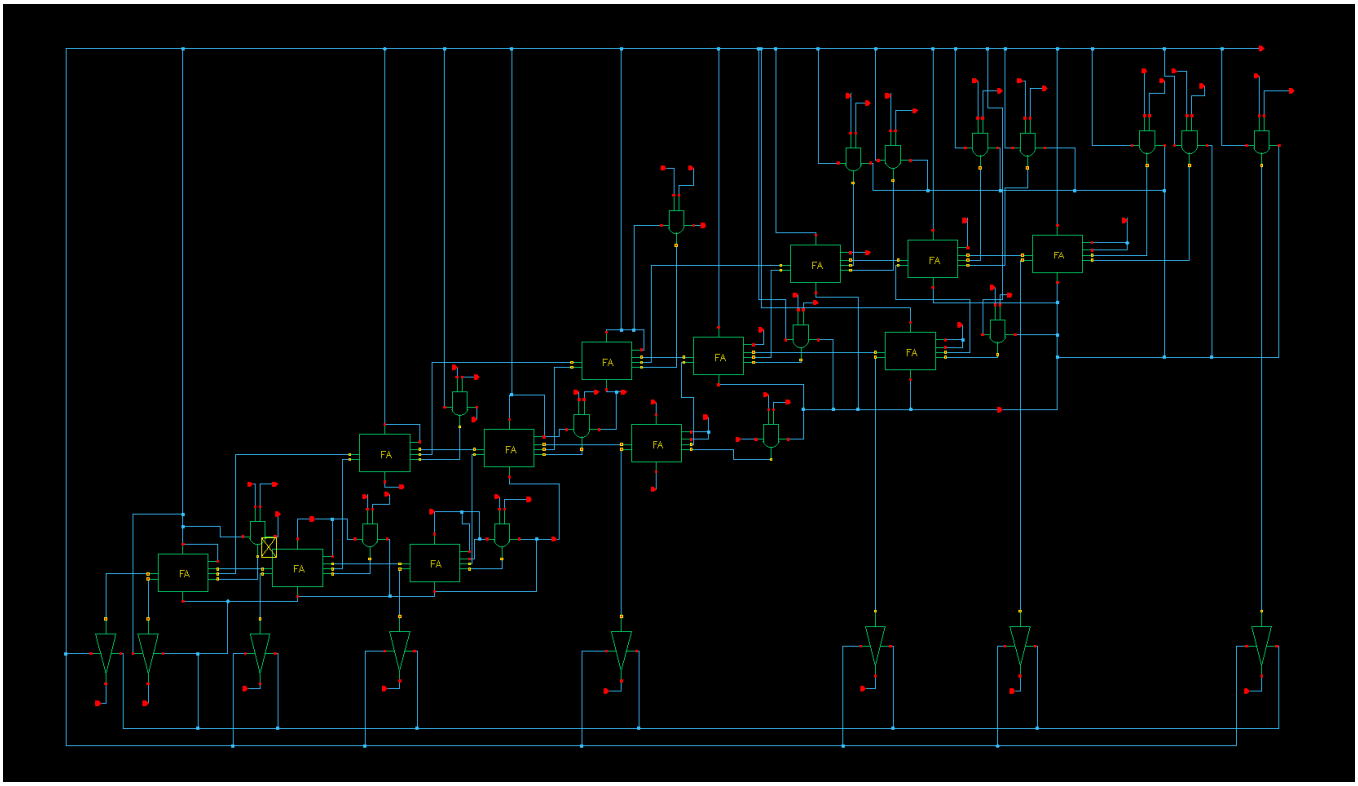
2. Logic Function and Truth Table

Some sample test cases.

A (bin)	B (bin)	A (dec)	B (dec)	Product (dec)	Product (bin)
0001	0010	+1	+2	2	0000_0010
1111	0001	-1	+1	-1	1111_1111
1100	0011	-4	+3	-12	1111_0100
0110	1010	+6	-4	-24	1110_1000
1110	1110	-2	-2	+4	0000_0100

3. Circuit Design

3.1. Schematic

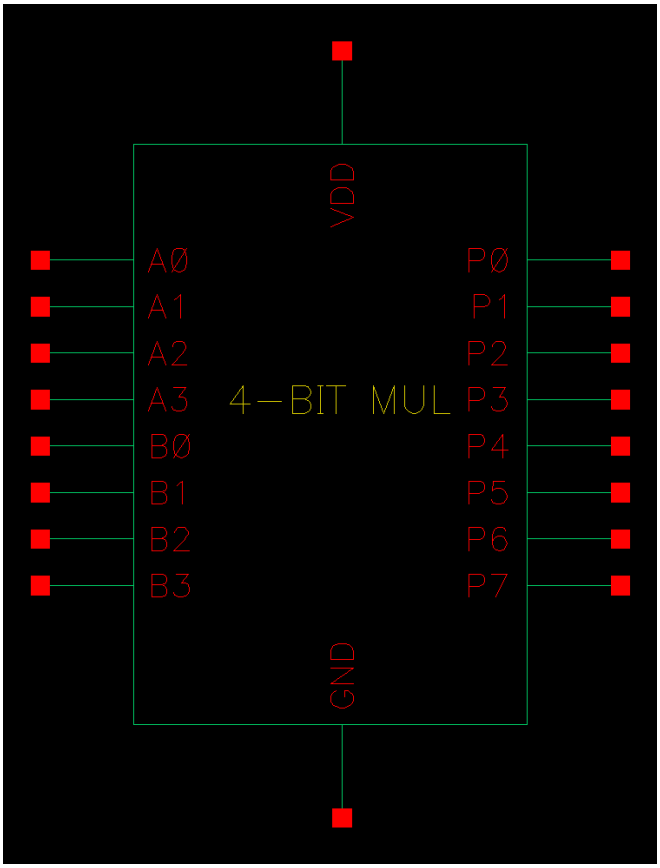


3.2. Design Approach

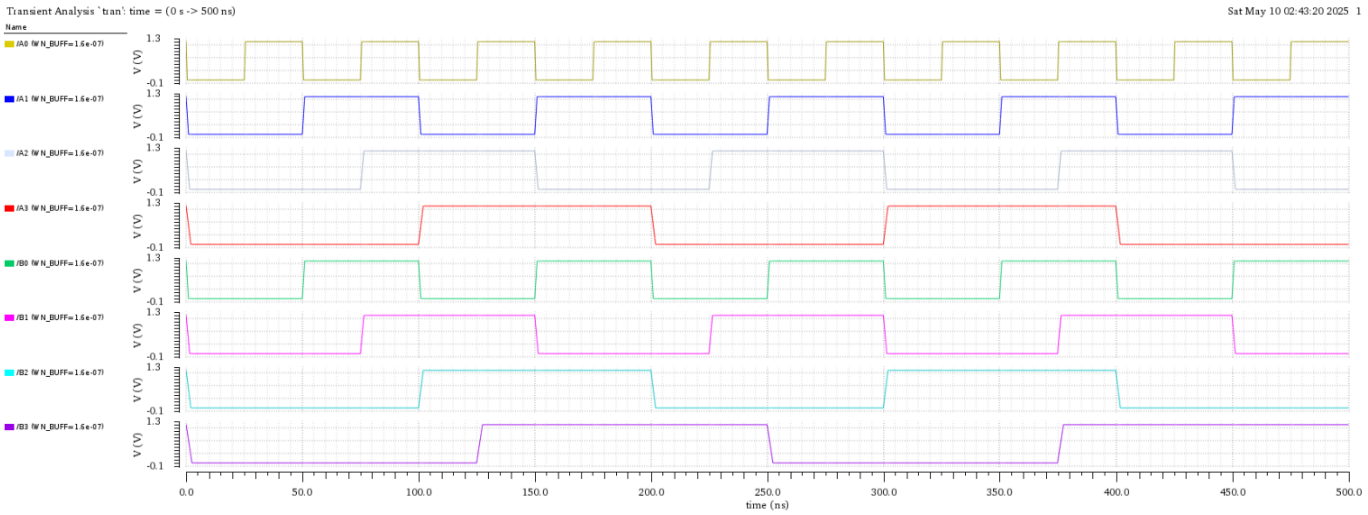
- 130nm CMOS process
- 1.2V VDD
- INPUTS: 4-BIT IN0, 4-BIT IN1
- OUTPUTS: 8-BIT OUT
- Input parameter: WN_MUL
- Gates used: 12*FA, 16*AND, 8*BUFF
  Note: number of used FA can be only 8 and 4 units for HA, but the FA circuit I already designed, so I used only FA in the whole design.
- Sizes: WN_MUL, WN_MUL, 4*WN_MUL

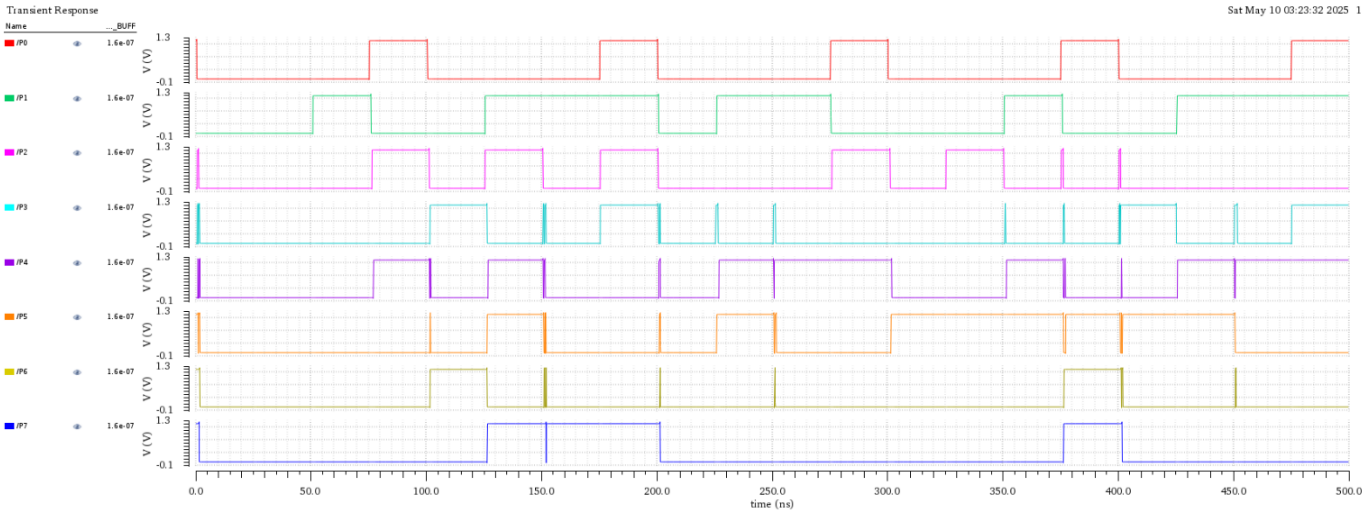
- why? As the BUFF is the last stage, it is supposed to be strong enough to drive the following stage, but (4) exactly is designed only by intuition.
- Partial product generation done via AND gates.
- Summation using ripple adder tree structure.

3.3. Symbol



4. Simulation and Results





Note: the simulation result is performed with a max input f = 20.0MHZ