بسم الله الرحمن الرحيم

Project Title: Transistor-Level NAND Gate Design

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17 ذو القعدة، 1446

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1. Abstraction

This report presents the design and implementation of a NAND gate at the transistor level, leveraging 130nm MOSFET technology. The circuit was meticulously developed and simulated using Cadence Virtuoso.

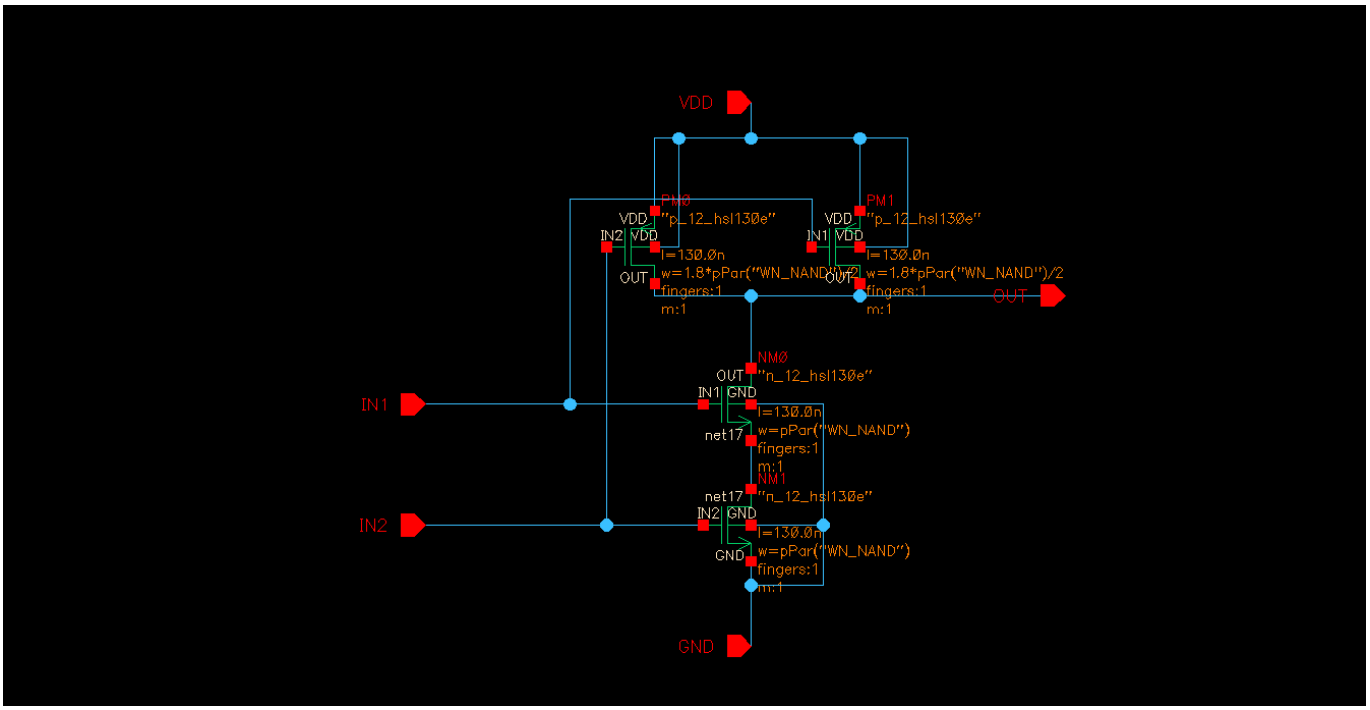
2. Logic Function and Truth Table

Y = ~(IN0 . IN1)

IN0	IN1	Y (IN0 NAND IN1)
0	0	1
0	1	1
1	0	1
1	1	0

3. Circuit Design

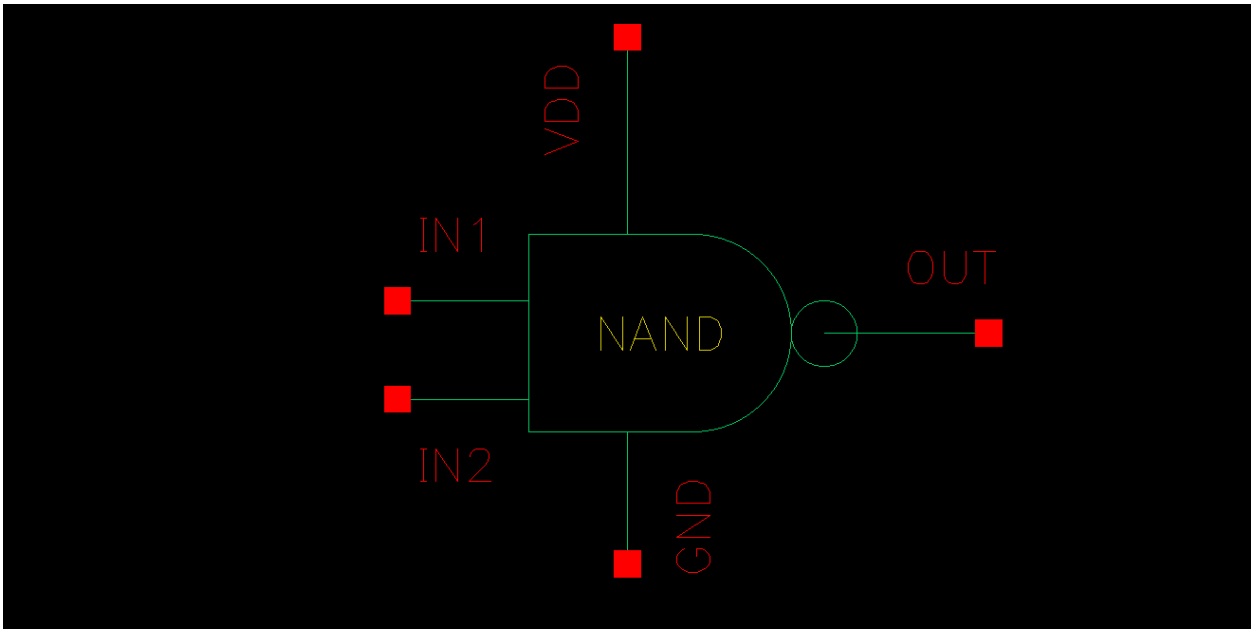
3.1. Schematic



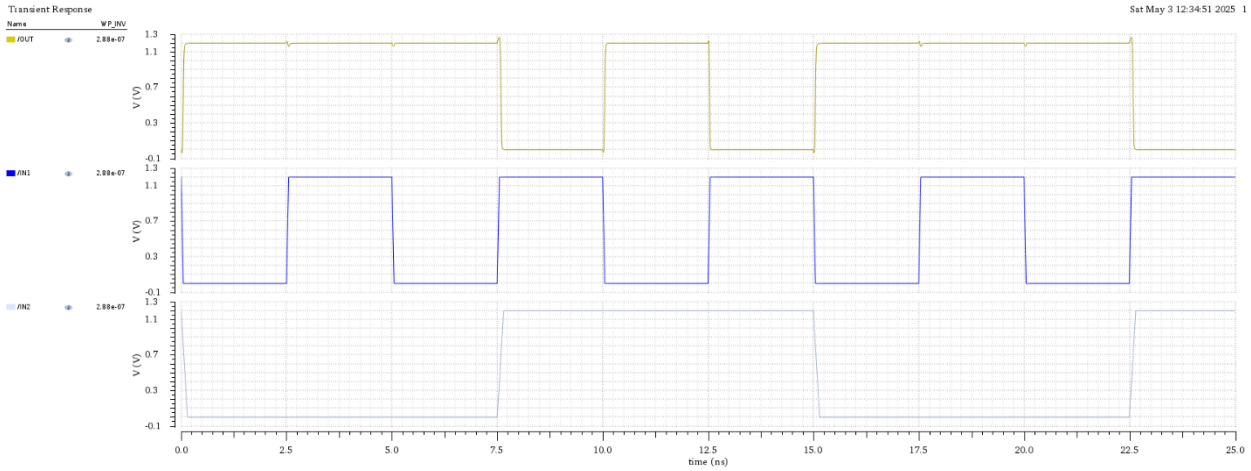
3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: IN0, IN1
- OUTPUT: OUT
- Input Parameter: WN_NAND
- Sizes: the two NMOS have the dimensions WN_NAND, while the two PMOS have the dimensions 1.8* WN_NAND /2
- why 1.8? (came from simulation of the basic INV) therefore a symmetric INV. Note: now g(Logical effort) of NAND = 1.36
- why two? to have the same R-ON of the ref INV.

3.3. Symbol



4. Simulation and Results



Note: the simulation result is performed with an input f = 333.3MHZ for IN1, while for IN2 1/3 * f