بسم الله الرحمن الرحيم

Project Title: Transistor-Level 4-BIT ALU DESIGN

Module: 1-BIT LOGIC UNIT
Design

- Author: Ahmed Assem Mohamed

May 18, 2025

21 ذو القعدة، 1446

1. Abstraction

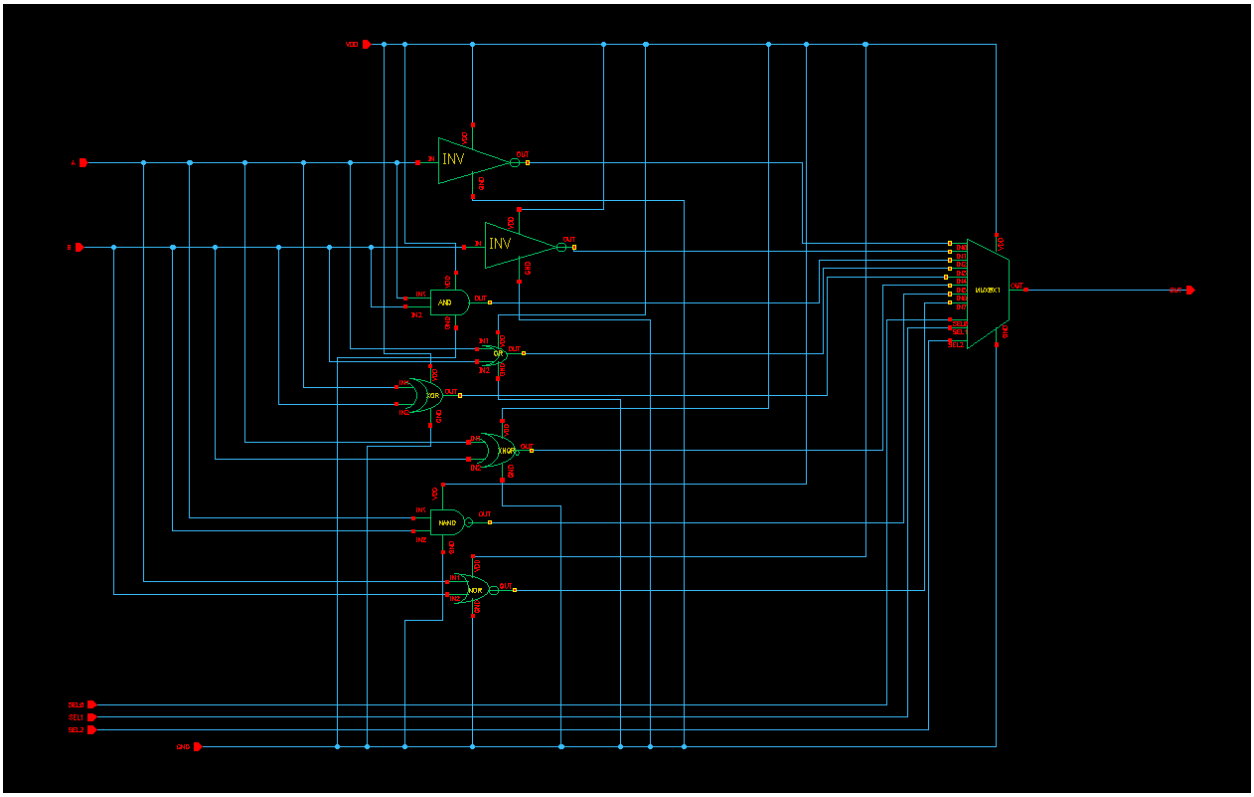
This report presents the design and implementation of a **Logical Unit (LU)** — a key sub-module in the ALU architecture, implemented at the transistor level using **130nm CMOS technology.** The LU performs basic **bitwise logical operations** on two 1-bit signed inputs, A and B, based on a 3-bit control word. The circuit was meticulously developed and simulated using Cadence Virtuoso.

2. Logic Function and Truth Table

A0	B0	SEL2	SEL1	SEL0	FUNC	OUT
0	0	0	0	0	~A	1
1	1	0	0	1	~B	0
0	0	0	1	0	A & B	0
1	1	0	1	1	A | B	1
0	0	1	0	0	A ^ B	0
1	1	1	0	1	~(A ^ B)	1
0	0	1	1	0	~(A & B)	1
1	1	1	1	1	~(A | B)	0

3. Circuit Design

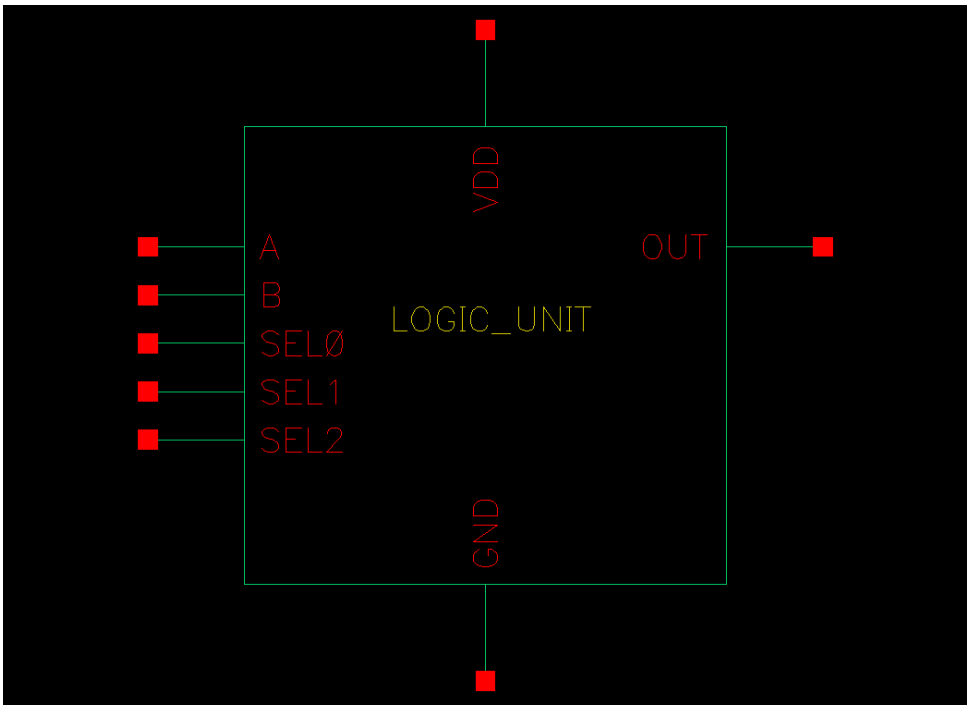
3.1. Schematic



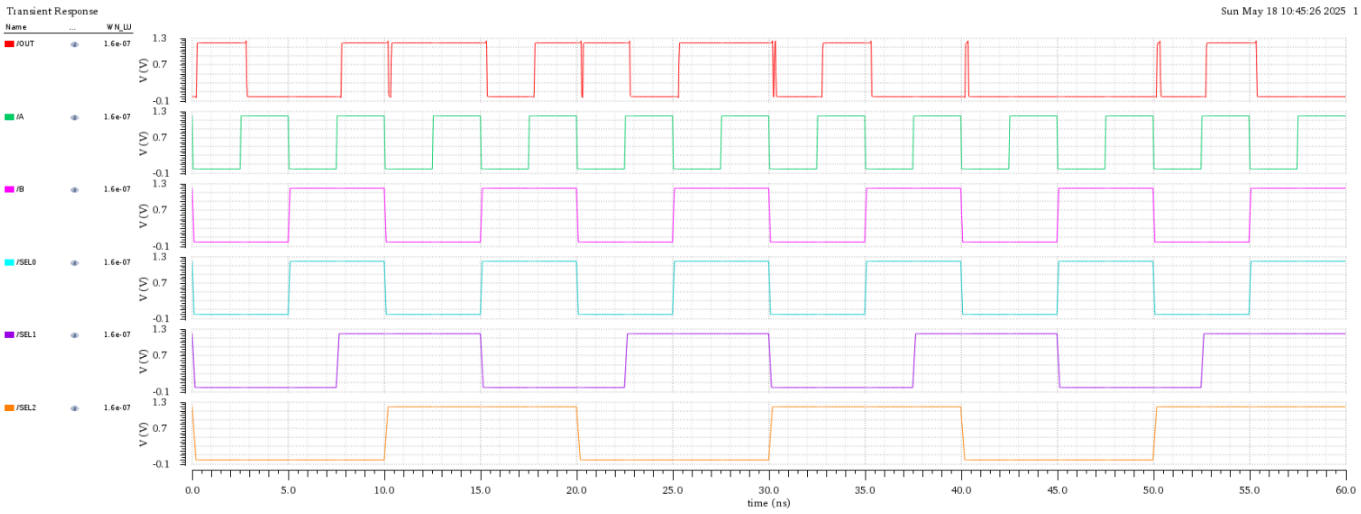
3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: INI0, IN1, SEL0, SEL1, SEL2
- OUTPUT: OUT
- Input Parameter: WN_LU
- Sizes All gates have this size(even if it is the parameter for MUX-8X1)
- why? as already each gate is designed alone which is suitable size. this parameter is only to reduce the number of variables.

3.3. Symbol



4. Simulation and Results



ALU:LOGIC_UNIT_TB:1	VOUT				
ALU:LOGIC_UNIT_TB:1	A				
ALU:LOGIC_UNIT_TB:1	B				
ALU:LOGIC_UNIT_TB:1	SEL0				
ALU:LOGIC_UNIT_TB:1	SEL1				
ALU:LOGIC_UNIT_TB:1	SEL2				
ALU:LOGIC_UNIT_TB:1	ENERGY	21.03u			
ALU:LOGIC_UNIT_TB:1	/I0/VDD				

Note: the simulation result is performed with an input f = 200MHZ for IN1, IN2: 1/2 * f, SEL0: 1/2 * f, SEL1: 1/3 * f, SEL2: 1/4 * f