بسم الله الرحمن الرحيم

Project Title: Transistor-Level 4-BIT ALU Design

Module: 4-BIT ARITHMETIC UNIT Design

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21 ذو القعدة، 1446

1. Abstraction

This report presents the design and implementation of a **4-bit Arithmetic Logic Unit (ALU)** — a key sub-module in the ALU architecture, implemented at the transistor level using **130nm CMOS technology.** The AU performs binary arithmetic operations on two 4-bit signed inputs, A and B, based on a 3-bit control word, and produces an **8-bit signed output**. The circuit was meticulously developed and simulated using Cadence Virtuoso.

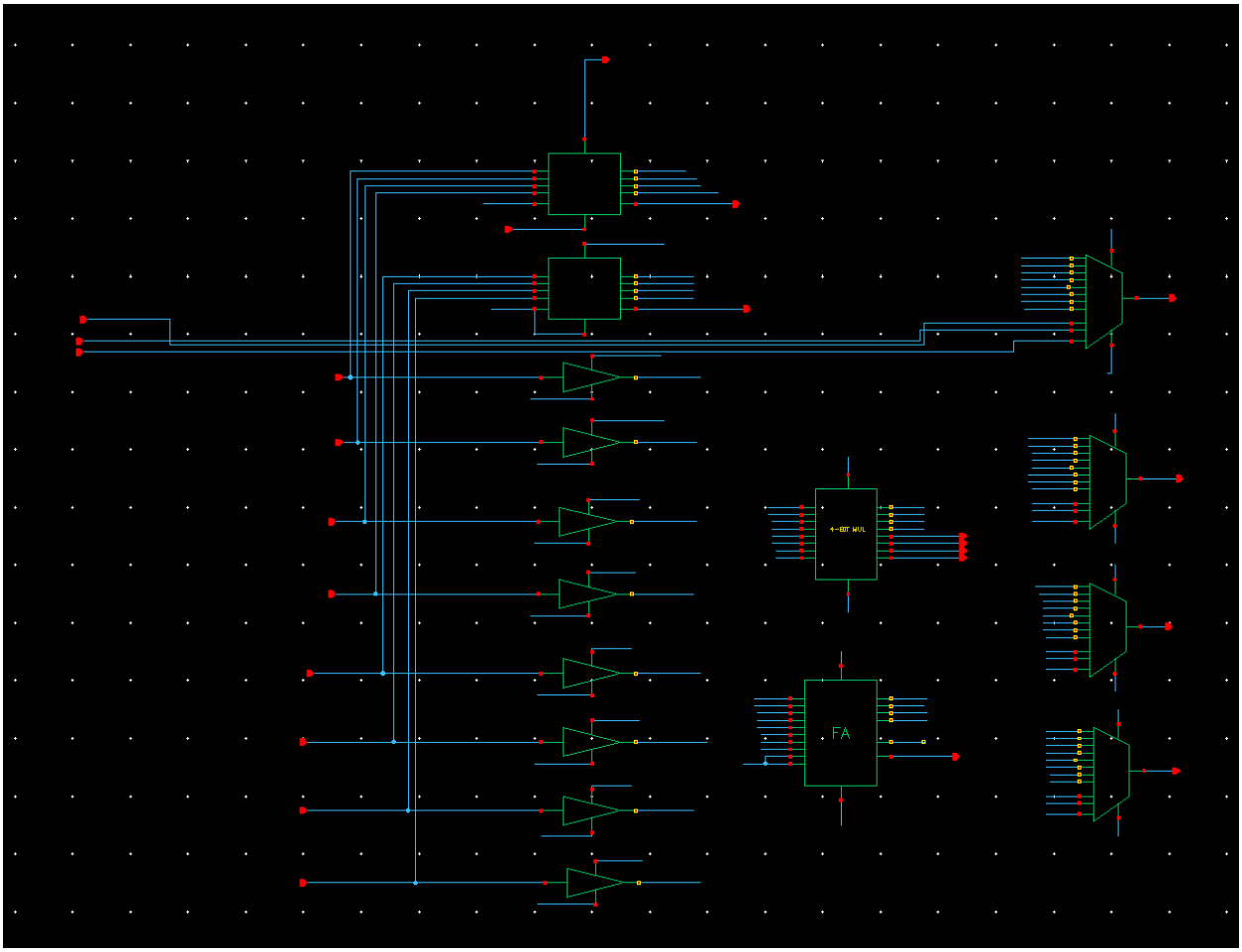
2. Logic Function and Truth Table

OUT[8:0] = A[3:0] FUNC B[3:0]

SEL2	SEL1	SEL0	FUNC
0	0	0	A++
0	0	1	B++
0	1	0	A
0	1	1	B
1	0	0	A--
1	0	1	A * B
1	1	0	A + B
1	1	1	A - B

3. Circuit Design

3.1. Schematic

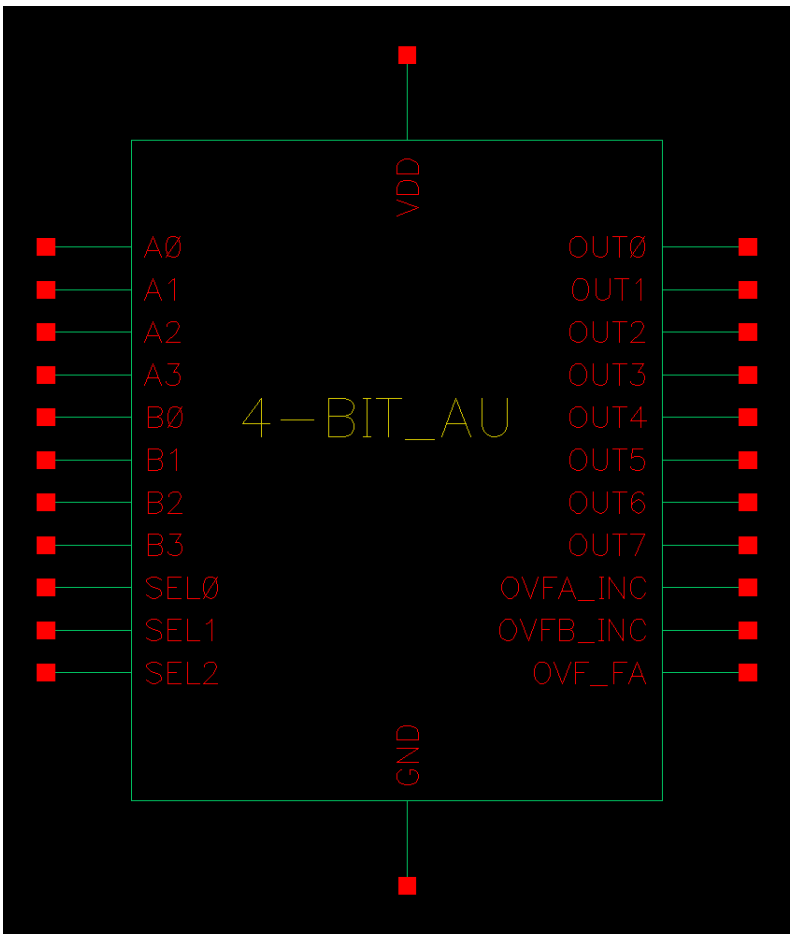


3.2. Design Approach

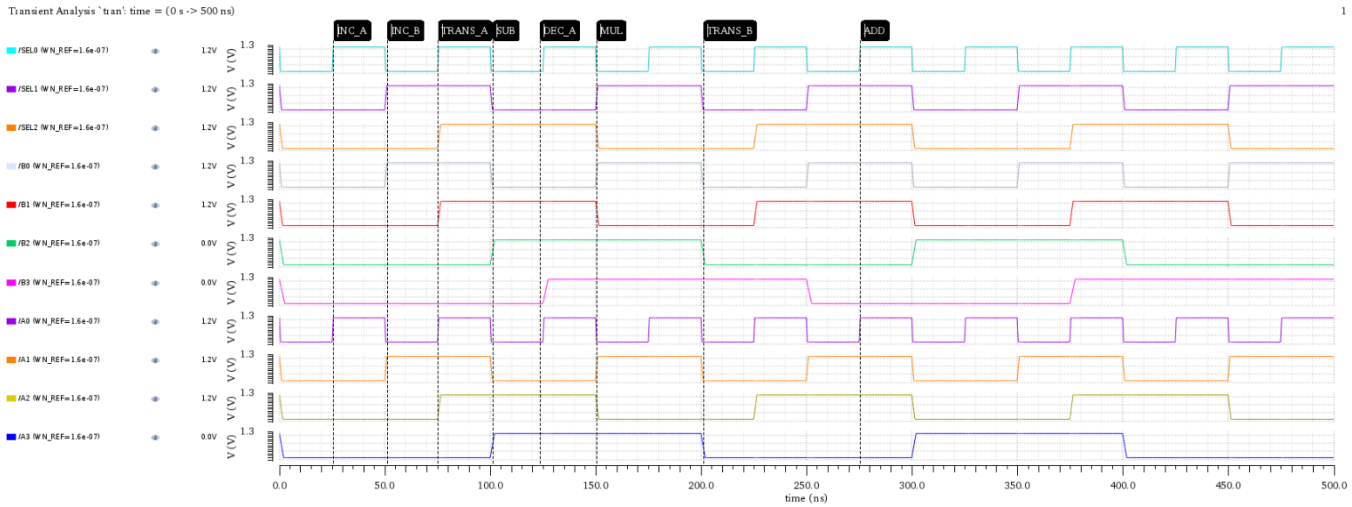
- 130nm CMOS process
- 1.2V VDD
- INPUTS: 4-BIT IN0, 4-BIT IN1, 3 SEL
- OUTPUTS: 8-BIT OUT, 3-BIT OVF
- OVF Flags: one for the full adder circuit, one for the A increment circuit, one for the B increment circuit.
  notes: they are based on signed inputs.
- Input parameter: WN_AU

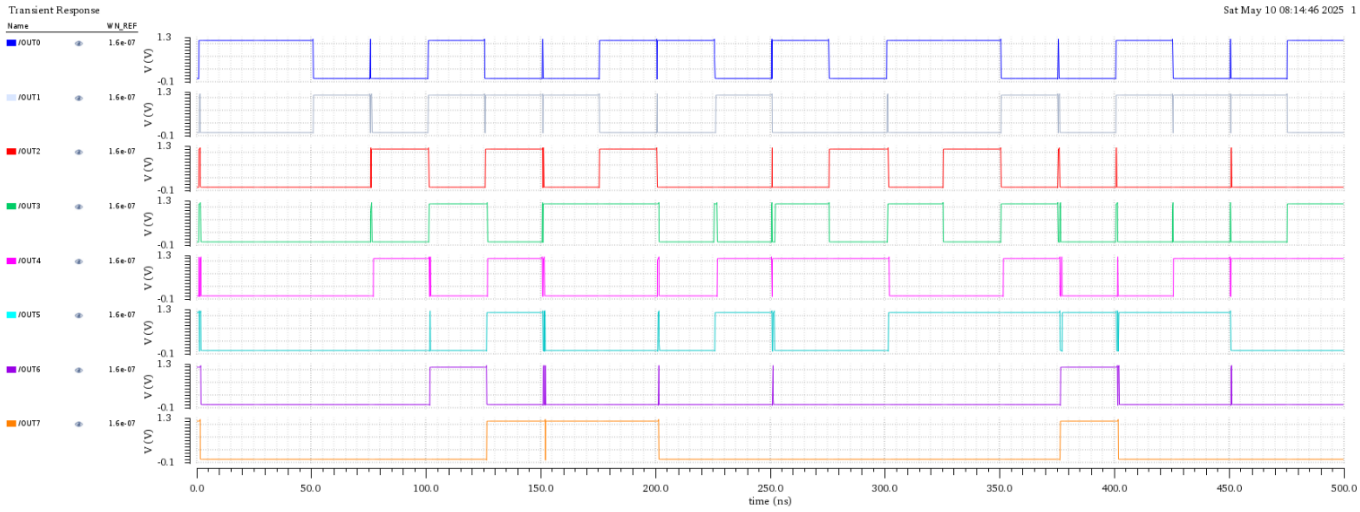
- SIZES: All gates have this size(even if it is the parameter for MUX-8X1)
- why? as already each gate is designed alone which is suitable size. this parameter is only to reduce the number of variables.

3.3. Symbol



4. Simulation and Results





Note: the simulation result is performed with a max f = 20.0MHZ