بسم الله الرحمن الرحيم

Project Title: Transistor-Level 4-BIT ALU Design

Module: MUX-8X1 UNIT
Design

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1. Abstraction

This report presents the design and implementation of a multiplexer (MUX 8×1) at the transistor level using **MOSFET** technology, leveraging **130nm CMOS technology**. The circuit was meticulously developed and simulated using Cadence Virtuoso.

2. Logic Function and Truth Table

SEL2	SEL1	SEL0	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0	Y
0	0	0	X	X	X	X	X	X	X	0	0
0	0	1	X	X	X	X	X	X	1	X	1
0	1	0	X	X	X	X	X	0	X	X	0
0	1	1	X	X	X	X	1	X	X	X	1
1	0	0	X	X	X	0	X	X	X	X	0
1	0	1	X	X	1	X	X	X	X	X	1
1	1	0	X	0	X	X	X	X	X	X	0
1	1	1	1	X	X	X	X	X	X	X	1

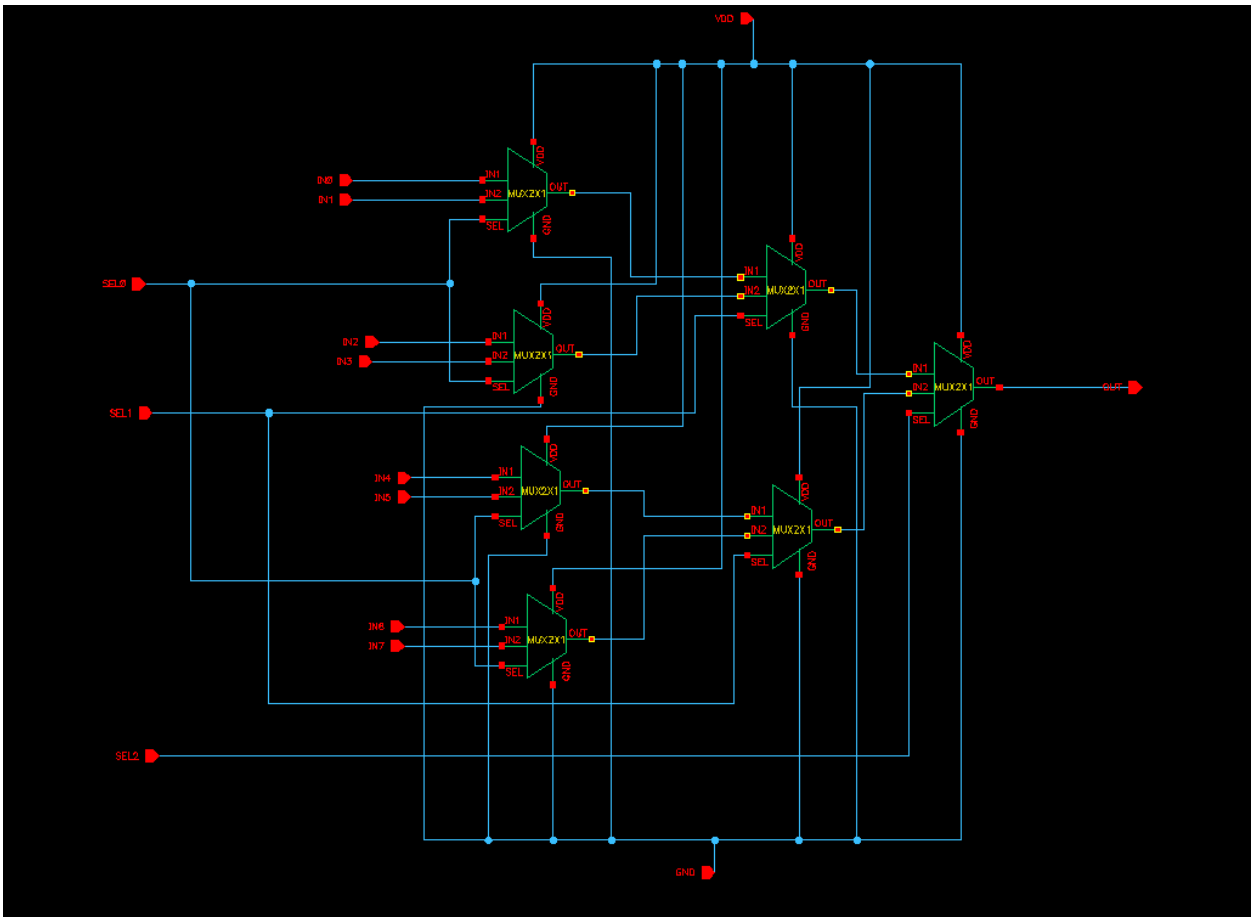
Explanation:

- When SEL[2:0] = 000, the output is IN0.
- When SEL[2:0] = 001, the output is IN1.
- When SEL[2:0] = 010, the output is IN2.
- When SEL[2:0] = 011, the output is IN3.
- When SEL[2:0] = 100, the output is IN4.
- When SEL[2:0] = 101, the output is IN5.
- When SEL[2:0] = 110, the output is IN6.

- When SEL[2:0] = 111, the output is IN7.

3. Circuit Design

3.1. Schematic



3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: IN0, IN1, IN2, IN3, IN4, IN5, IN6, IN7, SEL0, SEL1, SEL2
- OUTPUT: OUT

- Input Parameter: WN_MUX
- Sizes: WN_MUX

3.3. Symbol