بسم الله الرحمن الرحيم

Project Title: Transistor-Level 2X1 Multiplexer Design

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17 ذو القعدة، 1446

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1. Abstraction

This report presents the design and implementation of a multiplexer (MUX 2×1) at the transistor level using MOSFET technology, leveraging 130nm MOSFET technology. The circuit was meticulously developed and simulated using Cadence Virtuoso.

2. Logic Function and Truth Table

Y = ~SEL . IN0 | SEL . IN1

SEL	IN0	IN1	Y (OUT)
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

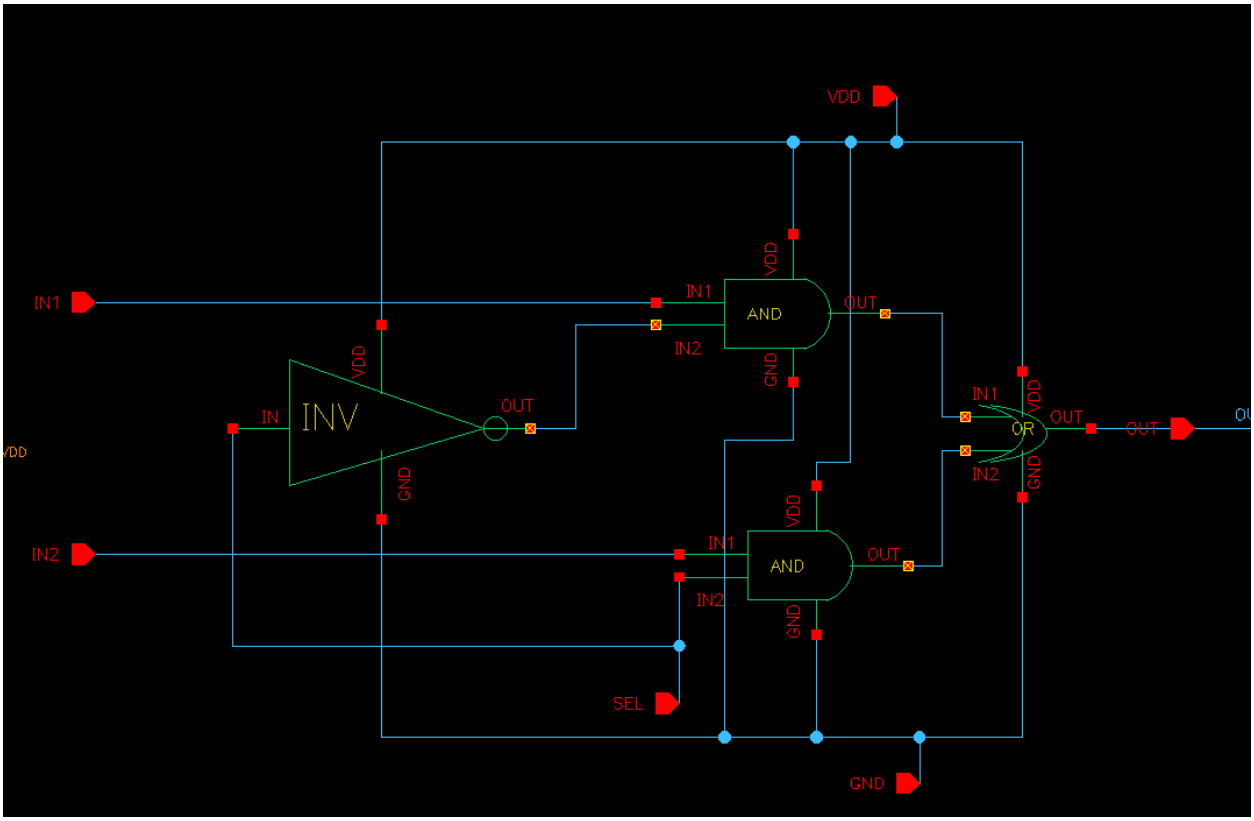
Explanation:

When S = 0, the output is IN0.

When S = 1, the output is IN1.

3. Circuit Design

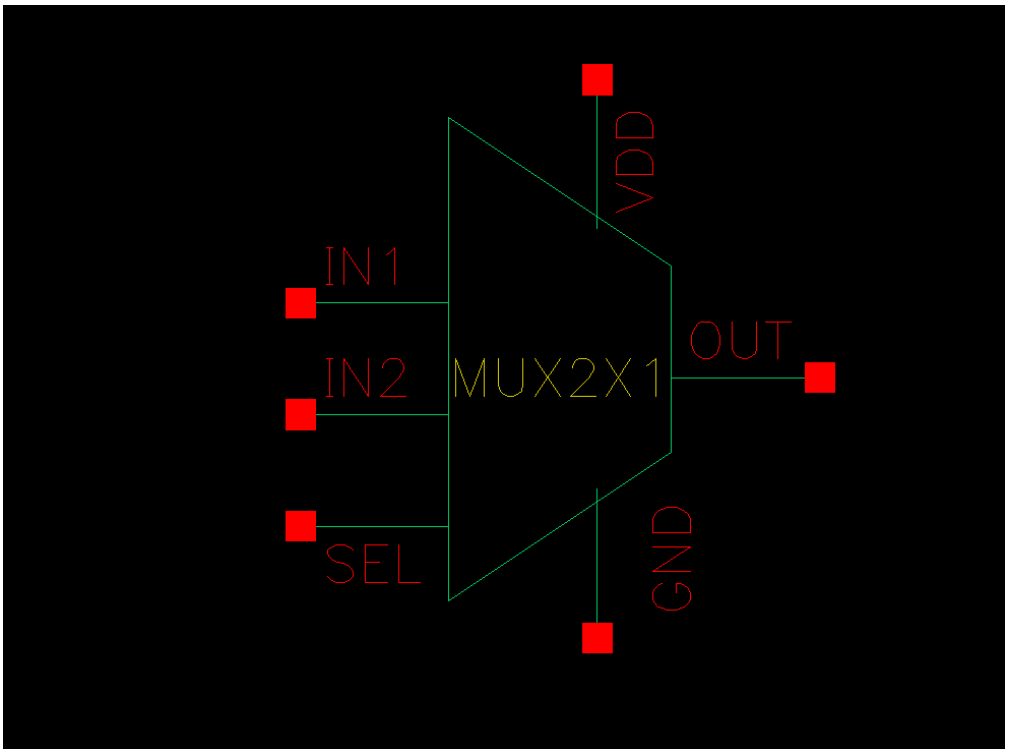
3.1. Schematic



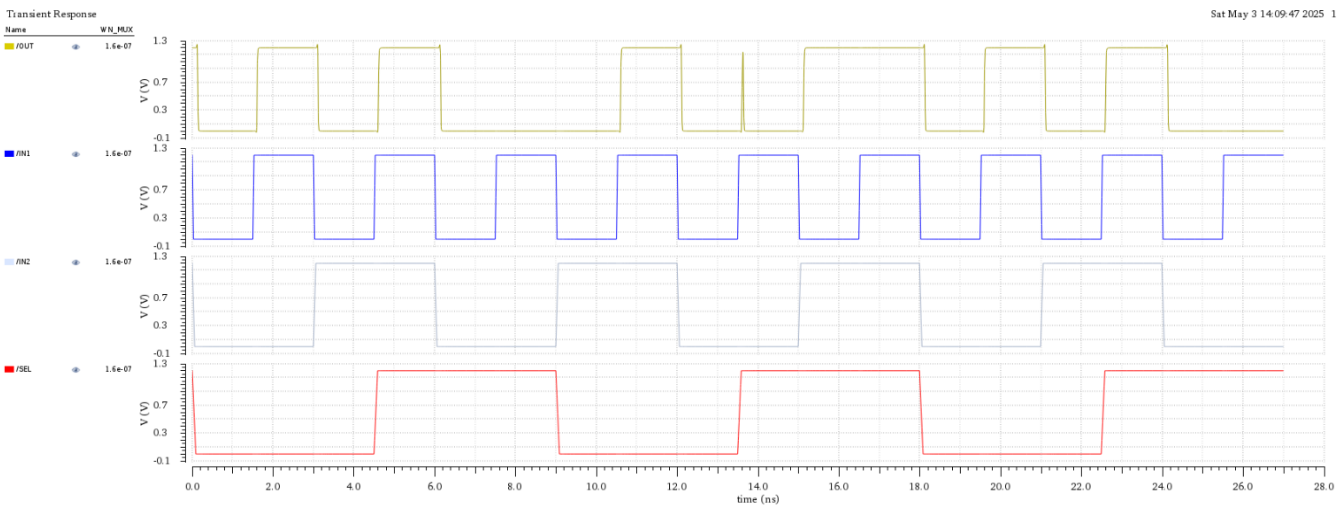
3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: IN0, IN1,SEL
- OUTPUT: OUT
- Input Parameter: WN_MUX
- Sizes: And: 2.5*WN_MUX, OR: 5*WN_MUX, INV: WN_MUX
- why? : The sizes of gates are approximated calculation based on the logical effort of each gate, not simulation results while assuming CL = 15*CREF(INV).

3.3. Symbol



4. Simulation and Results



Note: the simulation result is performed with an input f = 333.3MHZ for IN1, while for IN2 1/3 * f