بسم الله الرحمن الرحيم

Project Title: Transistor-Level AND Gate Design

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17 ذو القعدة، 1446

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1. Abstraction

This report presents the design and implementation of an AND gate at the transistor level, leveraging 130nm MOSFET technology. The circuit was meticulously developed and simulated using Cadence Virtuoso.

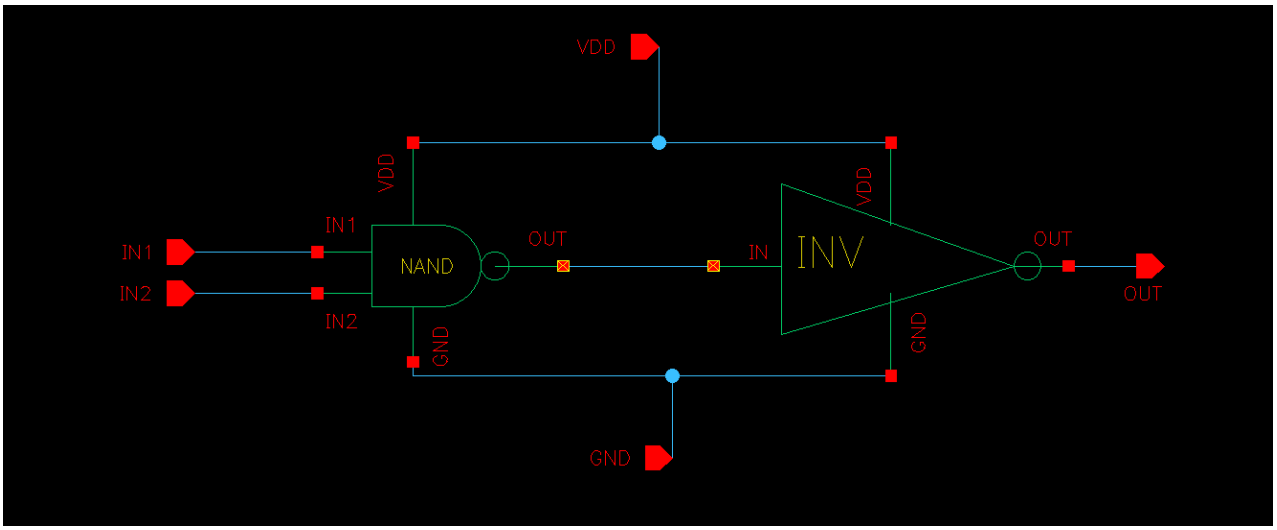
2. Logic Function and Truth Table

Y = IN0 . IN1

IN0	IN1	Y (IN0 AND IN1)
0	0	0
0	1	0
1	0	0
1	1	1

3. Circuit Design

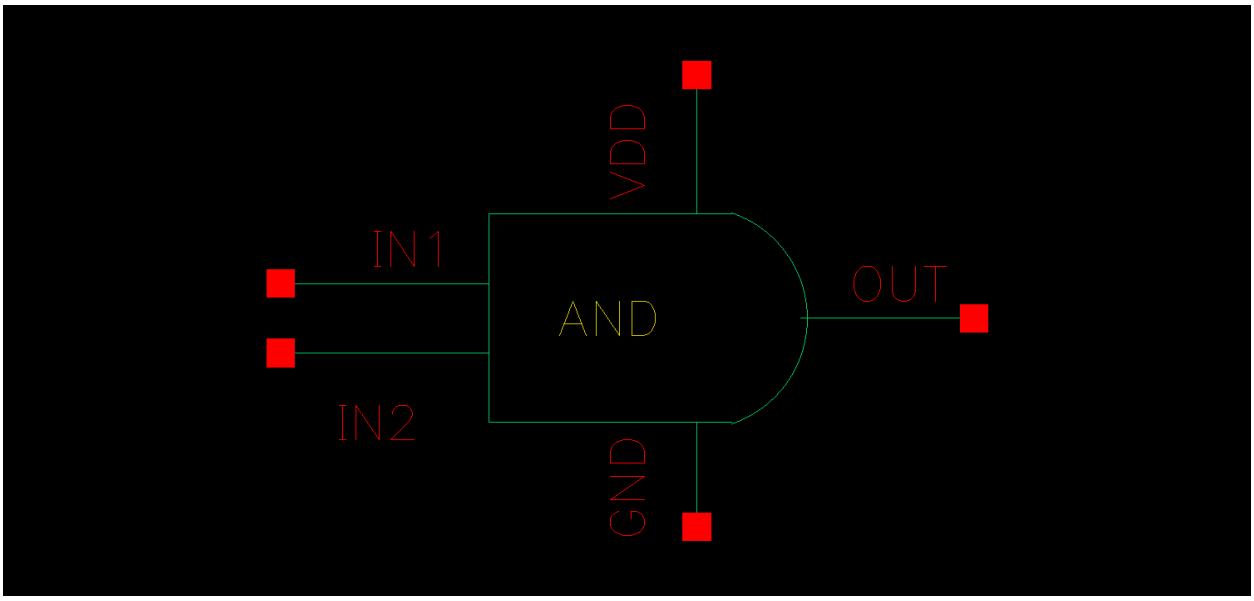
3.1. Schematic



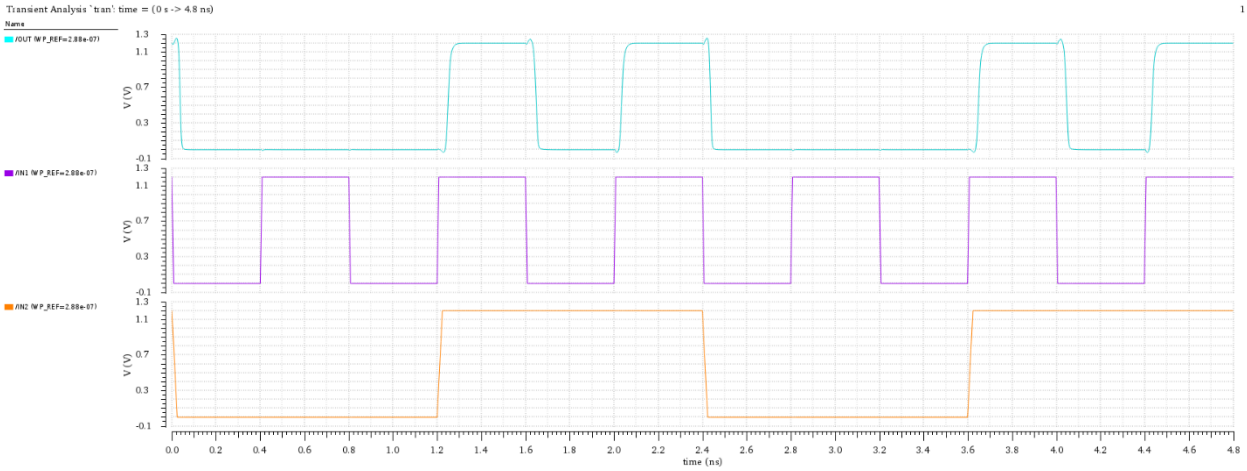
3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: IN0, IN1
- OUTPUT: OUT
- Input Parameter: WN_AND
- Sizes: WN_AND for the AND, while 1.4*WN_AND for the INV
- why 1.4? NAND should be lower, to avoid wasting extra power in charging and discharging its own capacitance.
- while assuming CL = 15*CREF(INV), g*f is approximately 4, g of NAND = 1.36 so, size of the AND = 0.8* AND_ref, since WN_AND_ref = 2*WN_INV therefore WN_INV = 1.4*WN_AND

3.3. Symbol



4. Simulation and Results



Note: the simulation result is performed with an input f = 1.25GHZ for IN1, while for IN2 = 1/3 * f