بسم الله الرحمن الرحيم

Project Title: Transistor-Level 4-BIT ALU Design

Module: 8-BIT REGISTER UNIT Design

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1. Abstraction

This report presents the design and implementation of an 8-bit register, a critical component in sequential digital systems. The register is used to store an 8-bit value synchronously with a clock signal and is implemented using eight cascaded D flip-flops at the transistor level using **MOSFET** technology, leveraging **130nm CMOS technology**. The circuit was meticulously developed and simulated using Cadence Virtuoso.

2. Logic Function and Truth Table

- Truth table(per bit)

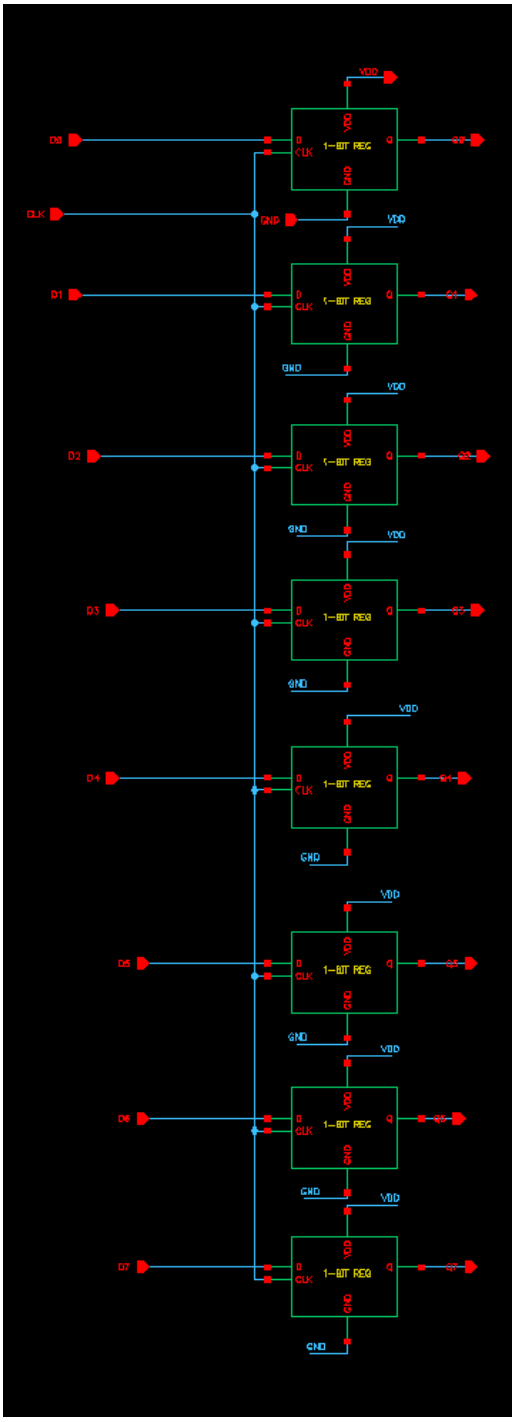
CLK ↑	Di	Qi (after edge)
Rising	0	0
Rising	1	1
No edge	X	Qi (unchanged)

- Logical Behavior
  At each CLK rising edge:

  Q[7:0] <= D[7:0].

3. Circuit Design

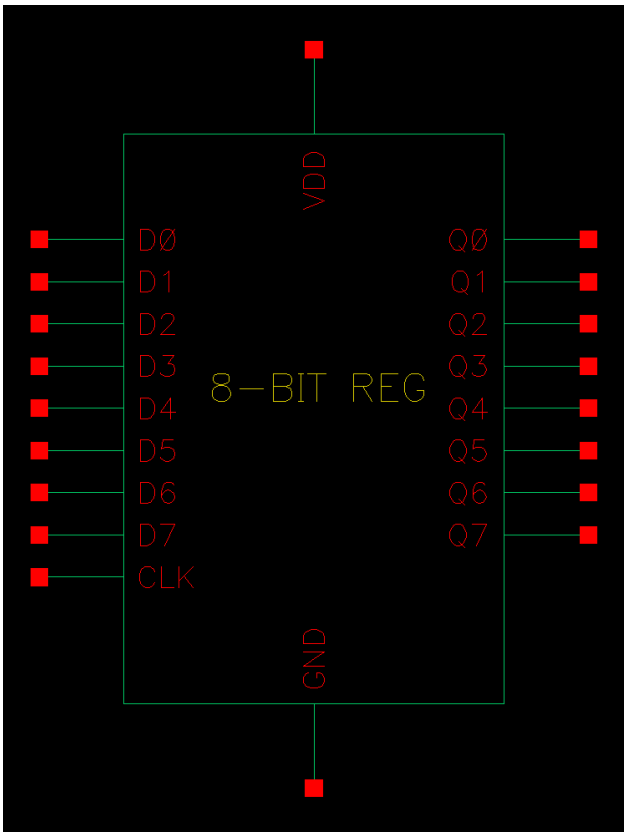
3.1. Schematic



3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, CLK
- OUTPUT: Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7
- Input Parameter: WN_REG
- Sizes: WN_REG

3.3. Symbol



4. Simulation and Results

- Timing parameters and waveforms will be the same as 1-bit register.