بسم الله الرحمن الرحيم

Project Title: Transistor-Level 4-BIT ALU Design

Module: 4-BIT FULL ADDER/SUBTRACTOR UNIT Design

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21 ذو القعدة، 1446

1. Abstraction

This report presents the design and implementation of a **4-bit Full Adder/Subtractor Unit** — a key sub-module in the ALU architecture, implemented at the transistor level using **130nm CMOS technology.** The design supports both addition and subtraction operations on 4-bit signed inputs (A and B), depending on a control signal (SEL). The implementation supports 2's. The circuit produces a **4-bit signed output**. The circuit was meticulously developed and simulated using Cadence Virtuoso.

2. Logic Function and Truth Table

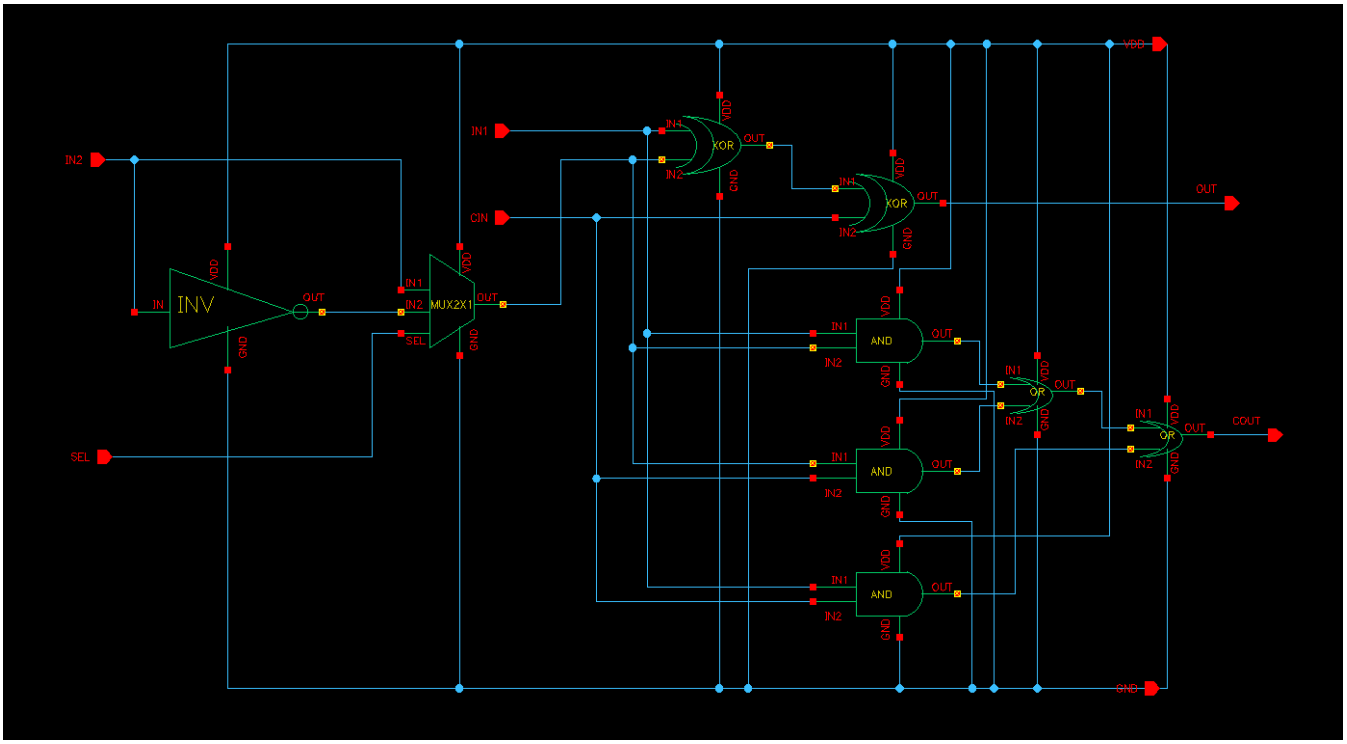
A (dec)	A (bin)	B (dec)	B (bin)	SEL	Op	OUT (bin)	OUT (dec)	OVF	COUT
3	0011	2	0010	0	3 + 2	0101	5	0	0
7	0111	1	0001	0	7 + 1	1000	-8	1	0
-3	1101	-4	1100	0	-3 + (-4)	1001	-7	0	1
-8	1000	-1	1111	0	-8 + (-1)	0111	7	1	1
5	0101	-2	1110	0	5 + (-2)	0011	3	0	1
4	0100	3	0011	1	4 - 3	0001	1	0	1
4	0100	7	0111	1	4 - 7	1101	-3	0	1
-7	1001	3	0011	1	-7 - 3	0110	6	1	1
-2	1110	-2	1110	1	-2 - (-2)	0000	0	0	1
7	0111	-8	1000	1	7 - (-8)	1111	-1	1	0

- COUT flag is only important for unsigned inputs. where the out has range: 0 : 15.
- OVF flag is only important for signed inputs. where the out has range: -8 : 7.

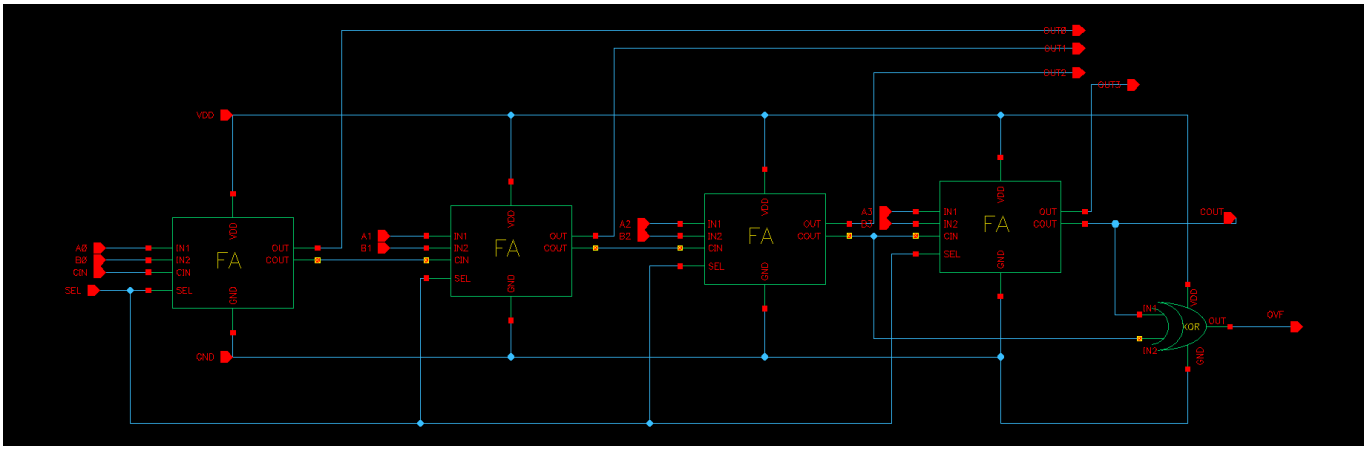
3. Circuit Design

3.1. Schematic

3.1.1. 1-BIT FA



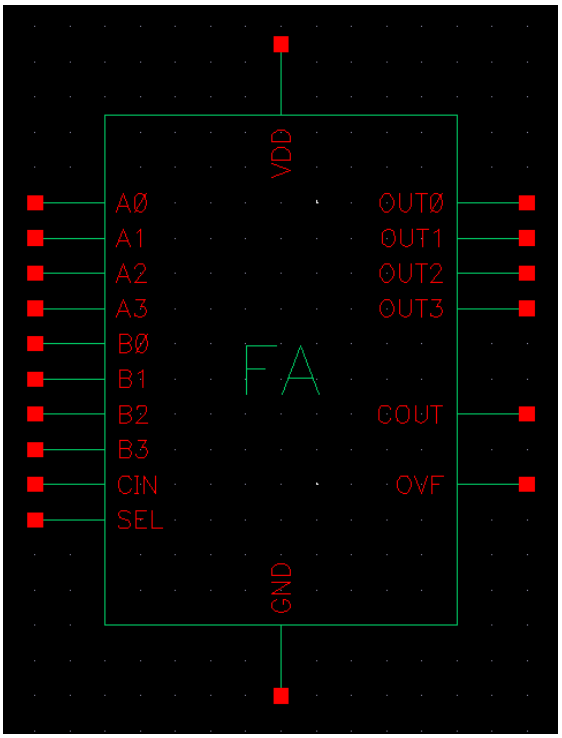
3.1.2. 4-BIT FA



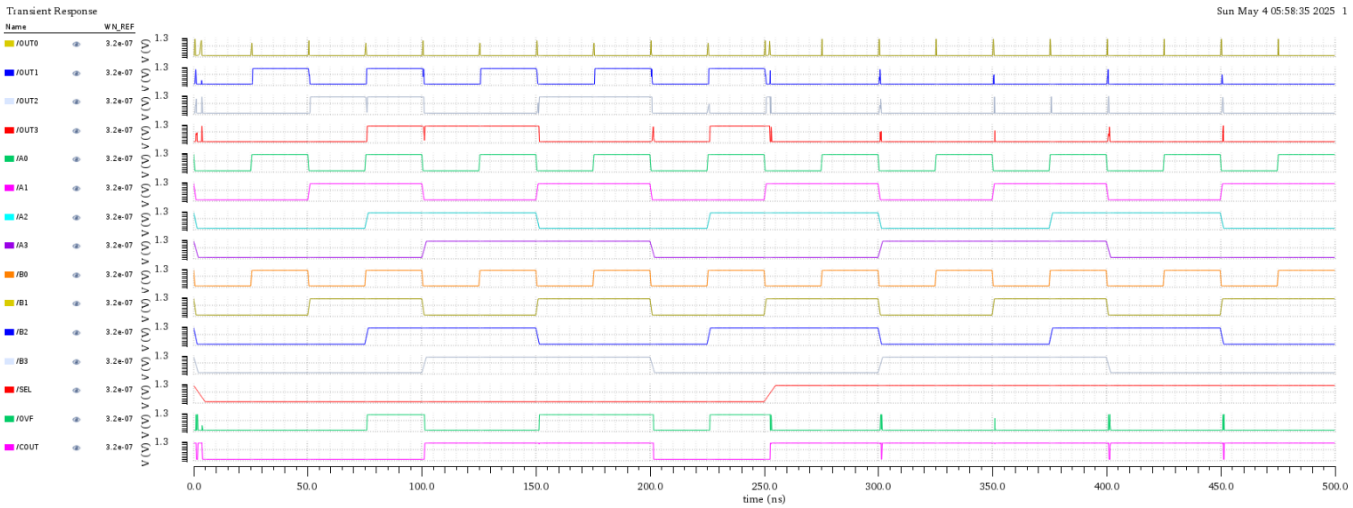
3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: 4-BIT IN0, 4-BIT IN1, 1 SEL, CIN
- OUTPUTS: 4-BIT OUT, 1-BIT OVF, 1-BIT COUT
- Input parameter: WN_FA
- Gates used: XOR, AND, INV, MUX-2X1, OR
- Sizes: 4*WN_FA, 1*, 1*, 2*, 1.7* followed by 5*
- why? : The sizes of the gates are approximated calculation based on the logical effort for each gate, not simulation results while assuming (CL = 15*CREF(INV))
- OVF: is for signed inputs, is designed using one XOR gate (CIN3 XOR COUT)
- The COUT flag: as OVF, but for un-signed inputs
- The design approach is as the following: for SEL and CIN = 0 and work as ADD, while for SEL and CIN = 1 work as SUB

3.3. Symbol



4. Simulation and Results



Note: the simulation result is performed with an input f = 20.0MHZ for A0, 1/2 *f A1, 1/3 * f for A2, 1/4 * f for A3. IN1(A3 A2 A1 A0), and the same for IN2