بسم الله الرحمن الرحيم

Project Title: Transistor-Level OR Gate Design

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MAY 14, 2025

1. Abstraction

This report presents the design and implementation of a OR gate at the transistor level, leveraging 130nm MOSFET technology. The circuit was meticulously developed and simulated using Cadence Virtuoso.

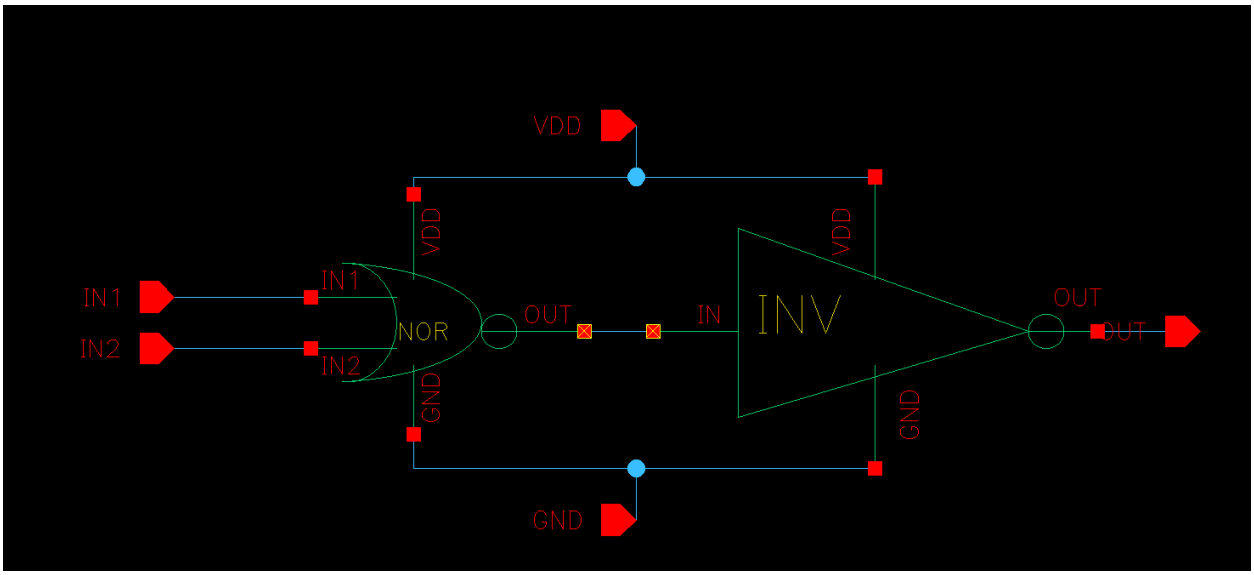
2. Logic Function and Truth Table

Y = (IN0 | IN1)

IN0	IN1	Y (IN0 OR IN1)
0	0	0
0	1	1
1	0	1
1	1	1

3. Circuit Design

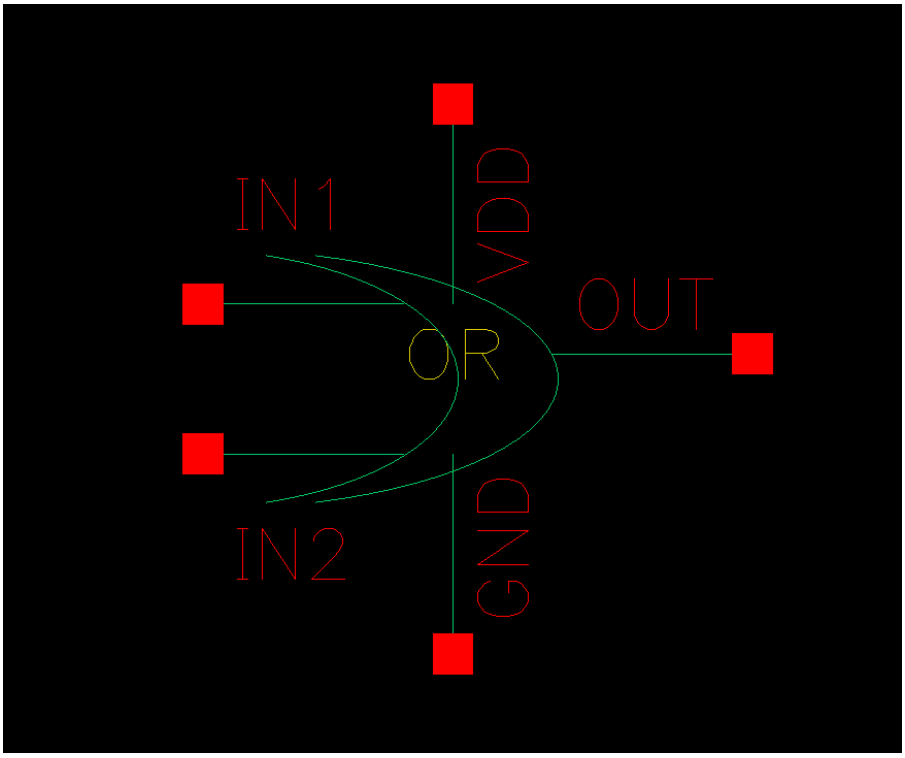
3.1. Schematic



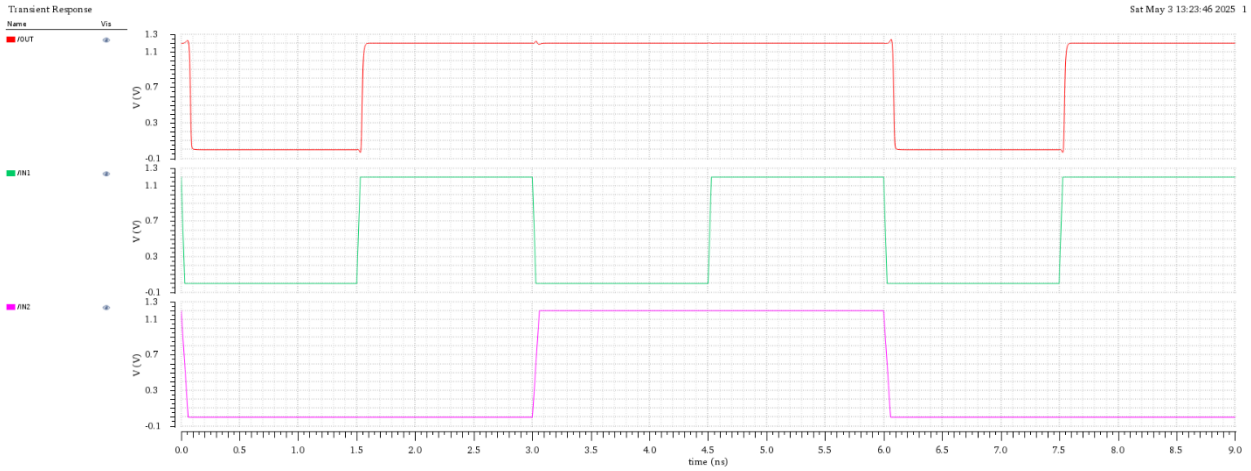
3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: IN0, IN1
- OUTPUT: OUT
- Input Parameter: WN_OR
- Sizes: the same as NOR, but for the INV: NMOS has 1.6*WN_OR, PMOS has 1.6*1.8*WN_OR
- why 1.6? NOR should be lower, to avoid wasting extra power in charging and discharging its own capacitance.
- while assuming CL = 15*CREF(INV), g*f is approximately 4, so size of the OR = 0.6 * OR_ref, since WN_OR_ref = WN_INV therefore WN_INV = 1.6*WN_OR.

3.3. Symbol



4. Simulation and Results



Note: the simulation result is performed with an input f = 1.0GHZ for IN1, while for IN2 1/3 * f