بسم الله الرحمن الرحيم

Project Title: Transistor-Level XNOR Gate Design

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17 ذو القعدة، 1446

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1. Abstraction

This report presents the design and implementation of a XNOR gate at the transistor level, leveraging 130nm MOSFET technology. The circuit was meticulously developed and simulated using Cadence Virtuoso.

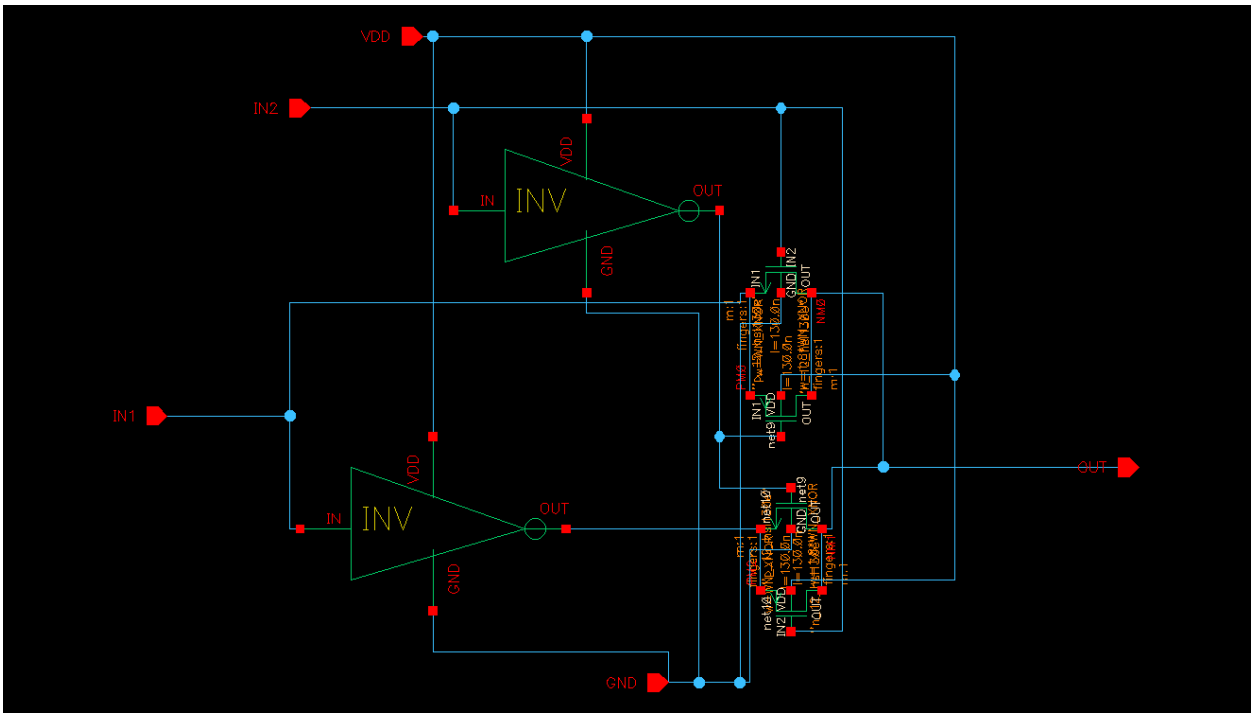
2. Logic Function and Truth Table

Y = ~(IN0 ^ IN1)

IN0	IN1	Y (IN0 XNOR IN1)
0	0	1
0	1	0
1	0	0
1	1	1

3. Circuit Design

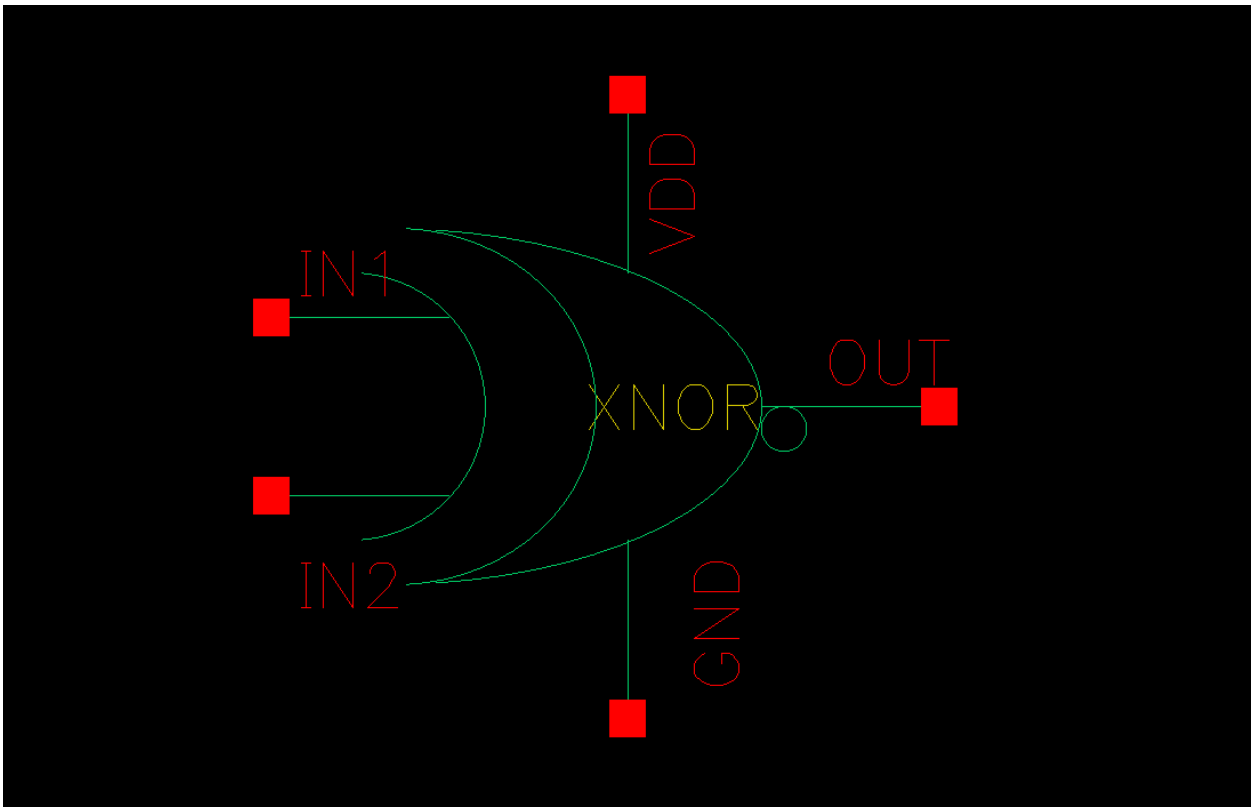
3.1. Schematic



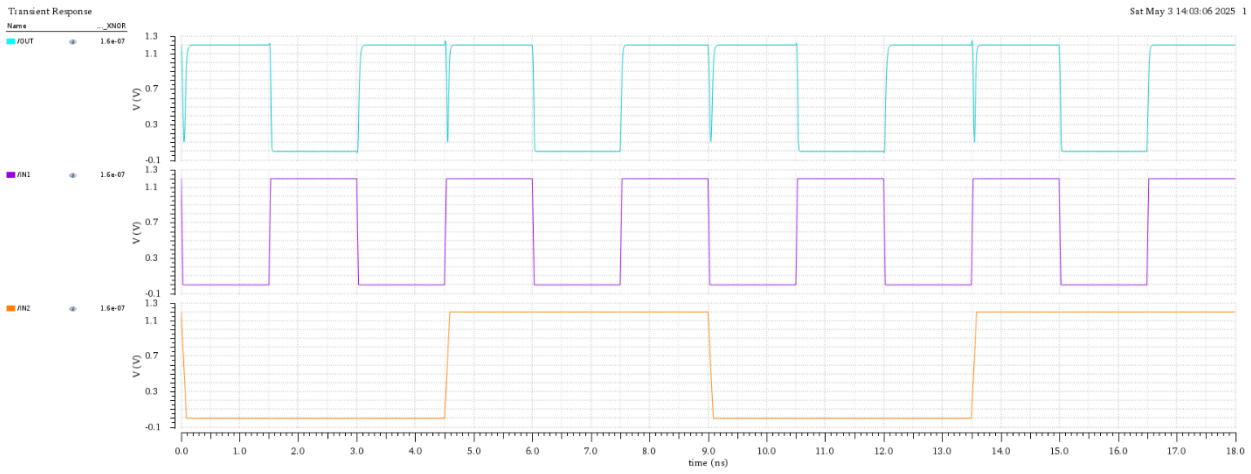
3.2. Design Approach

- 130nm CMOS process
- 1.2V VDD
- INPUTS: IN0, IN1
- OUTPUT: OUT
- Input Parameter: WN_XNOR
- It is designed using TGL and CMOS INV
- Sizes : INV: 5*WN_XNOR, TGL : WN_XNOR
- why? the INV should be stronger than the XNOR, why exactly 5? to be stronger and not to be too large, but this is only by intuition(not a simulation result)

3.3. Symbol



4. Simulation and Results



Note: the simulation result is performed with an input f = 333.3MHZ for IN1, while for IN2 1/3 * f