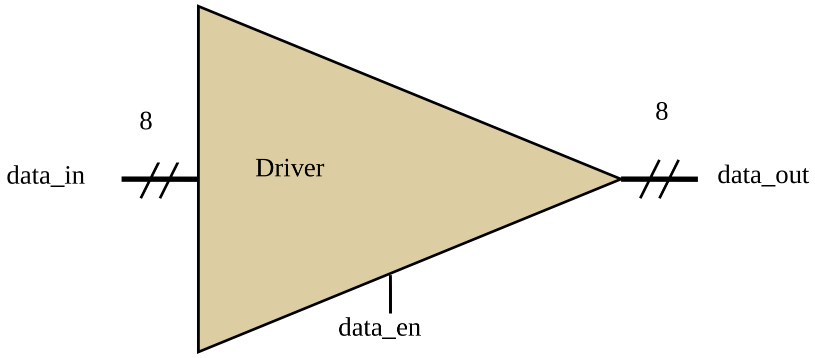
Module 4: Choosing Between Verilog Data Types

Lab 4-1 Modeling a Data Driver

Objective: To use a Verilog literal value to describe a parameterized-width bus driver.

The driver output is equal to the input value when enabled (*data_en* is true) and is high-impedance when not enabled (*data_en* is false).

In this lab, you create a data driver as per the specification and verify it using the provided testbench. Please make sure to use the same variable name as the ones shown in block diagrams.



Specifications

- `data_in` and `data_out` are both parameterized widths of 8-bit.
- If `data_en` is high, the input `data_in` is passed to the output `data_out`.
- Otherwise, `data_out` is high impedance.

Designing a Data Driver

1. Change to the *lab5-drvr* directory and examine the following files.

driver_test.v	Driver test

2. Create the *driver.v* file, and using your favorite editor, describe the driver module named “*driver*”.

3. Parameterize the driver input and output width and assign a default value of 8.

Verifying the Driver Design

1. Using the provided testbench module, check your driver design using the following command with VCS.

   ```
   vcs driver.v driver_test.v (Batch Mode)
   ```

   or

   ```
   vcs driver.v driver_test.v -gui -access +rwc ( GUI Mode)
   ```

2. You might find it easier to list all the files and simulation options in a text file and pass the file into the simulator using the `−f vcs` option.

   ```
    vcs-f filelist.txt -access rwc
   ```

   You should see the following results.

   ```
   At time 1 data_en=0 data_in=xxxxxxxx data_out=zzzzzzzz
   At time 2 data_en=1 data_in=01010101 data_out=01010101
   At time 3 data_en=1 data_in=10101010 data_out=10101010
   TEST PASSED
   ```

3. Correct your driver design as needed.