MSCS 1st Final Exam

Enter Your name *

Ahmed Bilal

Enter Your Ag Number *

2016-ag-7891

Final Term

Multiprocessors are classified as _____.

- [ ] SIMD
- [x] MIMD
- [ ] SISD
- [ ] MISD

Full-form of VLSI?

- [x] Very large scale integration
- [ ] Very least scale instructions
- [ ] Variety of large & small instructions
- [ ] Very long scalable integration

Which one is not benefit of multiprocessors?

- ○ Multiple independent jobs can be made to operate in parallel
- ○ A single job can be partitioned into multiple parallel tasks
- ◉ Multiple jobs can be made to operate in serial
- ○ All are benefits

What is another name of tightly coupled multiprocessor?

- ○ Distributed memory processors
- ○ Mutually coupled processors
- ○ Binding memory processors
- ◉ Shared memory processors

Which of the following is not one of the interconnection structures?

- ○ Crossbar switch
- ○ Hypercube system
- ◉ Single port memory
- ○ Time-shared common bus

In time-shared common bus, when one processor is communicating with the memory, what all other processors do?

- ○ busy with internal operations
- ○ must be idle waiting for the bus
- ○ interrupt the working processor
- ◉ either A or B

Full-form of MM in multiport memory & crossbar switch?

- ◉ Memory module
- ○ Multiport module
- ○ Multiport memory
- ○ Main Memory

A processor does not require _____ bus to communicate with memory.

- ○ address
- ◉ interrupt
- ○ data
- ○ control

What is the advantage of multiport memory organization?

- ○ Simple construction
- ○ Less hardware needed
- ◉ High transfer rate
- ○ None of above

How many buses/cables are required to establish multiport memory organization between 7 CPUs & 5 MMs?

- ○ 20
- ○ 35
- ○ 40
- ◉ 42

The protocols for maintaining coherence of multiple processors are known as?

- ○ Data coherence protocols
- ○ Commit coherence protocols
- ○ Recurrence
- ◉ Cache coherence protocols

From inter-processor communication, the misses arises are often called?

- (●) Coherence misses
- ( ) Commit misses
- ( ) Parallel processing
- ( ) Hit rate

Symmetric multiprocessors architectures, are sometimes known as?

- ( ) Static memory access
- (●) Uniform memory access
- ( ) Variable memory access
- ( ) All Above

Two-way set associative having a 64-byte block, the single clock-cycle hit time is a?

- (●) Level 1 instruction cache
- ( ) Level 1 data cache
- ( ) Level 2 data cache
- ( ) Level 2 instruction cache

The tightly coupled set of threads' execution working on a single task, that is called?

- (●) Multithreading
- ( ) Recurrence
- ( ) Parallel processing
- ( ) Serial processing

The alternative design technique consists of multiprocessors having physically distributed memory, called?

- ( ) Warehouse-scale
- ( ) Static memory access
- (●) Distributed shared memory
- ( ) Shared memory

Microprocessors which are directly connected memory to a single-chip, that is sometimes called as?

- ( ) Backside
- ( ) Memory bus
- ( ) Kernel
- (●) both a and b

The node which has the memory location and the entry of directory of an address is?

- (●) Home node
- ( ) Guest node
- ( ) Host node
- ( ) All above

When every cache hierarchy level is a subset of level which is further away from the processor, is referred to as?

- ( ) Synchronization
- ( ) Atomic synchronization
- (●) Multilevel inclusion
- ( ) Distributors

Interconnection network are also called?

- ( ) Communication subnet
- ( ) Communication subsystems
- ( ) Cellular telecommunication
- (●) Bath a & b

Private data that is used by single processor, then shared data are used by ?

- (●) Single processor
- ( ) Multi processor
- ( ) Single tasking
- ( ) Multi tasking

In the coherent multiprocessor, cache that is present provide both the migration and ...?

- ( ) Coherence
- ( ) Recurrence
- (●) Replication
- ( ) Uniformity

The Particular block statuses of physical memory are normally kept in one location called ?

- ( ) Register
- (●) Directory
- ( ) Stack
- ( ) Queue

What is the full form of RISC?

- ○ Read Instruction Set Architecture
- ◉ Reduced Instruction Set Computer
- ○ Register Instruction Set Computer
- ○ None of the above

Which Processors includes multi-clocks?

- ◉ Complex Instruction Set Computer
- ○ Reduced Instruction Set Computer
- ○ ISA
- ○ ANNA

Which Processors Data transfer Register to register?

- ○ Complex Instruction Set Computer
- ◉ Reduced Instruction Set Computer
- ○ ISA
- ○ ANNA

Which of the following is true?

- ○ The RISC processor has a more complicated design than CISC.
- ◉ Risc Focus on software
- ○ Cisc Focus on software
- ○ Risc has Variable sized instructions

Which processor requires more number of registers?

- ○ CISC
- ○ ISA
- ◉ RISC
- ○ ANNA

Both the CISC and RISC architectures have been developed to reduce the _____?

- ◉ Semantic gap
- ○ Time Delay
- ○ Cost
- ○ Reduced Code

Which of the following is true about CISC processor?

- ○ Micro programmed control unit is found in CISC.
- ○ Data transfer is from memory to memory.
- ○ In this instructions are not register based.
- ◉ All of above

Out of the following which is not a CISC machine.

- ○ IBM 370/168
- ◉ Motorola A567
- ○ Intel 80486
- ○ VAX 11/780

The iconic feature of the RISC machine among the following is _____?

- ○ Reduced number of addressing modes
- ○ Increased memory size
- ◉ Having a branch delay slot
- ○ None of these

A register is defined as ____?

- ○ The group of latches for storing one bit of information
- ○ The group of flip-flops suitable for storing one bit of information
- ○ The group of latches for storing n-bit of information
- ◉ The group of flip-flops suitable for storing binary information

The register is a type of ____?

- ◉ Sequential circuit
- ○ Combinational circuit
- ○ CPU
- ○ Latches

How many types of registers are?

- ○ 2
- ○ 3
- ◉ 4
- ○ 5

In D register, ‘D’ stands for __?

- ○ Delay
- ○ Decrement
- ◉ Data
- ○ Decay