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The I2S Audio Interface provides a bidirectional, synchronous, serial interface to off-chip audio devices. It complies with the Inter-IC Sound (I2S) bus specification from Philips Semiconductor (*I2S bus specification*; February 1986, revised June 5, 1996) and is the same I2S Audio Interface IP proven in high-volume devices from National Semiconductor.

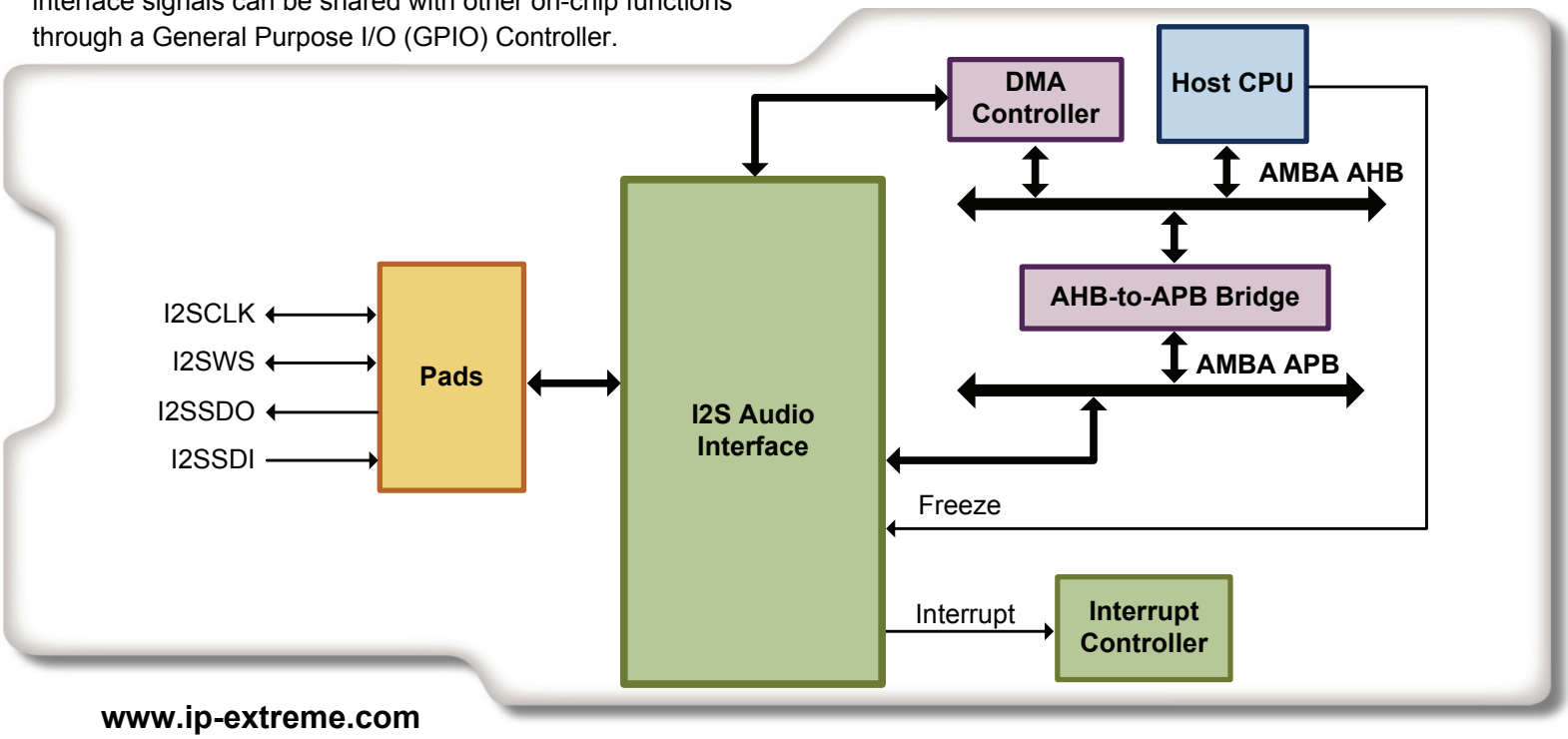
The host interface of the I2S Audio Interface complies with the AMBA 2.0 APB protocol. Control registers provide CPU control of master or slave mode, audio data format, data word length, bit clock generation, word select signal resolution, FIFO threshold levels, and enabling/disabling interrupts. Status registers provide interrupt and FIFO status.

Transfer of audio data to/from the host system can be either interrupt-driven or through DMA to reduce CPU utilization. In both cases, four 8-word-deep FIFOs with programmable threshold levels provide storage of transmit/receive data for the left and right channels. APB-accessible registers provide read or write access to each of the four FIFOs.

The I2S bus interface of the I2S Audio Interface is a set of unidirectional signals that connect to chip I/O pads to form the off-chip I2S bus signals: serial clock (I2SCLK), word select (I2SWS), serial data in (I2SSDI), and serial data out (I2SSDO). To reduce chip-level pin count, the I2S bus interface signals can be shared with other on-chip functions through a General Purpose I/O (GPIO) Controller.

FEATURES

- Can operate as master or slave in several configurations
  - Master or slave mode as transmitter
  - Master or slave mode as receiver
  - Master or slave mode as transmitter and receiver
  - Master mode as controller (does not transmit or receive data)
- Bidirectional operation through two unidirectional serial data lines
- Supports audio data widths from 8 to 24 bits
- Supports multiple audio data formats
  - I2S format
  - Left Justified
  - Right Justified
- Programmable word select resolution (8–32 clock cycles) in master mode
- Four reference clock sources selectable for bit clock generation with programmable clock divider
- Interrupt-driven or DMA operation
- Four 8-word FIFOs (left/right; transmit/receive)
- Programmable FIFO threshold levels for interrupt or DMA request generation



FEATURES (CONTINUED)

- Additional interrupts for transmit FIFO underrun and receive FIFO overrun with separate enables
- Freeze/suspend operation for system debug support
- Local clock gating for minimal power consumption

ABOUT THE I2S BUS

The I2S bus is a popular serial bus for interfacing to audio chips such as codecs. I2S is a simple data interface, without any form of address or device selection. On an I2S bus, there is only one bus master and one transmitter. The master may be a transmitter, a receiver, or a controller for data transfers between other devices acting as transmitter and receiver. In high-quality audio applications involving a codec, the codec is typically the master so that it has precise control over the I2S bus clock.

The I2S bus carries two channels, left and right, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by a word select signal driven by the bus master.

The I2S Audio Interface from IPextreme directly supports two-channel audio applications. In addition, multiple instances of the I2S Audio Interface can combined to support multi-channel audio applications such as surround sound.

INTERFACES

- AMBA 2.0 APB host interface
  - 32-bit read/write data buses
  - 10-bit address bus
- I2S bus interface pins (I2SCLK, I2SWS, I2SSDO, I2SSDI) through chip I/O pads (optionally through a GPIO Controller)
- DMA interface
  - Two transmit DMA channels (left and right)
  - Two receive DMA channels (left and right)
- Clock interface
  - APB clock for registers, FIFOs, DMA, and interrupt functions, and (optionally) for bit clock generation in master mode
  - Three auxiliary clock reference inputs for bit clock generation in master mode
  - Bit clock input for slave mode
- Interrupt interface (one interrupt signal)
- One asynchronous reset input
- Freeze/suspend interface
- DFT signals

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 13,700 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The I2S Audio Interface is available in Source and Encrypted products. The Source product is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools

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