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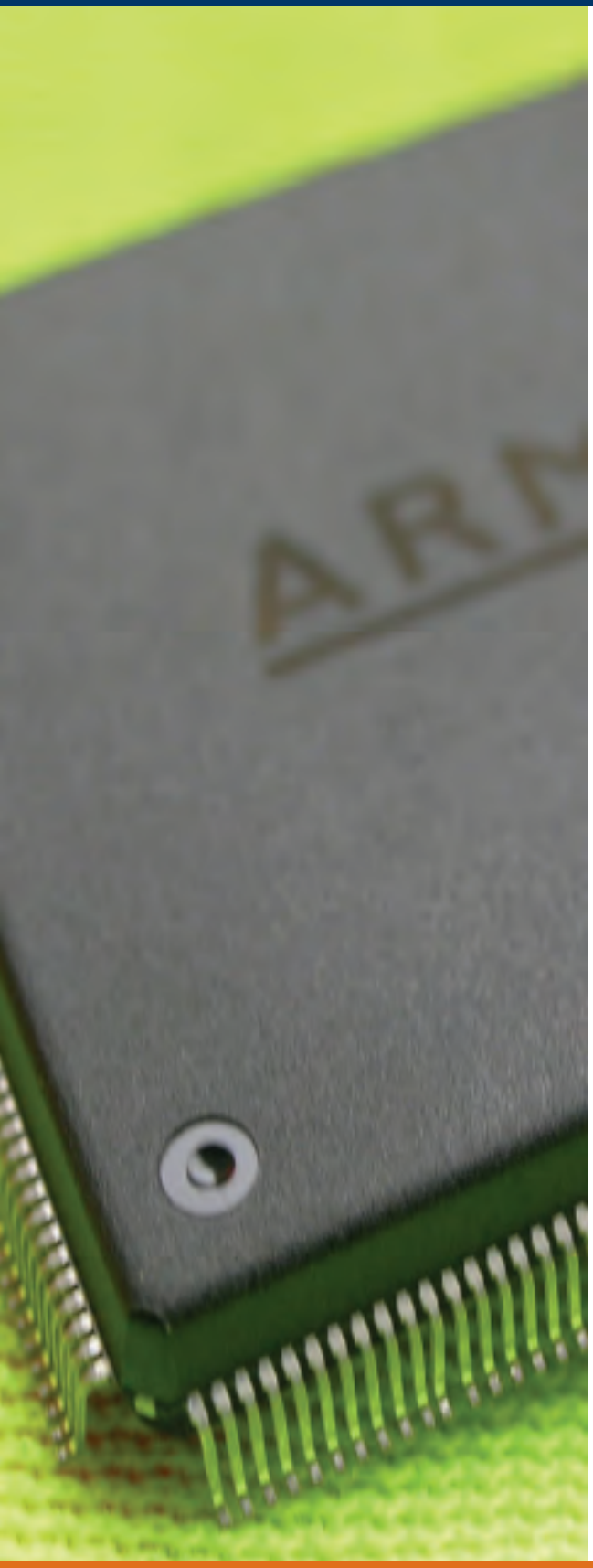
ARM CORTEX™-M3 PROCESSOR



The ARM® Cortex™-M3 processor has been specifically designed to deliver outstanding performance in cost and power sensitive applications, ranging from complex SoC to low-end microcontrollers.

Based on the ARMv7M architecture the Cortex-M3 processor is a highly configurable and fully synthesisable processor that includes an efficient Harvard 3-stage pipeline core that delivers more than 1.25 DMIPS/MHz. The core achieves an outstanding power efficiency of 0.047mW/MHz and the standard processor implementation, which includes 32 physical interrupts, achieves 0.06 mW/MHz (0.13µm Metro™ @ 50MHz).

To enable the design of cost sensitive devices the Cortex-M3 processor implements tightly coupled system components that reduce processor area and integration issues while significantly improving interrupt handling capabilities and system debug. Futhermore the central core is up to 30% smaller than existing 3-stage cores, providing additional cost reduction. The Cortex-M3 processor implements the Thumb®-2 ISA to ensure high code density and lower memory requirements. Thumb-2 also provides the exceptional performance expected of a modern 32-bit architecture, while supporting traditional Thumb code.

Key Benefits

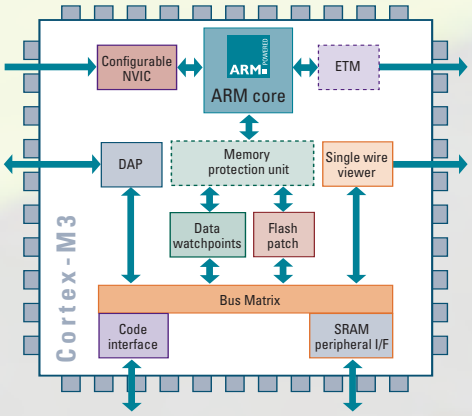
The ARM Cortex-M3 processor offers significant benefits to system and software developers.

- Lower cost devices through smaller processing core, system and memories
- Ultra low power consumption and integrated sleep modes
- Outstanding processing performance for challenging applications
- Fast interrupt handling for critical control applications
- Platform security with optional integrated memory protection unit
- Enhanced system debug for faster development
- No assembler code requirement to ease system development
- Wide application envelope encompassing ultra-low cost microcontrollers and high performance SoC.

Cortex-M3 Performance Estimates: 0.13µm ARM Metro

	Performance	Frequency (Worst case maximum)	Area (50MHz nominal)	Power Consumption (50MHz nominal)
Central Core (Equivalent to ARM7TDMI-S™)	1.25 DMIPS/MHz	135MHz Metro (150MHz Sage-X)	0.166mm²	0.047mW/MHz
Processor (Includes central core, NVIC, bus matrix and debug)	1.25 DMIPS/MHz	135MHz Metro (170MHz Sage-X)	0.302mm²	0.059mW/MHz

All data is based on pre-layout netlists. Please contact ARM for current specifications



ARM Cortex-M3 Processor Overview

The ARM Cortex-M3 processor integrates multiple system peripherals with a high-performance core to deliver unrivalled benefits in both cost sensitive and performance focused applications. The processor is fully synthesisable and is highly customizable, enabling a wide range of physical interrupts and debug architectures to be implemented. Additionally the Cortex-M3 processor enables the optional integration of a fine-granularity Memory Protection Unit (MPU) and an Embedded Trace Macrocell™ (ETM™)

ARM Cortex-M3 Core

The ARM Cortex-M3 processor is built on a high performance 3-stage pipeline Harvard architecture core, making it ideal for demanding event driven applications.

Exceptional power efficiency is delivered through extensive clock gating plus technology that improves performance per cycle including single-cycle 32x32 multiplication and hardware division.

Additionally the core has significantly reduced physical area through the implementation of a stack-based exception model.

The Cortex-M3 processor implements the Thumb-2 instruction set, a super-set of traditional Thumb instructions, which delivers both the performance of traditional 32-bit code and the high code density of 16-bit

Nested Vectored Interrupt Controller (NVIC)

The Cortex-M3 processor closely integrates the core with a configurable interrupt controller to deliver industry-leading interrupt processing performance. In its standard implementation the NVIC supplies a Non-Maskable Interrupt (NMI) plus 32 general purpose physical interrupts with 8 levels of pre-emption priority, however through simple synthesis choices the controller can be configured down to a single physical interrupt or up to 244. Additionally the number of levels of pre-emptive priority can be configured at synthesis up to 255.

The tight integration with the processing core enables far faster execution of Interrupt Service Routines (ISR), reducing the number of cycles typically taken to enter an interrupt by up to 70%. This is accomplished through the use of hardware stacking of registers, plus the ability to exit and restart load-store multiple executions. This implementation also means that no assembler stubs are required to handle the movement of registers, vastly simplifying code.

Moving between active and pending interrupts has also been significantly simplified through the use of Tail-Chaining technology which replaces serial stack Pop & Push actions that normally take over 30 clock cycles with a simple 6 cycle instruction fetch.

To enhance low power designs the NVIC integrates three sleep modes, including a Deep Sleep function that may be exported to other system components to enable the entire device to be rapidly powered down.

Interconnect Matrix

The ARM Cortex-M3 processor integrates an AMBA® AHB-Lite™ interconnect to support the system peripherals and reduce system integration complexity. The Bus Matrix delivers support for unaligned data accesses ensuring data is tightly packed into memory, significantly lowering SRAM requirements and system cost.

Additionally the Cortex-M3 Bus Matrix implements atomic bit manipulation that enables system spin-locks and ensures the safe use of single-bit data representation in heavily interrupt drive applications.

Integrated Debug

The ARM Cortex-M3 processor implements a complete hardware debug solution enabling high system visibility of the processor through a traditional JTAG port or the 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

For system trace the processor integrates an optional ETM alongside data watch points that can be configured to trigger on specific system events. To enable simple and cost effective profiling of these system events a Serial Wire Viewer (SWV) can export streams of standard ACSII data through a single pin.

Flash Patch technology offers device and system developers the ability to patch errors in code from ROM to SRAM or Flash during both debug and run-time, potentially eliminating the need for costly respins.

Optional Components

The ARM Cortex-M3 processor has two optional components:

Memory Protection Unit (MPU) — The fine grain MPU design enables applications to implement security privilege levels, separating code, data and stack on a task-by-task basis. Such requirements are becoming critical in many embedded applications such as automotive.

ETM —The Cortex-M3 ETM delivers unrivalled instruction trace capture in an area far smaller than traditional trace units enabling many low cost devices, such as MCUs, to implement it for the first time.

Cortex-M3 Processor Applications

The features of the Cortex-M3 processor make it ideal for a wide range of applications, including:

- Cost Sensitive Devices — Generic MCUs, Smart Toys, Personal Electronics
- Low Power Devices — ZigBee, PAN (Bluetooth), Medical Electronics
- High Performance Devices — Ultra Low Cost Handsets, Automotive Systems, Mass Storage

Cortex-M3 Processor in Cost Sensitive Devices

- Small core reduces silicon area
- Tight integration of system peripherals reduces area and development costs
- Thumb-2 code reduces instruction memory by up to 30%
- SWD enables smaller pin packages
- No need for assembler code in ISRs and Boot routines
- Single cycle Read/Modify/Write enables tighter data packing
- Deterministic interrupt handling
- Patching ability of ROM to Flash or SRAM for system updates

Cortex-M3 Processor in Low Power Devices

- Low power core — 0.047mW/MHz (0.13µm — ARM Metro Libraries 50MHz)
- Advanced clock gating drives down power consumption
- Integrated sleep modes
- Power control of system components
- High efficiency enables slower clocking
- Fast task execution increases time asleep and reduces aggregate power consumption

Cortex-M3 Processor in High Performance Devices

- Performance — 1.25DMIPS/MHz
- 70% more efficient than ARM7™ family processor executing Thumb
- 35% more efficient than ARM7 family processor executing ARM
- Hardware division enables better algorithm implementation
- Fast interrupt handling for critical events
- Optional MPU for critical applications
- Extensive Debug & Trace capabilities

Cost Sensitive Devices	Lower Power Devices	High Performance Devices
30+ DMIPS < $1	25 DMIPS < 1mW[1]	120 DMIPS < 100MHz
32-Bit MCUs at 16-Bit prices	Extended battery life	Higher Efficiency Processor
Minimal packaging < 20 pins	Integrated sleep modes	Lower clock speeds
Low-cost tools	System peripherals control	Deterministic interrupt handling

(1) Based on 0.13um process and ARM Metro Library

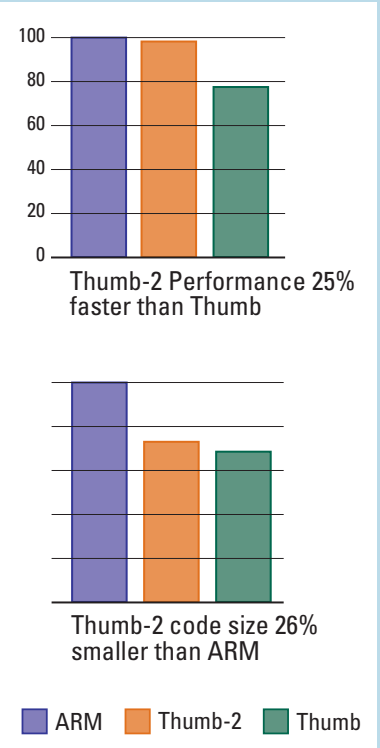
Thumb-2 instruction Set

Thumb-2 combines the functionality of 32-Bit instructions with the code density, and smaller memory requirements, of traditional 16-Bit instructions to provide code that delivers optimal performance and size for any application without the need for complex interworking.

Through the use of Thumb-2 developers can choose to maintain their current performance and reduce memory sizes, and hence system costs, or alternatively they may chose to keep their current memory sizes and enjoy increased performance.

Thumb-2 builds on the traditional 16-Bit Thumb instruction set, and is fully backward compatible ensuring that the majority of assembler code can be easily migrated. Additionally, due to the underlying ARM Unified Assembler framework, 32-Bit ARM assembly can be seamlessly ported to Thumb-2.

Thumb-2 is an ideal target for C code, and a simple recompile will ensure optimal execution.



Thumb-2 requires 26% less memory that ARM and provides 25% higher performance than Thumb — reducing system costs without sacrificing performance

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RealView® Tools Support

ARM RealView Tool Support

RealView® tools and models by ARM are unique in their ability to provide solutions that span the complete development process from concept to final product deployment. Each member of the RealView tools series has been developed closely alongside the ARM processor IP ensuring that it maximizes the IP's performance. No other supplier can offer this unique end-to-end toolchain support for ARM IP, from system and processor design through to software development.

The RealView series development tools consist of:

- The RealView DEVELOP family of embedded software tools
- The RealView CREATE family of Electronic System Level (ESL) tools

RealView Microcontroller Development Kit

RealView Microcontroller Development Kit for ARM Powered™ devices features the RealView Compilation Tools together with the Keil µVision® development environment. This kit provides developers with a feature-rich, integrated development environment, specifically optimized for a wide range of ARM processor-based microcontrollers (MCUs) and new devices based on the ARM Cortex-M3 processor.

This kit is perfect for the developer requiring the advantages of industry standard RealView compilation tools and sophisticated debugging support via the industry's leading microcontroller development environment.

Unique features include:

- Seamless environment for project management, debugging and simulation
- Accurate Device Simulation (CPU and Peripherals)
- Comprehensive device support in the integrated Device Database®
- Configuration support for leading microcontrollers with complete simulation of target hardware.
- Advanced software logic analyzer and software trace tools enabling execution profiling and performance analysis.

Optional hardware products:

- ULINK USB-JTAG Adapter
- Evaluation Boards

RealView® Tools by ARM®

ARM Artisan® Physical IP

ARM's Artisan Physical IP products are designed to achieve the best combination of performance, density, power and yield for a given manufacturing process. The products are available for 90- through 250-nanometer processes and delivered with an extensive set of views and models supporting industry leading EDA tools. ARM Artisan IP platforms and product portfolios offer a wide range of choices to meet system-on-chip (SoC) designers' nanometer requirements.

Artisan Metro™ Low Power Platform

ARM's Artisan Metro low-power platform is based on a series of new architectures that dramatically reduce power while enhancing density and yield: eighty-percent lower power, a twenty-percent reduction in area and improved production yield.

Metro IP takes advantage of new process, circuit design, voltage scaling, power-aware EDA and chip-level design techniques to deliver a solution that enables designers to meet the growing demand for performance-oriented, low-power ICs.

The Metro product portfolio includes memory generators, standard cell libraries, general-purpose and specialty I/O cells and analog and mixed-signal IP. The IP conforms to the Artisan design standard, which thousands of IC designers have come to rely on for their advanced system-on-chip (SoC) development.

Artisan® ARM® Physical IP