Lab 05

RTL Design of an Elevator Controller

# Purpose

* The objectives of this lab are:
  + RTL implementation of an elevator controller
  + Validation of the design using self-checking testbenches and simulation

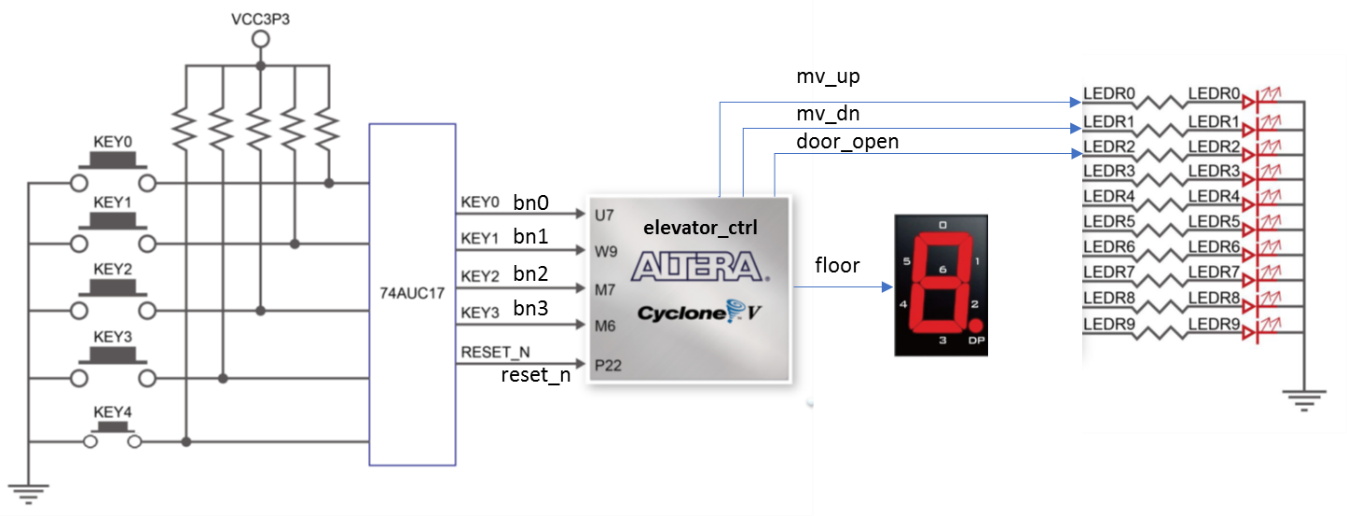
# Required tools

Notepad++ (source code editing)

ModelSim PE student editions (simulation)

# Design specification

Move the elevator either up or down to reach the requested floor. Once at the requested floor, open the door for at least 2 seconds. Ensure the door is never open while moving. Don’t change directions unless there are no higher requests when moving up or no lower requests when moving down. Assume that the elevator moves from one floor to another in 2 seconds. The controller should use the 50 MHz clock on DE1-CV board. Use a 1 sec clock enable to the timer for the elevator movement and the opening of the door. The inputs and outputs of the controller are shown in the figure below. Also, the controller can be broken into a Request Resolver that resolves various floor requests into single requested floor and a Unit Control that moves elevator to this requested floor. Design the controller to serve up to 10 floors (0 is the ground floor and 9 is the highest floor). Use VHDL generics for the number of floors. The floor output should be connected to a seven segment display through a binary to SSD converter (from HW1). All control signals and status signals will be connected to push button switches and LEDS.



## Submission

1. A design document showing the state diagram of the finite state machine of the elevator controller (elevator\_ctrl\_fsm.docx)
2. RTL files
   1. Seven segment interface (from lab 1) ssd.vhd
   2. The RTL implementation of the controller, elevator\_ctrl.vhd.
3. Create at testbench to verify the functionality of elevator\_ctrl.vhd. Name this testbench elevator\_ctrl\_tb.vhd. Make sure your testbench verifies multiple simultaneous floor requests.