

Ahmed Fathy

Computer Engineer – FPGA & Embedded Systems

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EDUCATION

- Cairo University, Faculty of Engineering
B.Sc. in Computer Engineering; GPA: 3.6

Giza, Egypt
2023 – 2027

EXPERIENCE

- Al Nada Scientific Office | *Technical Support Trainee* Cairo, Egypt | June 2022 – 2024
 - **Diagnostics & Maintenance:** Troubleshoot workstations and network equipment; performed firmware updates and preventive maintenance.
 - **Documentation:** Created systematic troubleshooting documentation to streamline hardware issue resolution.

HARDWARE & EMBEDDED PROJECTS

- 5-Stage Pipelined Processor (RISC) | *VHDL, QuestaSim, Computer Architecture* Source Code | 2025
 - **Core Architecture:** Engineered a **32-bit 5-stage pipelined processor** in VHDL, supporting a custom ISA of over 25 instructions.
 - **Hazard Resolution:** Optimized throughput by implementing Hazard Detection and Data Forwarding units to resolve control and data dependencies.
 - **Verification:** Validated functional correctness through rigorous simulation and testbench environments in **QuestaSim**.
- CNN Convolution Accelerator | *Verilog, OpenLane2, ASIC Design* Source Code | 2025
 - **Architecture:** Designed a synthesizable **2D convolution accelerator** using **Systolic Arrays** and fully pipelined dataflow to maximize MAC throughput.
 - **Memory Hierarchy:** Implemented DMA-based loading and dual-port SRAM buffering to support up to **16x16 kernel** execution.
 - **Physical Design:** Executed RTL-to-GDSII synthesis using **OpenLane2**, validating physical feasibility and achieving timing closure.
- AES Encryption/Decryption Engine | *Verilog, FPGA, Cryptograph* Source Code | 2023
 - **Core Logic:** Synthesized robust AES cryptographic core in Verilog HDL supporting **128-bit, 192-bit, and 256-bit** key standards.
 - **Datapath:** Engineered hardware-optimized modules for SubBytes, ShiftRows, MixColumns, and AddRoundKey transformations.
 - **Validation:** Verified cryptographic correctness against standard NIST test vectors using rigorous debug tracing.
- Tactic (Robotics & AI) | *Embedded Systems* Source Code | 2024
 - **System Integration:** Developed browser-controlled robotics suite integrating AI computer vision with low-latency hardware control.
 - **Firmware:** Programmed ESP32 microcontrollers to handle WebSocket communication for real-time motor control and telemetry.
 - **Backend Processing:** Deployed YOLOv5 and OpenCV on host server to process visual feedback and automate robotic decision-making.
- x86 Brick Breakers Arcade | *Assembly (x86), MASM, Low-Level Programming* Source Code | 2024
 - **Game Logic:** Developed a real-time, multiplayer arcade game using x86 Assembly and the MASM assembler.
 - **System Control:** Directly manipulated video memory for low-latency graphics rendering and managed hardware interrupts to handle real-time I/O.

STUDENT ACTIVITIES

- IEEE | *UI/UX Designer - Frontend Team Leader* Cairo | Oct 2025 – Present
 - **Leadership:** Architected intuitive user interfaces and optimized user journey protocols for internal platforms.
- Technical Center for Career Development (TCCD) | *Frontend Developer* Cairo | June 2025 – Present
 - **Development:** Engineered HR dashboard for event tracking and spearheaded optimization of the official TCCD web.
- Physics Helping District (PhD) | *Team Leader* Cairo | June 2022 – 2024
 - **Mentorship:** Led peer tutoring initiative in electronics, achieving measurable academic improvement.

TECHNICAL SKILLS

- **Digital Design & Verification:** Verilog HDL, VHDL, RTL Design, RISC-V ISA, MIPS Architecture, Pipeline Design, RTL-to-GDSII Flow, OpenLane2, DRC/LVS Verification, Static Timing Analysis, FSM Design
- **Development Tools & Platforms:** ModelSim, QuestaSim, Intel Quartus Prime, GTKWave, ESP32, AVR/Arduino
- **Programming Languages:** C/C++ (Advanced), Python, x86 Assembly, MIPS Assembly