Ahmed Fathy

Computer Engineer – FPGA & Embedded Systems
LinkedIn | GitHub | Portfolio

Email: ahmedfathi20044002@gmail.com
Mobile: +20 155 285 1443
Giza, Egypt

Professional Summary

Detail-oriented Computer Engineering student with hands-on experience in FPGA development, digital circuit design, and embedded systems programming. Experienced in ASIC design flow from RTL coding to tape-out. Skilled in RTL design using Verilog and VHDL, with demonstrated ability to implement and verify complex hardware architectures including pipelined processors and hardware accelerators. Eager to apply academic knowledge and project experience to a hardware engineering role.

Education

- **Cairo University, Faculty of Engineering** — Giza, Egypt
  B.Sc. in Computer Engineering; GPA: 3.6 — *2023 – 2027*

Experience

- **Al Nada Scientific Office** — Cairo, Egypt
  Technical Support Trainee — *June 2022 – 2024*
  - **Hardware Diagnostics**: Assisted senior technicians in troubleshooting electronic devices including workstations, printers, and network equipment.
  - **Technical Skills Development**: Gained hands-on experience with hardware diagnostics, firmware updates, and preventive maintenance procedures.
  - **Documentation Support**: Contributed to creating troubleshooting documentation and learned systematic approaches to hardware issue resolution.

Hardware & Embedded Projects

- **Staged Pipelined Processor (RISC)** — Source Code
  Computer Architecture Implementation — *VHDL*
  - **Core Architecture**: Engineered **32-bit** RISC processor utilizing classic **5-stage** pipeline (IF, ID, EX, MEM, WB) with **16 general-purpose registers**.
  - **Hazard Resolution**: Integrated hazard detection units, data forwarding paths, and pipeline stalling mechanisms to resolve data dependencies and control hazards.
  - **Verification**: Validated functional correctness via ModelSim waveform simulations; developed custom Python assembler to generate machine code test vectors.
- **CNN Convolution Accelerator** — Source Code
  VLSI Hardware Acceleration — *Verilog*
  - **Architecture**: Architected high-throughput hardware accelerator for **2D convolution** operations targeting Edge-AI inference workloads.
  - **Micro-Architecture**: Implemented **8x8 Systolic Array** topology with DMA-based data loading and dual-port SRAM buffering for efficient memory bandwidth.
  - **Kernel Support**: Optimized for split-kernel execution supporting **16x16 kernels** using fully pipelined dataflow strategy.
  - **Verification**: Completed RTL-to-GDSII flow using OpenLane2; performed Static Timing Analysis (STA), DRC, and LVS verification with GTKWave waveform analysis.
- **AES Encryption/Decryption Engine** — Source Code
  Cryptographic Core Design — *Verilog*
  - **Core Logic**: Synthesized robust AES cryptographic core in Verilog HDL supporting **128-bit, 192-bit, and 256-bit** key standards.
  - **Datapath**: Engineered hardware-optimized modules for SubBytes, ShiftRows, MixColumns, and AddRoundKey transformations.
  - **Validation**: Verified cryptographic correctness against standard NIST test vectors using rigorous debug tracing.
- **Tactic (Robotics & AI)** — Source Code
  IoT & Computer Vision Integration — *Embedded Systems*

- **System Integration**: Developed browser-controlled robotics suite integrating AI computer vision with low-latency hardware control.
- **Firmware**: Programmed ESP32 microcontrollers to handle WebSocket communication for real-time motor control and telemetry.
- **Backend Processing**: Deployed YOLOv5 and OpenCV on host server to process visual feedback and automate robotic decision-making.

- **Brick Breakers Arcade** Source Code
  Low-Level Game Development *Assembly (x86)*
  - **Low-Level Logic**: Programmed competitive multiplayer game directly in 8086 Assembly, bypassing high-level abstractions.
  - **Interrupts**: Manipulated hardware interrupts for real-time keyboard input (A/D keys) and video memory mapping.
  - **Execution**: Optimized execution flow within MASM/DOSBox environment.

Student Activities

- **IEEE** Cairo
  UI/UX Designer - Frontend Team Leader *Oct 2025 – Present*
  - **Interface Design**: Architected intuitive user interfaces for internal platforms, optimizing user journey and accessibility protocols.
- **Technical Center for Career Development (TCCD)** Cairo
  Frontend Developer *June 2025 – Present*
  - **HR Management System**: Engineered internal dashboard enabling HR personnel to monitor events, track attendees, and analyze participation metrics.
  - **Web Maintenance**: Spearheaded development and ongoing optimization of official TCCD web presence.
- **Physics Helping District (PhD)** Cairo
  Team Leader *June 2022 – 2024*
  - **Mentorship Initiative**: Directed student-led initiative supporting peers in physics and electronics via tutoring and practical workshops, resulting in measurable academic improvement.

Technical Skills

- **RTL Design & Synthesis**: Verilog HDL, VHDL, SystemVerilog, Digital Logic Synthesis, Finite State Machines (FSM), Timing Closure
- **EDA Tools & Simulation**: ModelSim, QuestaSim, Intel Quartus Prime, Xilinx Vivado, GTKWave, Waveform Analysis
- **Embedded Systems Development**: ESP32 Microcontrollers, AVR/Arduino Platforms, ARM Cortex Architecture, UART Protocol, SPI Protocol, I2C Protocol, GPIO Interface
- **Computer Architecture**: RISC-V ISA, MIPS Architecture, Pipeline Design, Hazard Detection, Memory Hierarchy, Cache Coherence
- **VLSI Design Concepts**: Systolic Array Architecture, Hardware Accelerators, DMA Controllers, Static Timing Analysis, Resource Utilization
- **Programming Languages**: C/C++ Programming (Advanced), Python Scripting, x86 Assembly Language, MIPS Assembly Language