

LCD Display Module

QC12864B

User Manual

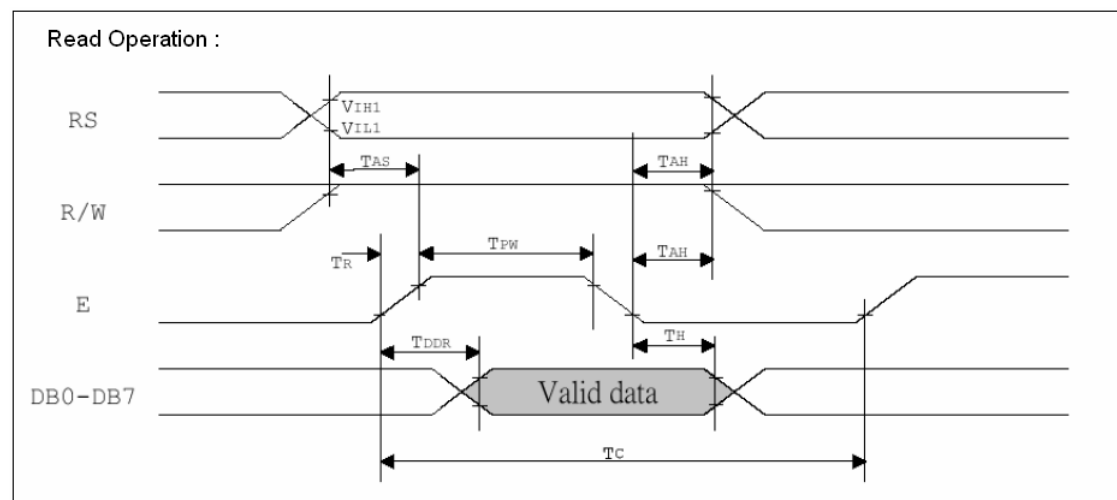
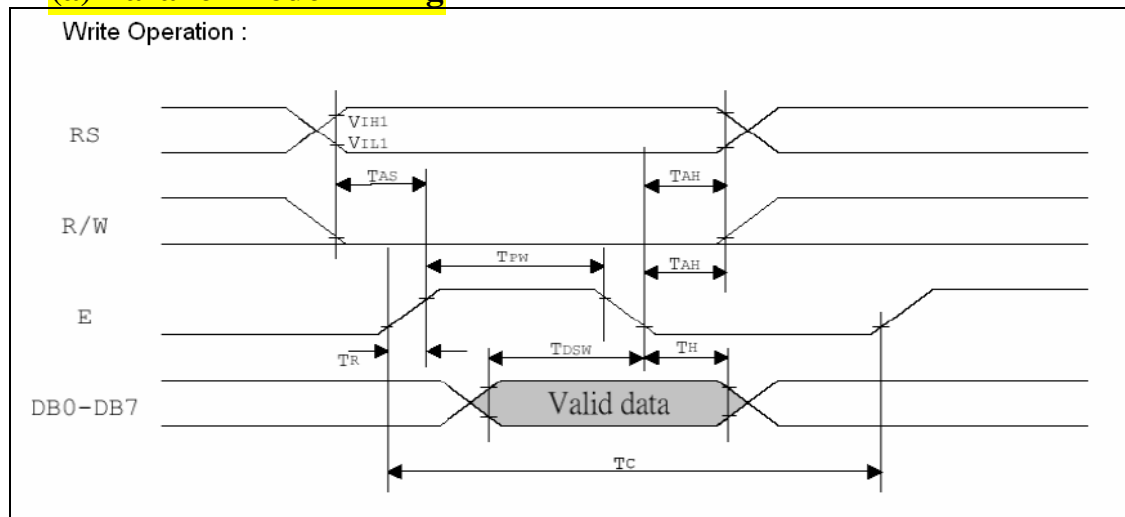
LCD12864 Specification

1. Features

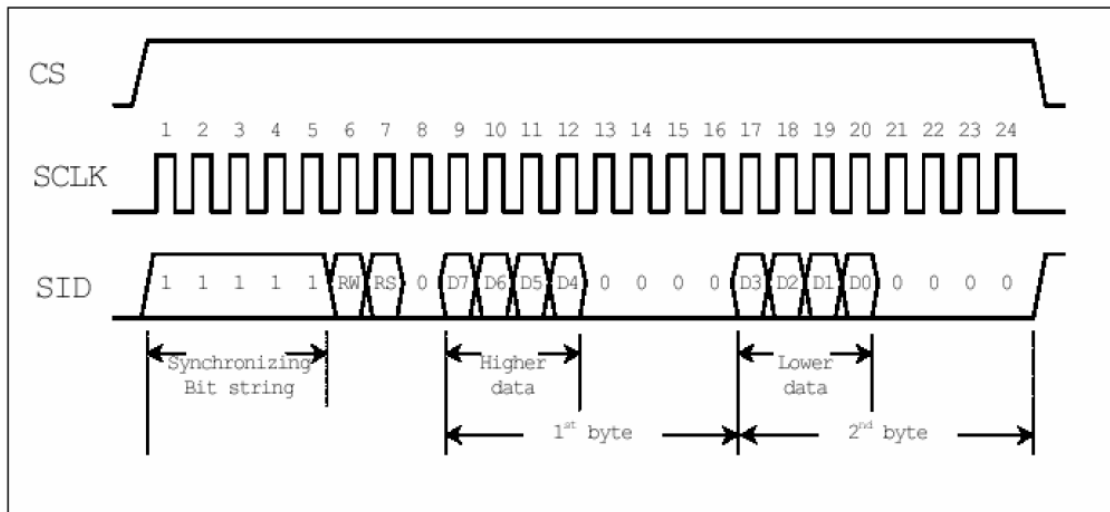
- . Display construction - 128 * 64 Dots
- . Display mode - STN
- . Display color - Yellow Green / Blue
- . Viewing direction - 6 o' clock
- . Operating Power - **VCC 5V**
- . Type - COB (Chip On Board)
- . MCU I/F - **8-bit parallel or serial**
- . Backlight - **LED**

2. Read/Write Timing

(a) Parallel Mode Timing



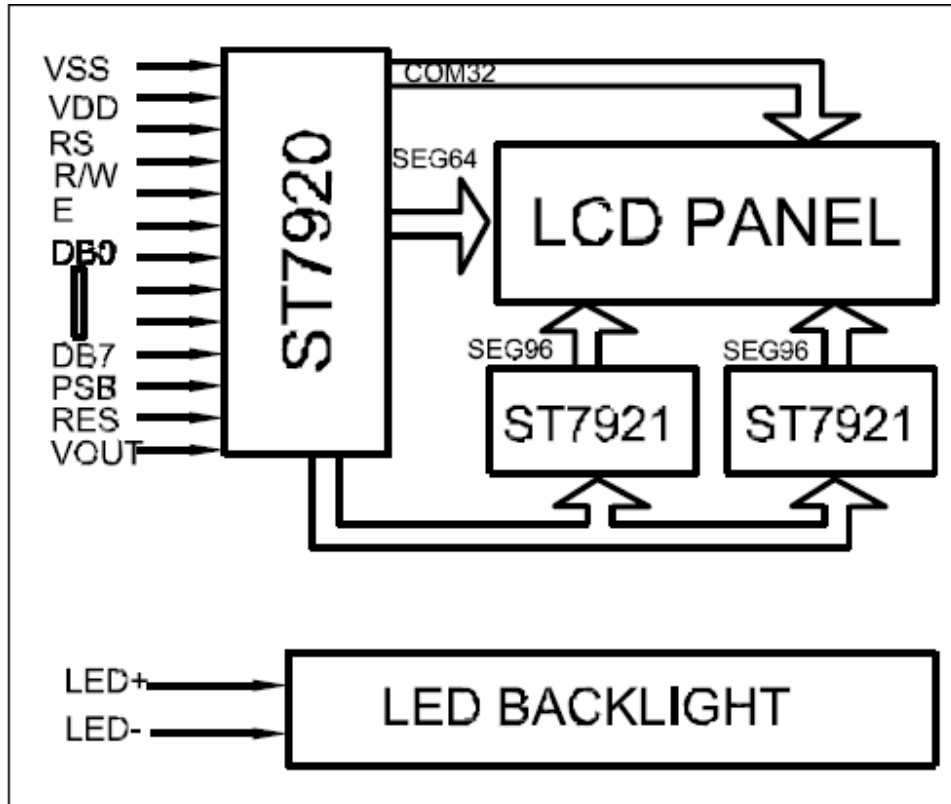
(b) Serial Mode Timing



3. Electrical Characteristics

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------------|------------------|------|------|------|---------|
| <i>Internal Clock Operation</i> | | | | | | |
| f_{OSC} | OSC Frequency | R = 33K Ω | 470 | 530 | 590 | KHz |
| <i>External Clock Operation</i> | | | | | | |
| f_{EX} | External Frequency | - | 470 | 530 | 590 | KHz |
| | Duty Cycle | - | 45 | 50 | 55 | % |
| T_R, T_F | Rise/Fall Time | - | - | - | 0.2 | μ s |
| TSCYC | Serial clock cycle | Pin E | 400 | - | - | ns |
| TSHW | SCLK high pulse width | Pin E | 200 | - | - | ns |
| TSLW | SCLK low pulse width | Pin E | 200 | - | - | ns |
| TSDS | SID data setup time | Pins RW | 40 | - | - | ns |
| TSDH | SID data hold time | Pins RW | 40 | - | - | ns |
| TCSS | CS setup time | Pins RS | 60 | - | - | ns |
| TCSH | CS hold time | Pins RS | 60 | - | - | ns |

4. Block Diagram



5. Instruction Set

Instruction set 1: (RE=0: basic instruction)

| Ins | code | | | | | | | | | | Description | Exec time (540KHZ) |
|------------------------------|------|----|-----|-----|-----|-----|-----|---------|-----|-----|---|-----------------------|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| CLEAR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Fill DDRAM with "20H", and set DDRAM address counter (AC) to "00H" | 1.6 ms |
| HOME | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | Set DDRAM address counter (AC) to "00H", and put cursor to origin ; the content of DDRAM are not changed | 72us |
| ENTRY MODE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Set cursor position and display shift when doing write or read operation | 72us |
| DISPLAY ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | D=1: display ON C=1: cursor ON B=1: blink ON | 72 us |
| CURSOR DISPLAY CONTROL | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | Cursor position and display shift control ; the content of DDRAM are not changed | 72 us |
| FUNCTION SET | 0 | 0 | 0 | 0 | 1 | DL | X | 0 RE | X | X | DL=1 8-BIT interface DL=0 4-BIT interface <u>RE=1: extended instruction</u> <u>RE=0: basic instruction</u> | 72 us |

| | | | | | | | | | | | | |
|--|---|---|----|----------|-----|-----|-----|-----|-----|-----|--|-------|
| SET CGRAM ADDR. | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address to address counter (AC) <u>Make sure that in extended instruction SR=0 (scroll or RAM address select)</u> | 72 us |
| SET DDRAM ADDR. | 0 | 0 | 1 | 0 AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address to address counter (AC) AC6 is fixed to 0 | 72 us |
| READ BUSY FLAG (BF) & ADDR. | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Read busy flag (BF) for completion of internal operation, also Read out the value of address counter (AC) | 0 us |
| WRITE RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data to internal RAM (DDRAM/CGRAM/IRAM/GDRAM) | 72 us |
| READ RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM/IRAM/GDRAM) | 72 us |

Instruction set 2: (RE=1: extended instruction)

| Inst. | code | | | | | | | | | | description | Exec. time (540KHZ) |
|-------------------------------------|------|----|-----|----------|----------|----------|-----|---------|-----|-----|--|------------------------|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| STAND BY | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Enter stand by mode, any other instruction can terminate (Com1..32 halted, only Com33 ICON can display) | 72 us |
| SCROLL or RAM ADDR. SELECT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SR | SR=1: enable vertical scroll position SR=0: enable IRAM address (<u>extended instruction</u>) SR=0: enable CGRAM address(<u>basic instruction</u>) | 72 us |
| REVERSE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | R1 | R0 | Select 1 out of 4 line (in DDRAM) and decide whether to reverse the display by toggling this instruction R1,R0 initial value is 00 | 72 us |
| EXTENDED FUNCTION SET | 0 | 0 | 0 | 0 | 1 | DL | X | 1 RE | G | 0 | DL=1 8-BIT interface DL=0 4-BIT interface <u>RE=1: extended instruction set</u> <u>RE=0: basic instruction set</u> G=1 :graphic display ON G=0 :graphic display OFF | 72 us |
| SET IRAM or SCROLL ADDR. | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | SR=1: AC5~AC0 the address of vertical scroll SR=0: AC3~AC0 the address of ICON RAM | 72 us |
| SET GRAPHIC RAM ADDR. | 0 | 0 | 1 | 0 AC6 | 0 AC5 | 0 AC4 | AC3 | AC2 | AC1 | AC0 | Set GDRAM address to address counter (AC) First set vertical address and the horizontal address by consecutive writing Vertical address range AC6...AC0 Horizontal address range AC3...AC0 | 72 us |

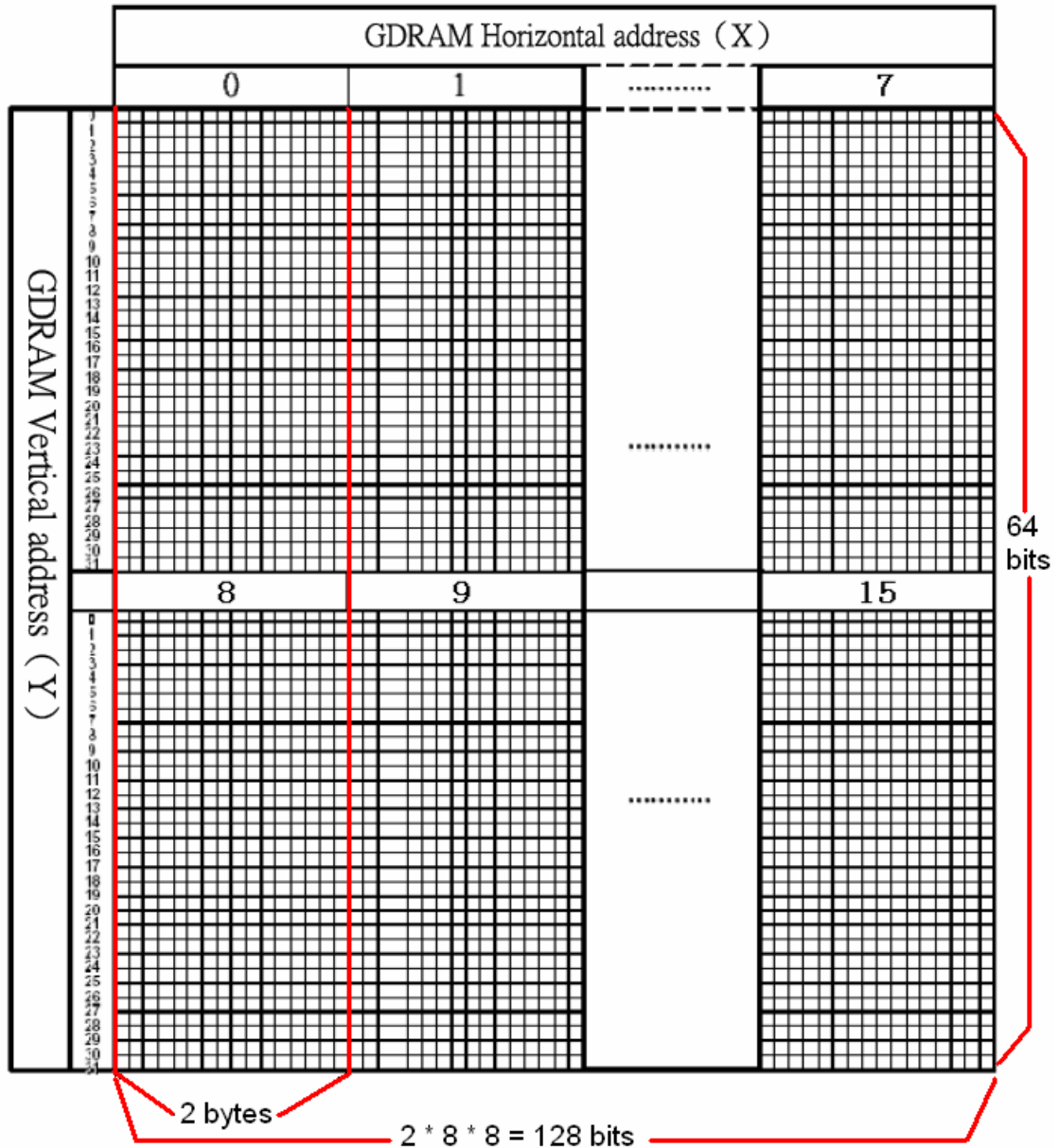
Note :

1. **Make sure that ST7920 is not in busy state** by reading the busy flag **before** sending instruction or data.
If use delay loop instead please make sure the delay time is enough. Please refer to the instruction execution time.
2. **“RE” is the selection bit of basic and extended instruction set.** Each time when altering the value of RE it will remain. There is no need to set RE every time when using the same group of instruction set.

6. Coordinate

6.1 Graphic display coordinate

- Horizontal X : unit is bytes.
- Vertical Y : unit is bit.

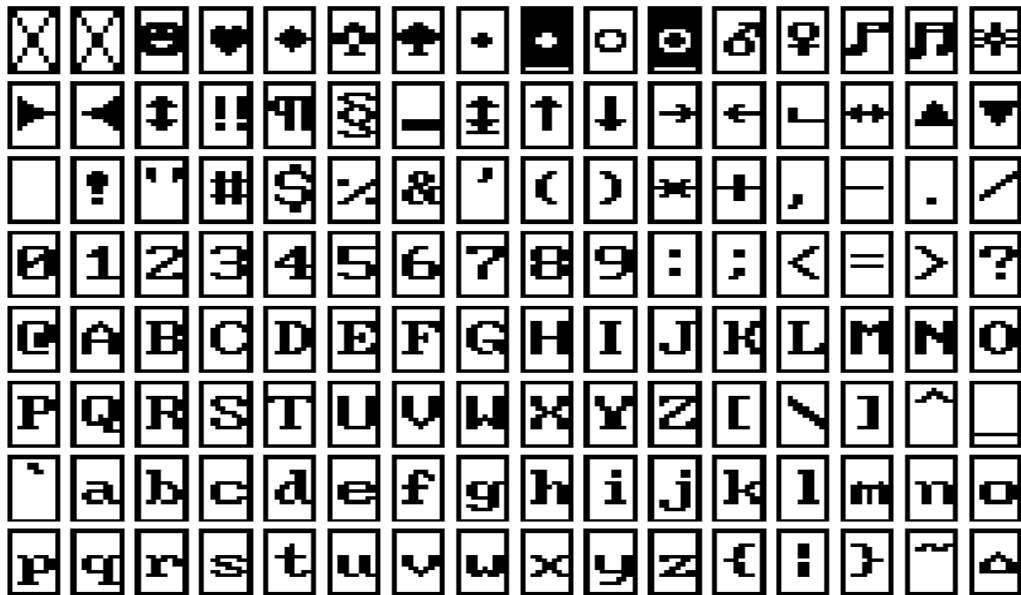


6.2 Character Display Coordinate

| | X Address | | | | | | | |
|-------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Line1 | 80H | 81H | 82H | 83H | 84H | 85H | 86H | 87H |
| Line2 | 90H | 91H | 92H | 93H | 94H | 95H | 96H | 97H |
| Line3 | 88H | 89H | 8AH | 8BH | 8CH | 8DH | 8EH | 8FH |
| Line4 | 98H | 99H | 9AH | 9BH | 9CH | 9DH | 9EH | 9FH |

6.3 Character Map

- Address : 00 – 7F

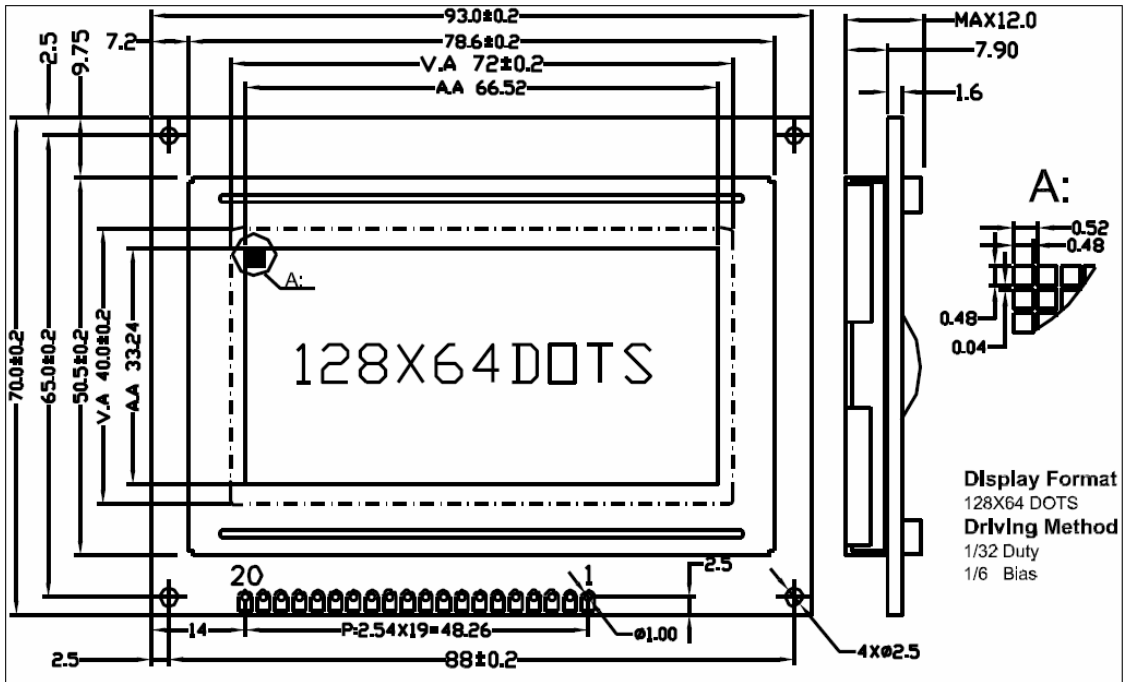


7. Access Graphic RAM (GDRAM)

GDRAM address is set by writing 2 consecutive bytes for vertical address and horizontal address. Two-bytes data write to GDRAM for one address. Address counter will automatically increase by one for the next two-byte data. The procedure is as followings.

1. Set vertical address (Y) for GDRAM
2. Set horizontal address (X) for GDRAM
3. Write D15~D8 to GDRAM 中(first byte)
4. Write D7~D0 to GDRAM 中(second byte)

8. Dimension



9. Interface

| PIN NO. | SYMBOL | DESCRIPTION | FUNCTION |
|---------|-----------|--|---|
| 1 | VSS | GROUND | 0V (GND) |
| 2 | VDD | POWER SUPPLY FOR LOGIC CIRCUIT | +5V |
| 3 | V0/VDD/NC | LCD CONTRAST ADJUSTMENT OR LCD VOLTAGE OR NC | |
| 4 | D/I | INSTRUCTION/DATA REGISTER SELECTION | D/I = 0 : INSTRUCTION REGISTER D/I = 1 : DATA REGISTER |
| 5 | R/W | READ/WRITE SELECTION | R/W = 0 : REGISTER WRITE R/W = 1 : REGISTER READ |
| 6 | E | ENABLE SIGNAL | |
| 7 | DB0 | DATA INPUT/OUTPUT LINES | 8 BIT: DB0-DB7 |
| 8 | DB1 | | |
| 9 | DB2 | | |
| 10 | DB3 | | |
| 11 | DB4 | | |
| 12 | DB5 | | |
| 13 | DB6 | | |
| 14 | DB7 | | |
| 15 | PSB | SERIAL/PARALLEL SELECTION | PSB=0:SERIAL MODE PSB=1 3/4BIT PARALLEL BUS MODE |
| 16 | NC | | |
| 17 | RST | RESET SIGNAL | RSTB=0,DISPLAY OFF,DISPLAY FROM LINE 0. |
| 18 | VEE/NC | LCD DRIVE VOLTAGE/NC | |
| 19 | A | SUPPLY VOLTAGE FOR LED+ | +5V |
| 20 | K | SUPPLY VOLTAGE FOR LED- | 0V |