Mansoura University
Faculty of Computers and Information
Department of Computer Science
First Semester- 2020-2021

[CS131]

Computer Organization & Architecture

Grade: 2

DR: Zahraa Tarek, Reem El-Deep

Input/Output Systems

AGENDA

- I/O Introduction
- I/O Architecture
- Bus Operation
  - Types of bus
  - System bus (Data bus- Address Bus- Control Bus)
- Bus arbitration
  - Daisy chain arbitration
  - Centralized parallel arbitration
  - Distributed arbitration using self- selection
  - Distributed arbitration using collision detection

I/O INTRODUCTION

- The I/O subsystem of a computer provides an efficient mode of communication between the central system and the outside environment. It handles all the input-output operations of the computer system.
- Peripheral Devices:
  - Input or output devices that are connected to computer are called **peripheral devices**. These devices are designed to read information into or out of the memory unit upon command from the CPU and are considered to be the part of computer system. These devices are also called **peripherals**.

I/O INTRODUCTION

- There are three types of peripherals:

1. **Input peripherals** : Allows user input, from the outside world to the computer. Example: Keyboard, Mouse etc.
2. **Output peripherals**: Allows information output, from the computer to the outside world. Example: Printer, Monitor etc
3. **Input-Output peripherals**: Allows both input(from outised world to computer) as well as, output(from computer to the outside world). Example: Touch screen etc.

I/O ARCHITECTURE

- We will define I/O as a subsystem.
- I/O subsystems include, but not limited to:

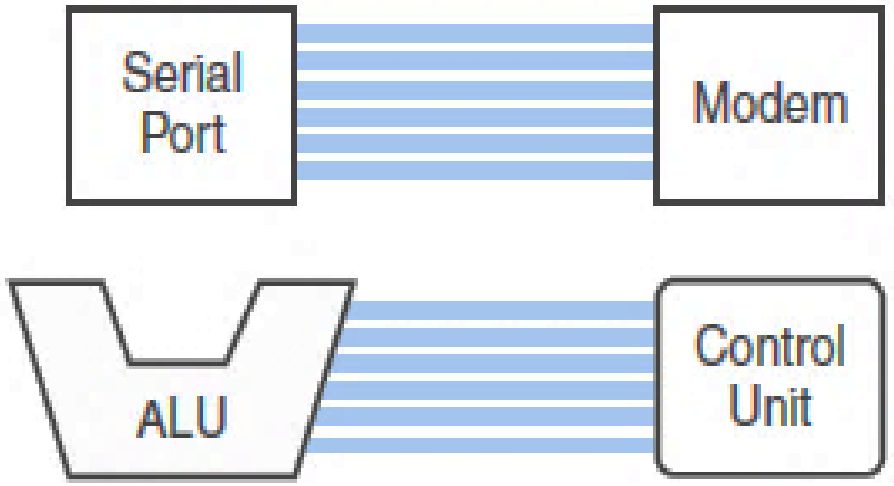
  - Blocks of main memory that are devoted to I/O functions
  - Buses that provide the means of moving data into and out of the system
  - Control modules in the host and in peripheral devices
  - Interfaces to external components such as keyboards and disks
  - Cabling or communications links between the host system and its peripherals

Bus

- **A bus** is a set of wires that acts as a shared data path to connect multiple subsystems within the system.
- **A bus** consists of multiple lines allowing parallel movements of bits.
- **Buses** are low cost but very versatile.
- It is easy to connect new devices to each other and to the system.
- At any one time only one device may use the bus.
- The speed of the bus is affected by its length as well as the number of devices sharing it.

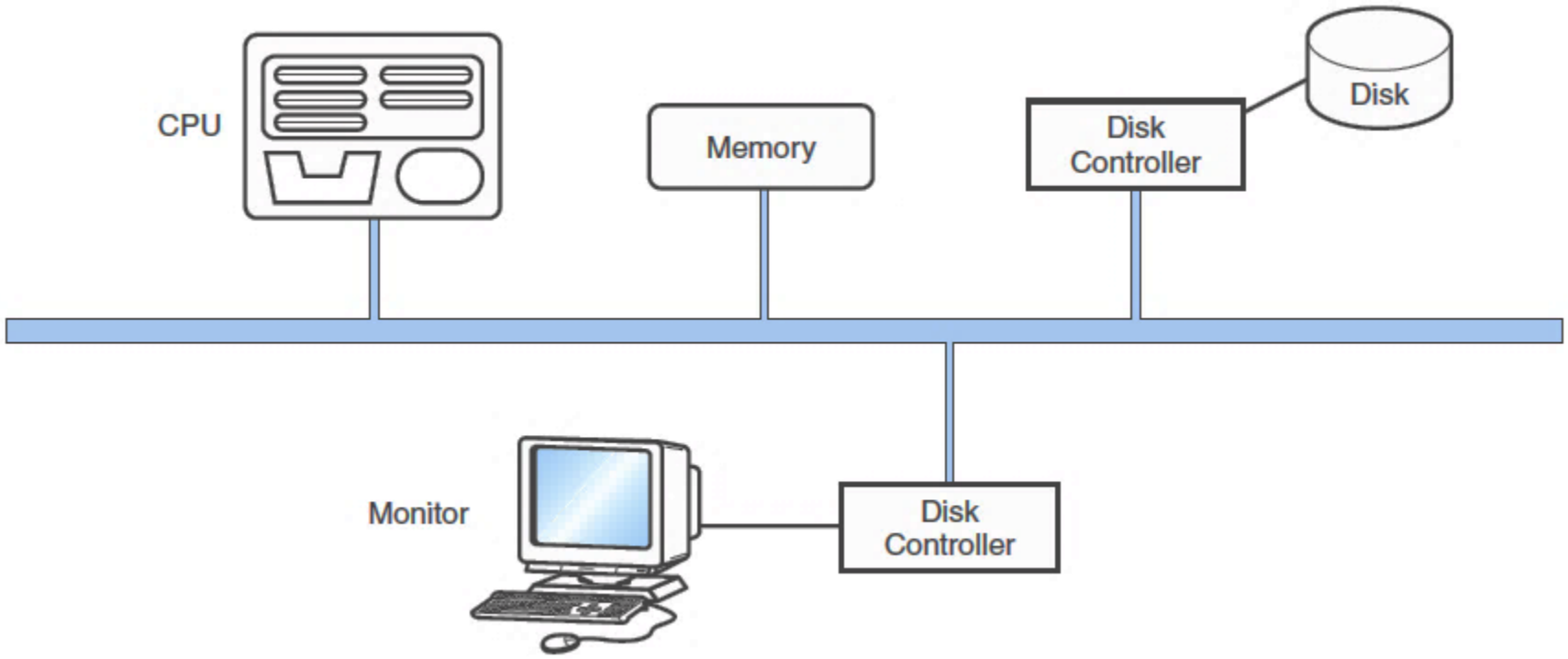
Bus

- A bus can be point-to-point, connecting two specific components.



BUS

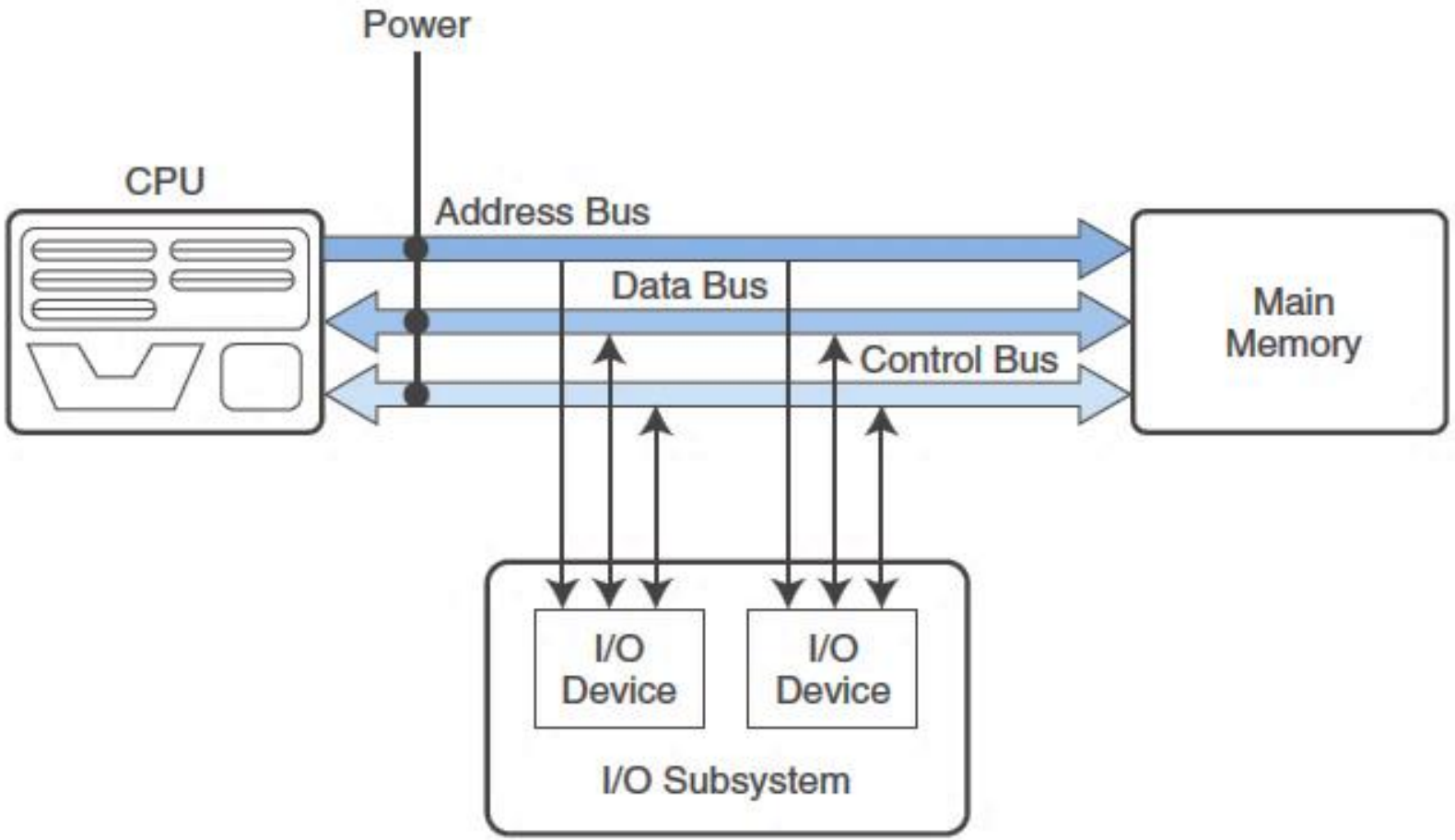
- A bus can be a common pathway (a multipoint bus) that connect a number of devices, requiring these devices to share the bus



SYSTEM BUS

- **System bus** is a bus that connect major components (processor, memory, I/O)
- It contains many hundreds of separate lines and each group of them has a separate function.
- **System bus is separated into three functional groups**:
  - Data bus
  - Address bus
  - Control Bus

Components of Typical Bus



Components of Bus

- **Data bus:** the lines of a bus that carry data.
- It consists of 8, 16,32,….etc. separate lines.
- The number of lines referred as width of data bus.
- Each line carries only one bit.
- It is a bidirectional bus.

Components of Bus

- **Address bus :** collection of wires used to identify particular location in main memory.
- It is used to identify the source or destination of data.
- It is a unidirectional bus.
- The data should be either read from or written to.
- The bus width determine the maximum memory capacity of the system.

Components of Bus

- **Control bus:** regulates the activity on the bus.
- Indicate which device has permission to use the bus and for what purpose (reading or writing from memory or from I/O device.
- It carries signals that report the status of various devices
  - Memory read: get the data from address location to be placed on the data bus
  - Memory write: data should place on address location.
  - I/O read: get the data from Input device to be placed on the data bus
  - I/O write: data should place on output device .

TYPES OF BUSES

- **Processor-Memory buses:**
  - ✓ Short,
  - ✓ high speed buses closely matched to memory system to maximize bandwidth (transfer of data)
  - ✓ Very design specific.
- **I/O Buses:**
  - ✓ Longer than processor-memory buses
  - ✓ Allow for many types of devices with varying bandwidths.
  - ✓ Compatible with many different architecture.

TYPES OF BUSES

- **Backplane bus:**
  - ✓ Is built into the chassis of the machine and connects the processor, the I/O devices, and the memory (All devices share one bus)
- Many computers have a hierarchy of buses (Two or more).
- High performance systems often use all three types of buses.

BUSES

- Devices are divided into master and slave categories.
- **Master** devices is one that initiates actions.
- **Slave** is one that responds to requests by a master.
- In a very simple system **the processor** is the only one allowed to be the **bus master**.
- It is good in avoiding conflict, but it needs processor to be involved in every transaction uses the bus.
- In system with more than one master device **a bus arbitration** is needed.

Bus Arbitration

- Bus arbitration must provide priority to master device to make sure lower priority devices are not starved out at the same time.
- **Categories of Bus arbitration schemes:**
  - ✓ **Daisy chain arbitration**
    - uses a "grant bus" control line that passed down the bus from the height priority to the lowest priority devices.
    - Fairness is not ensured (low priority devices may be starved out –never allowed to use the bus)
    - Simple but not fair.

Bus Arbitration

- **Categories of Bus arbitration schemes:**
  - ✓ **Centralized parallel arbitration**
    - Each device has a request control line to the bus.
    - A centralized arbiter selects who gets the bus.
    - Bottleneck can result.
  - ✓ **Distributed arbitration using self-selection**
    - similar to centralized arbitration
    - Instead of a central authority to get the bus, the devices themselves determine who has the height priority and get the bus.

Bus Arbitration

- **Categories of Bus arbitration schemes:**
  - ✓ **Distributed arbitration using collision detection**
    - Each device is allowed to make request for the bus.
    - If collision (multi requests in the same time), the device must make another request.

Thank You