Asynchronous FIFO Assignment

Submitted by:
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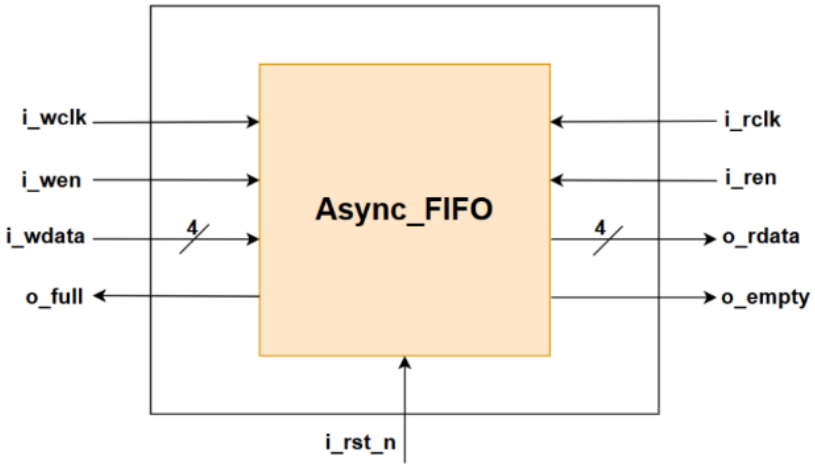
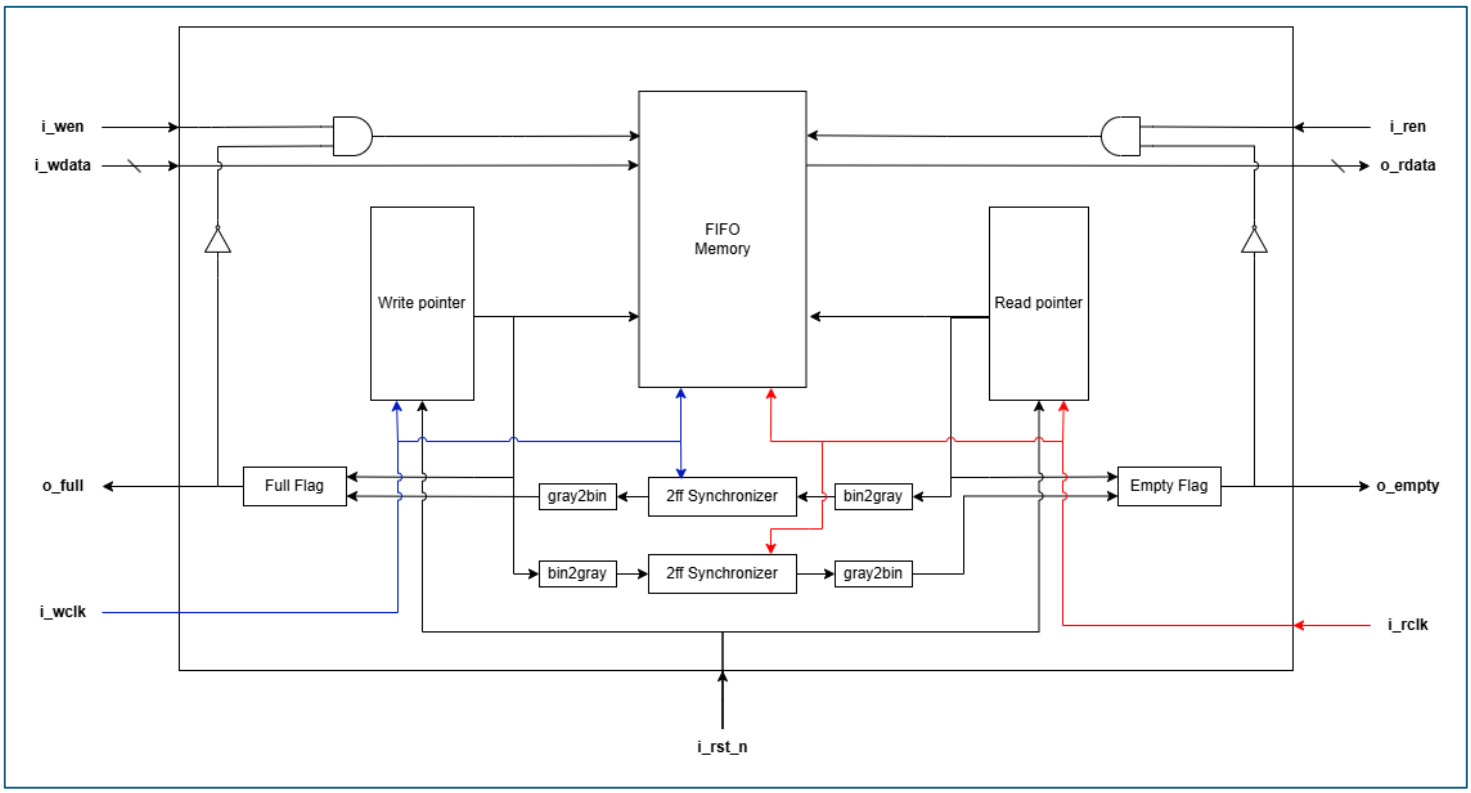
1-FIFO Ports



Signal	Width	Direction	Description
i_rst_n	1	Input	Negative edge asynchronous system reset in both domains.
i_wclk	1	Input	Positive edge clock of the write domain.
i_wen	1	Input	Write enable at the write domain: (1: write operation , 0: no write operation)
i_wdata	4	Input	Data written in the FIFO at the write domain in case of write operation.
o_full	1	Output	Flag Indicates that the FIFO is full (there is no space available to write new data).
i_rclk	1	Input	Positive edge clock of the read domain.
i_ren	1	Input	read enable at write domain: (1: read operation , 0: no read operation)
i_rdata	4	Output	Read data from the FIFO at the read domain in case of read operation.
o_empty	1	Output	Flag Indicates that the FIFO is empty (there is no data available to read).

2- System Block Diagram.



Block explanation

- **Write Pointer**: Operates in the write clock domain and increments when data is written. It points to the current write address in the FIFO memory.

- **Read Pointer**: Operates in the read clock domain and increments when data is read. It points to the current read address in the FIFO memory.

- **FIFO Memory**: A dual-port memory that stores data.

- **2FF Synchronizers**: Double flip-flop synchronizers are used to safely transfer the Gray-coded pointers between the clock domains.

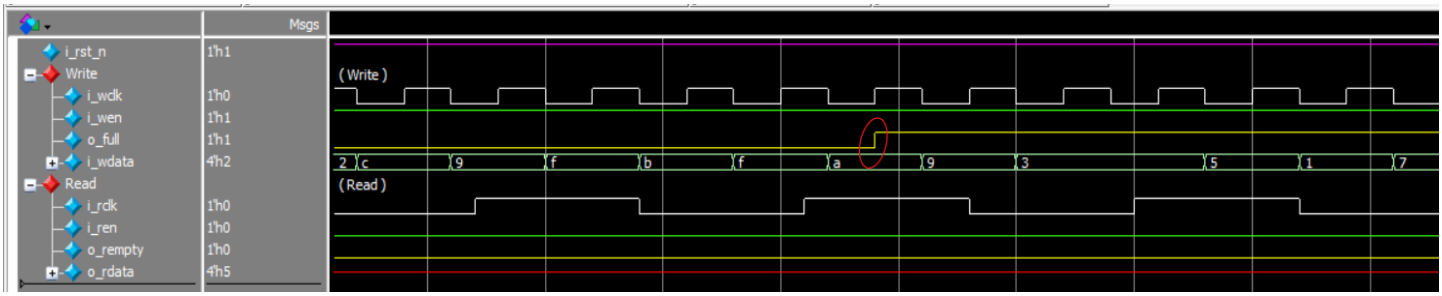
- **bin2gray / gray2bin Converters**: These convert binary pointers to Gray code and vice versa. Gray code is used to reduce errors during synchronization.

- **Full Flag**: Indicates when the FIFO is full.

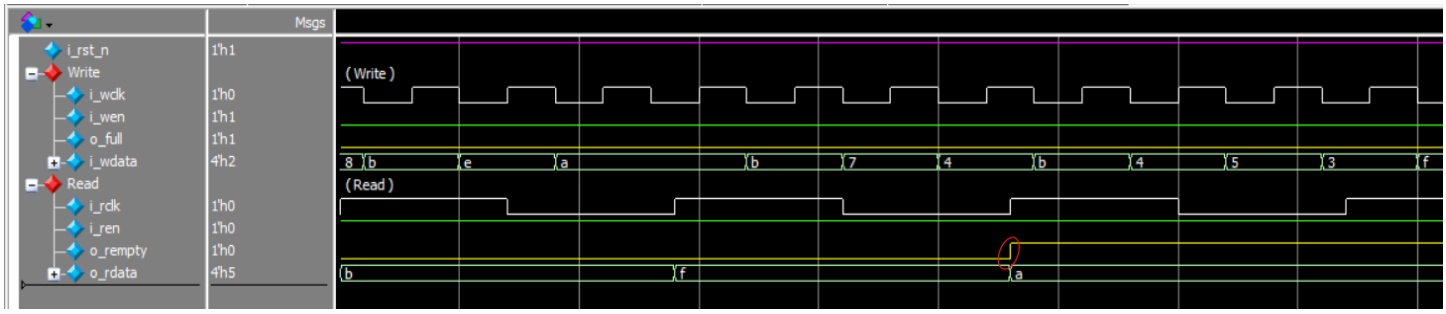
- **Empty Flag**: Indicates when the FIFO is empty.

3-Simulation results

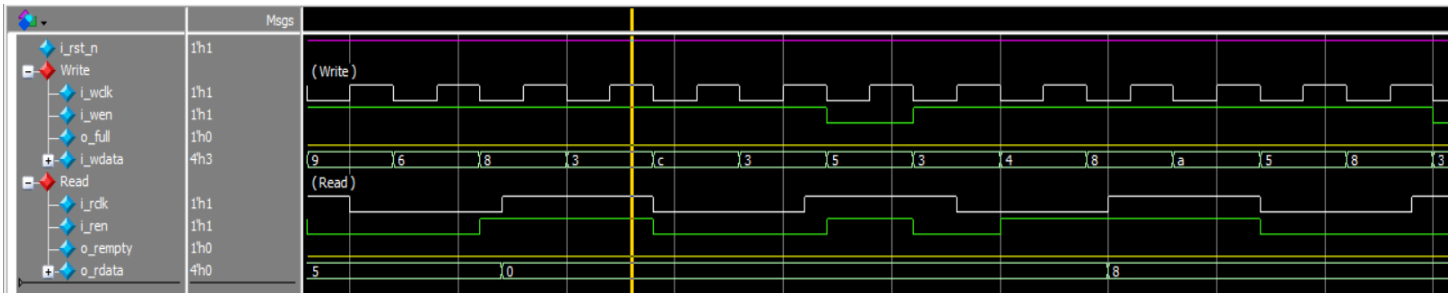
Test write operation and full flag



Test read operation and empty flag

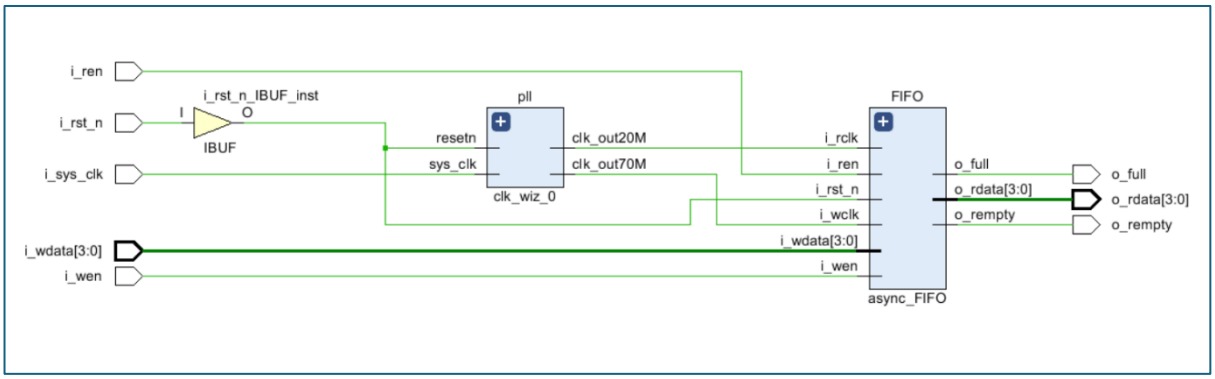


Test simultaneous read and write

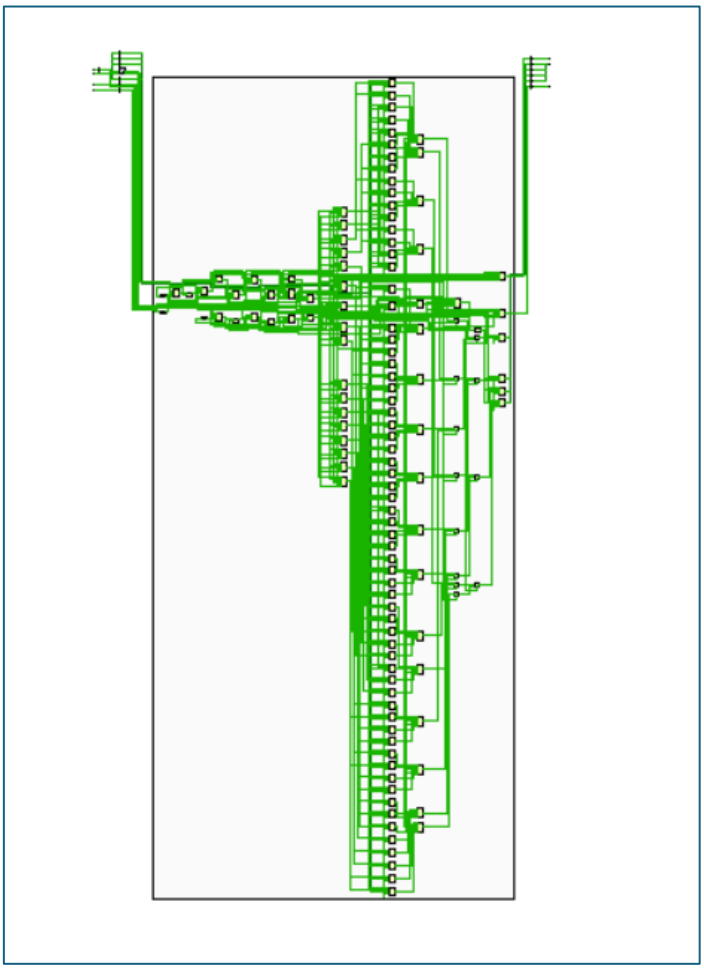


4- Vivado results

Elaboration result:



Synthesis result:



Implementation result: