

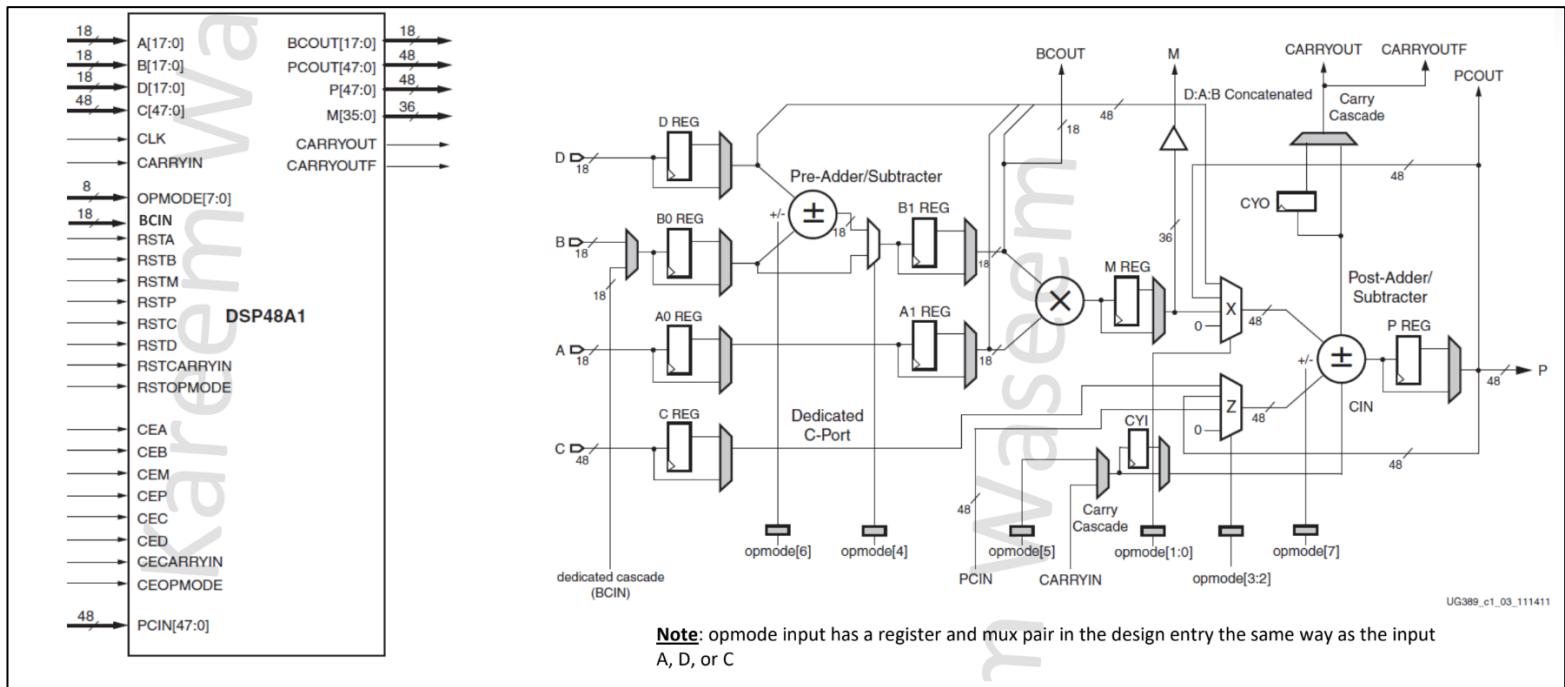
Spartan6-DSP48A1

by

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Under the guidance of **Eng. Kareem Waseem**

Schematic



1. RTL code



Digital Design - DSP48A1.v

```
1 module DSP48A1(
2     A, B, C, D, CARRYIN, M, P, CARRYOUT, CARRYOUTF, CLK, OPMODE,
3     CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, RSTA, RSTB,
4     RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP, BCOUT, BCIN ,PCIN, PCOUT
5 );
6
7 parameter A0REG      = 0,
8     A1REG      = 1,
9     B0REG      = 0,
10    B1REG      = 1,
11    CREG       = 1,
12    DREG       = 1,
13    MREG       = 1,
14    PREG       = 1,
15    CARRYINREG = 1,
16    CARRYOUTREG = 1,
17    OPMODEREG   = 1;
18
19 parameter CARRYINSEL = "OPMODES", //or CARRYIN -> else tie to 0
20     B_INPUT     = "DIRECT", //CASCADE -> else tie to 0
21     RSTTYPE     = "SYNC"; //ASYNC
22
23 ///////////////
24 //Data Ports://
25 ///////////////
26     input [17:0] A, B, D;
27     input [47:0] C;
28     input CARRYIN;
29
30     output [35:0] M;
31     output [47:0] P;
32     output CARRYOUT, CARRYOUTF;
33
34 /////////////////
35 //Control Input Ports://
36 /////////////////
37     input CLK;
38     input [7:0] OPMODE;
39
40 /////////////////
41 //Clock Enable Input Ports://
42 /////////////////
43     input CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;
44
45 /////////////////
46 //Reset Input Ports://
47 /////////////////
48     input RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;
49
50
51 ///////////////
52 //Cascade Ports://
53 ///////////////
54     input [17:0] BCIN;
55     output [17:0] BCOUT;
56
57     input [47:0] PCIN;
58     output [47:0] PCOUT;
59
60
61 /////////////////
62     wire [7:0] mux_OPMODE_out;
63     wire [17:0] mux_D_out, mux_B0_input, mux_B0_out, mux_A0_out;
64     wire [47:0] mux_C_out;
65
66 //OPMODE
67     mux_with_reg #(.RSTTYPE(RSTTYPE), .SIZE(8)) mux_OPMODE(.I(OPMODE), .sel(OPMODEREG), .CLK(CLK),
68     .rst(RSTOPMODE), .EN(CEOPMODE), .out(mux_OPMODE_out));
69
70 //D Input
71     mux_with_reg #(.RSTTYPE(RSTTYPE), .SIZE(18)) mux_D(.I(D), .sel(DREG), .CLK(CLK), .rst(RSTD), .EN(CED), .out(mux_D_out));
72
73 //B Input
74     assign mux_B0_input = (B_INPUT == "DIRECT") ? B : (B_INPUT == "CASCADE") ? BCIN : 0;
75     mux_with_reg #(.RSTTYPE(RSTTYPE), .SIZE(18)) mux_B0(.I(mux_B0_input), .sel(B0REG), .CLK(CLK),
76     .EN(CEB), .rst(RSTB), .out(mux_B0_out));
77
78 //A Input
79     mux_with_reg #(.RSTTYPE(RSTTYPE), .SIZE(18)) mux_A0(.I(A), .sel(A0REG), .CLK(CLK), .rst(RSTA), .EN(CEA), .out(mux_A0_out));
80
81 //C Input
82     mux_with_reg #(.RSTTYPE(RSTTYPE), .SIZE(48)) mux_C(.I(C), .sel(CREG), .CLK(CLK), .rst(RSTC), .EN(CEC), .out(mux_C_out));
83
84 /////////////////
```




Digital Design - mux_with_reg.v

```
1 module mux_with_reg(I, sel, CLK, EN, rst, out);
2     parameter RSTTYPE = "SYNC", // ASYNC
3             SIZE      = 1;
4
5     input [SIZE-1:0] I;
6     input sel, CLK, EN, rst;
7     output [SIZE-1:0] out;
8
9     reg [SIZE-1:0] I_reg;
10
11    assign out = (~sel) ? I : I_reg;
12
13    generate
14        if(RSTTYPE == "SYNC") begin
15            always @(posedge CLK) begin
16                if(rst)
17                    I_reg <= 0;
18                else if(EN)
19                    I_reg <= I;
20                end
21            end
22        else if(RSTTYPE == "ASYNC") begin
23            always @(posedge CLK, posedge rst) begin
24                if(rst)
25                    I_reg <= 0;
26
27                else if(EN)
28                    I_reg <= I;
29                end
30            end
31        endgenerate
32
33    endmodule
```

2. Testbench

Digital Design - DSP48A1_tb.v

```
1 module DSP48A1_tb;
2   parameter A0REG      = 0,
3             A1REG      = 1,
4             B0REG      = 0,
5             B1REG      = 1,
6             CREG       = 1,
7             DREG       = 1,
8             MREG       = 1,
9             PREG       = 1,
10            CARRYINREG = 1,
11            CARRYOUTREG = 1,
12            OPMODEREG   = 1;
13
14  parameter CARRYINSEL = "OPMODE5",    //or CARRYIN -> else tie to 0
15        B_INPUT      = "DIRECT",     //CASCADE -> else tie to 0
16        RSTTYPE      = "SYNC";      // ASYNC
17
18  reg CLK;
19  reg CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;
20  reg RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;
21
22 //Input Signals
23  reg [17:0] A, B;
24  reg [47:0] C;
25  reg [17:0] D;
26
27  reg CARRYIN;
28
29  reg [7:0] OPMODE;
30
31  reg [17:0] BCIN;
32  reg [47:0] PCIN;
33
34 //Output Signals//
35  wire [35:0] M;
36  wire [47:0] P;
37  wire CARRYOUT, CARRYOUTF;
38  wire [17:0] BCOUT;
39  wire [47:0] PCOUT;
40
41 DSP48A1 #(A0REG, A1REG, B0REG, B1REG, CREG, DREG, MREG, PREG, CARRYINREG,
42           CARRYOUTREG, OPMODEREG, CARRYINSEL, B_INPUT, RSTTYPE)
43 dut(A, B, C, D, CARRYIN, M, P, CARRYOUT, CARRYOUTF, CLK, OPMODE,
44      CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, RSTA, RSTB,
45      RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP, BCOUT, BCIN ,PCIN, PCOUT);
46
47 initial begin
48   CLK = 0;
49   forever
50     #1 CLK = ~CLK;
51 end
52
53 initial begin
54   {A, B, C, D, CARRYIN, OPMODE, BCIN, PCIN} = 0;
55   {CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP} = 0;
56
57   {RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP} = {8{1'b1}};
58   @(negedge CLK);
59   {RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP} = 0;
60
61   {CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP} = {8{1'b1}};
62
63
64 ///////////////
65 //pre-adder/subtractor//
66 ///////////////
67 OPMODE[6] = 0; //addition
68 OPMODE[4] = 1;
69 repeat(2) begin
70   repeat(100) begin
71     D = $random;
72     B = $random;
73     @(negedge CLK);
74   end
75   OPMODE[6] = 1; //subtraction
76 end
77
78 ///////////////
79 //multiplier//
80 ///////////////
81 OPMODE[4] = 0;
82 repeat(100) begin
83   B = $random;
84   A = $random;
85   @(negedge CLK);
86 end
87
```

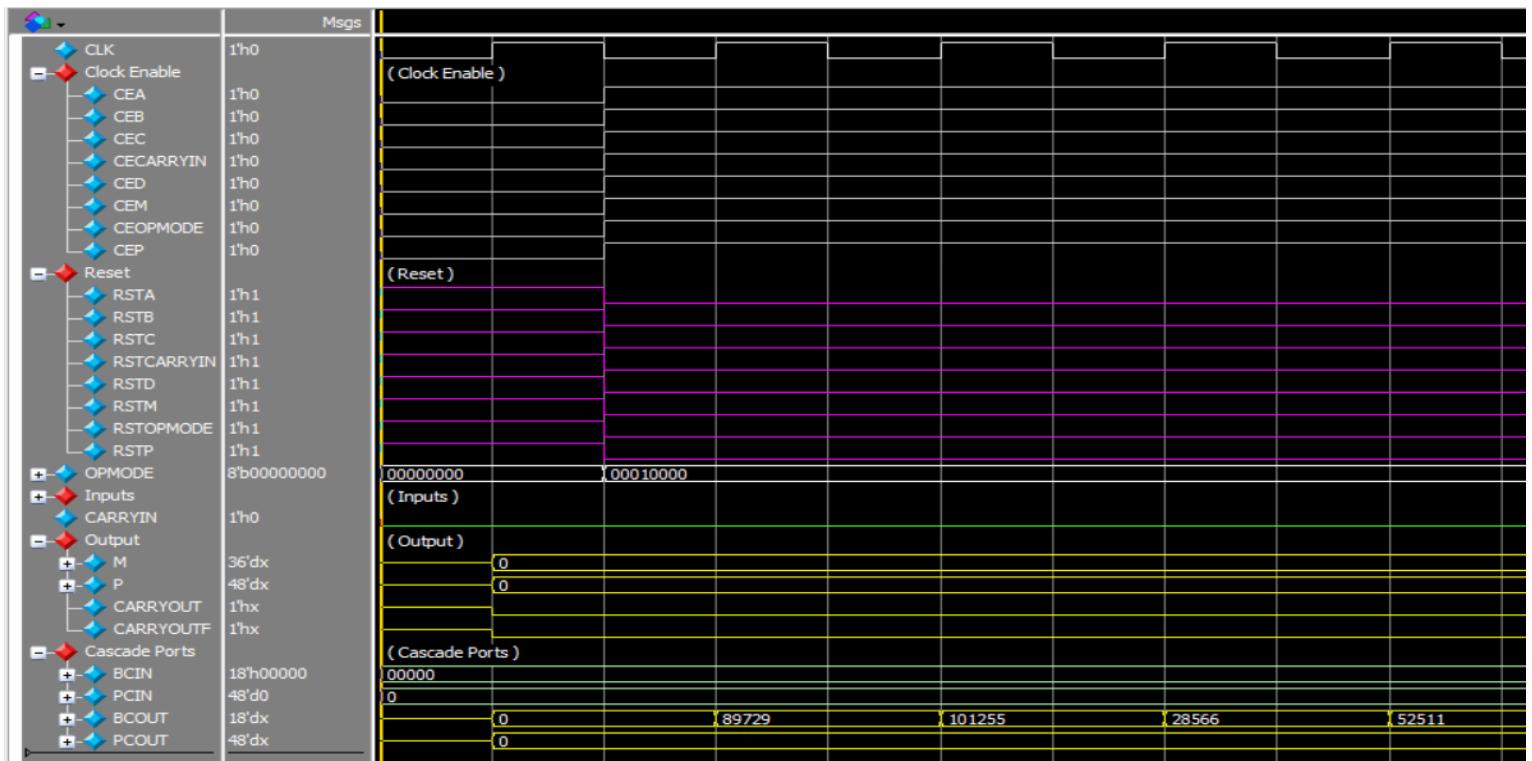
```
88   ///////////////////////
89   //post-adder/subtracter//
90   ///////////////////////
91   OPMODE[1:0] = 2'b11; // mux_X
92   OPMODE[3:2] = 2'b11; // mux_Z
93
94   D = 0;
95   OPMODE[7] = 0; //addition
96   repeat(2) begin
97     repeat(100) begin
98       OPMODE[5] = $random;
99       D[11:0] = $random;
100      A = $random;
101      B = $random;
102      C = $random;
103      @(negedge CLK);
104    end
105    OPMODE[7] = 1; //subtraction
106  end
107
108 ///////////////////
109 //accumulator// 
110 //////////////////
111
112 //input C accumulation
113 OPMODE[1:0] = 2'b10; // mux_X
114 OPMODE[5] = 0;
115 OPMODE[7] = 0; //addition
116 RSTP = 1;
117 RSTCARRYIN = 1;
118 @(negedge CLK);
119 RSTP = 0;
120 RSTCARRYIN = 0;
121 repeat(100) begin
122   C = $random;
123   @(negedge CLK);
124 end
125
126 //cascade P accumulation
127 OPMODE[3:2] = 2'b01; // mux_Z
128 RSTP = 1;
129 RSTCARRYIN = 1;
130 @(negedge CLK);
131 RSTP = 0;
132 RSTCARRYIN = 0;
133 repeat(100) begin
134   PCIN = $random;
135   @(negedge CLK);
136 end
137
138 $stop;
139 end
140 endmodule
```

3. Do file

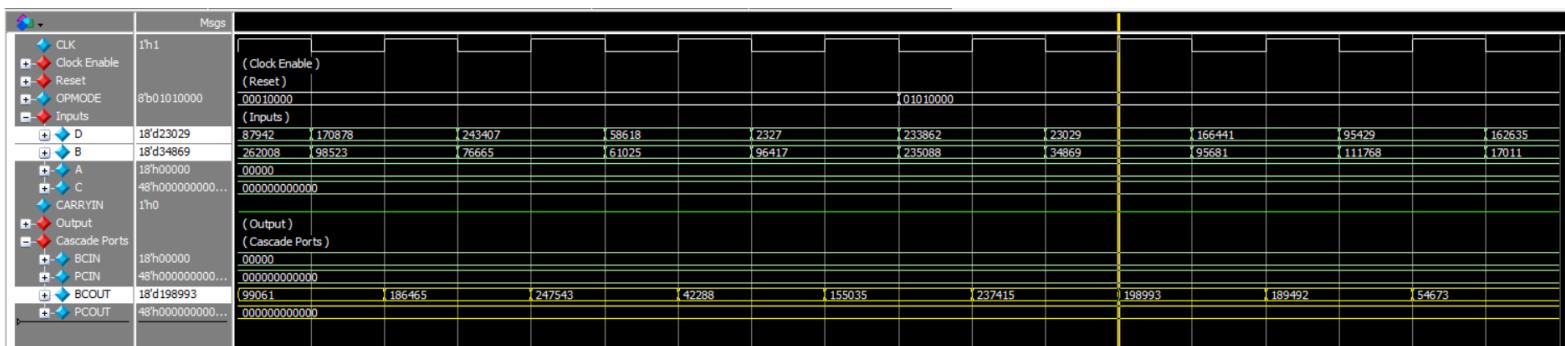
```
Digital Design - DSP48A1_do.do

1 vlib work
2 vlog mux_with_reg.v DSP48A1.v DSP48A1_tb.v
3 vsim -voptargs=+acc work.DSP48A1_tb
4 add wave -color White CLK
5 add wave -expand -group {Clock Enable} -color Gray80 CEA
6 add wave -expand -group {Clock Enable} -color Gray80 CEB
7 add wave -expand -group {Clock Enable} -color Gray80 CEC
8 add wave -expand -group {Clock Enable} -color Gray80 CECARRYIN
9 add wave -expand -group {Clock Enable} -color Gray80 CED
10 add wave -expand -group {Clock Enable} -color Gray80 CEM
11 add wave -expand -group {Clock Enable} -color Gray80 CEOPMODE
12 add wave -expand -group {Clock Enable} -color Gray80 CEP
13 add wave -expand -group Reset -color Magenta RSTA
14 add wave -expand -group Reset -color Magenta RSTB
15 add wave -expand -group Reset -color Magenta RSTC
16 add wave -expand -group Reset -color Magenta RSTCARRYIN
17 add wave -expand -group Reset -color Magenta RSTD
18 add wave -expand -group Reset -color Magenta RSTM
19 add wave -expand -group Reset -color Magenta RSTOPMODE
20 add wave -expand -group Reset -color Magenta RSTP
21 add wave -color White -radix binary OPMODE
22 quietly virtual function -install /DSP48A1_tb -env /DSP48A1_tb/#INITIAL#53 { &{D, A, B }} D_A_B
23 add wave -expand -group Inputs -radix unsigned D_A_B
24 add wave -expand -group Inputs -radix unsigned D
25 add wave -expand -group Inputs -radix unsigned B
26 add wave -expand -group Inputs -radix unsigned A
27 add wave -expand -group Inputs -radix unsigned C
28 add wave CARRYIN
29 add wave -expand -group Output -color Yellow -radix unsigned M
30 add wave -expand -group Output -color Yellow -radix unsigned P
31 add wave -expand -group Output -color Yellow CARRYOUT
32 add wave -expand -group Output -color Yellow CARRYOUTF
33 add wave -expand -group {Cascade Ports} BCIN
34 add wave -expand -group {Cascade Ports} -radix unsigned PCIN
35 add wave -expand -group {Cascade Ports} -color Yellow -radix unsigned BCOUT
36 add wave -expand -group {Cascade Ports} -color Yellow -radix unsigned PCOUT
37 run -all
```

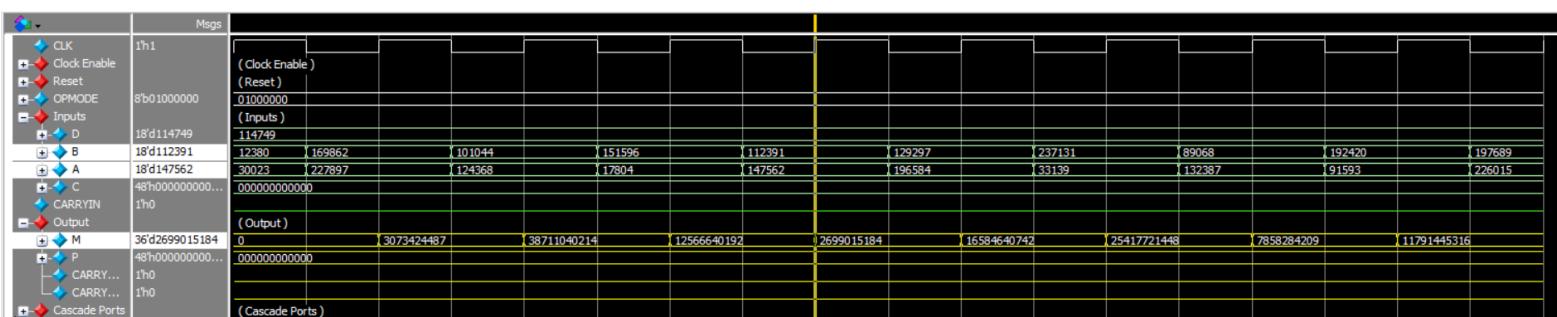
4. QuestaSim Snippets



→ Reset



→ pre-adder/subtractor



→ multiplier

	Msgs												
CLK	1'h1	(Clock Enable)											
Clock Enable		(Reset)											
Reset		01101111	01001111	01101111						01001111	01101111	01001111	01101111
OPMODE	8'b01101111	(Inputs)											
Inputs		D_A_B	54'd982139220...	106288769984918	83417485682806	98213922073212	13870711219674	53691482728323	43997978815750	207351727622320	103247837723401	3614584...	
D	18'd1429	2828	1546	1213	1429	1201	781	640	3017	1502	525		
B	18'd256636	117478	59798	141430	256636	42458	92035	126214	100528	64265	200403		
A	18'd52603	235451	184856	231782	52603	221620	82288	66809	95620	118956	243601		
C	48'd281473767...	28147344...	281472911222281	983049589	281473767927071	281474283514029	281473513342033	281474524134090	1958478825	1811424215	1299708314		
CARRYIN	1'h0	(Output)											
Output		M	36'd32780928260	27660312578	11054019088	32780928260	13499823508	9409541960	7573376080	8432231126	9612487360		
P	48'd534184687...	96256197658403	19439887056056	106286704496544	8341846873295	98212713339627	13870018023048	53690019359701	43997526239185	207353686101145			
CARRYOUT	1'h0	CARRYOUTF	1'h0	(Cascade Ports)									
Cascade Ports													

→ post-adder/subtractor -- addition

	Msgs												
CLK	1'h1	(Clock Enable)											
Clock Enable		(Reset)											
Reset		11101111	11001111	11001111									
OPMODE	8'b11001111	(Inputs)											
D_A_B	54'd133864789...	200205280946813	17220838770644	90394242347813	53751609199460	133864789178987	276924784335042	107585479639846	77820540534192	6012112790351			
D	18'd1947	2910	2505	1315	782	1947	4029	1565	1132	87			
B	18'd64107	157565	188084	28977	166756	64107	153794	806	48560	58191			
A	18'd359277	186552	252145	107309	49508	259277	106041	150675	114795	127862			
C	48'd1442784171	2062460918	1922272909	792118622	605469000	144284171	262558496	-2101901819	-73418505	1514519988			
CARRYIN	1'h0	(Output)											
Output		M	21890346...	49788051008	29394065880	47424440180	3109492893	8255756048	16621470639	31687869554	121444050	5574445200	
P	-48'd535751003...	-5926234...	136338608570501	81450333302925	10926851172920	-90393450228692	-53751003730460	-133863346394816	4549929817118	-1075851541666	-782061...		
CARRYOUT	1'h1	CARRYOUTF	1'h1	(Cascade Ports)									
Cascade Ports													

→ post-adder/subtractor -- subtraction

	Msgs												
CLK	1'h1	(Clock Enable)											
Clock Enable		(Reset)											
Reset		01001110	01001110	01001110									
OPMODE	8'b01001110	(Inputs)											
Inputs		D_A_B	54'd712668517...	71266851782063	1037	165247	18136						
D	18'd1037	281473385543746	281474267640491	711352148	281472883384838	1849150940	281474484765893	281474315580593	466402615	1678280136			
B	18'd163247	5061046882	2960647592	51108235...	281473385543746	281472676473581	281473387825729	28147129449911	281473143650851	281472651705088	281471990576025	28147245...	
A	18'd18136	5062960647592	51108235...	0	281473385543746	281472676473581	281473387825729	28147129449911	281473143650851	281472651705088	281471990576025	28147245...	
C	48'd281472883...	0	281474119664281	281471995857051	281473056886809	281472262360762	281471927805842	281471445350488	281473363512380	281471970823317			
CARRYIN	1'h0	(Output)											
Output		M	36'd2960647592	51108235...	0	281473385543746	281472676473581	281473387825729	28147129449911	281473143650851	281472651705088	281471990576025	28147245...
P	48'd281473385...	51108235...	0	281473385543746	281472676473581	281473387825729	28147129449911	281473143650851	281472651705088	281471990576025	28147245...		
CARRYOUT	1'h0	CARRYOUTF	1'h0	(Cascade Ports)									
Cascade Ports													

→ Accumulator for input C

	Msgs												
CLK	1'h1	(Clock Enable)											
Clock Enable		(Reset)											
Reset		01000110	01000110	01000110									
OPMODE	8'b01000110	(Inputs)											
Inputs		C	48'd281473056...	48'd2960647592	0	281474119664281	281471995857051	281473056886809	281472262360762	281471927805842	281471445350488	281473363512380	281471970823317
D	18'h00000	PCIN	48'd1061029758	0	281474119664281	281472852903426	1061029758	281474182184609	281474642155736	281474494255302	1918161892	281473584021593	28147340...
B	18'd163247	BCIN	48'd281473056...	163247	0	281474119664281	281471995857051	281473056886809	281472262360762	281471927805842	281471445350488	281473363512380	281471970823317
A	18'h00000	PCOUT	48'd281473056...	0	281474119664281	281471995857051	281473056886809	281472262360762	281471927805842	281471445350488	281473363512380	281471970823317	
CARRYIN	1'h0	(Output)											
Output		M	36'd2960647592	51108235...	0	281473385543746	281472676473581	281473387825729	28147129449911	281473143650851	281472651705088	281471990576025	28147245...
P	48'd281473385...	51108235...	0	281473385543746	281472676473581	281473387825729	28147129449911	281473143650851	281472651705088	281471990576025	28147245...		
CARRYOUT	1'h0	CARRYOUTF	1'h0	(Cascade Ports)									
Cascade Ports													

→ Test accumulator for input cascade P

5. Constraint File



Digital Design - DSP48A1_constraints.xdc

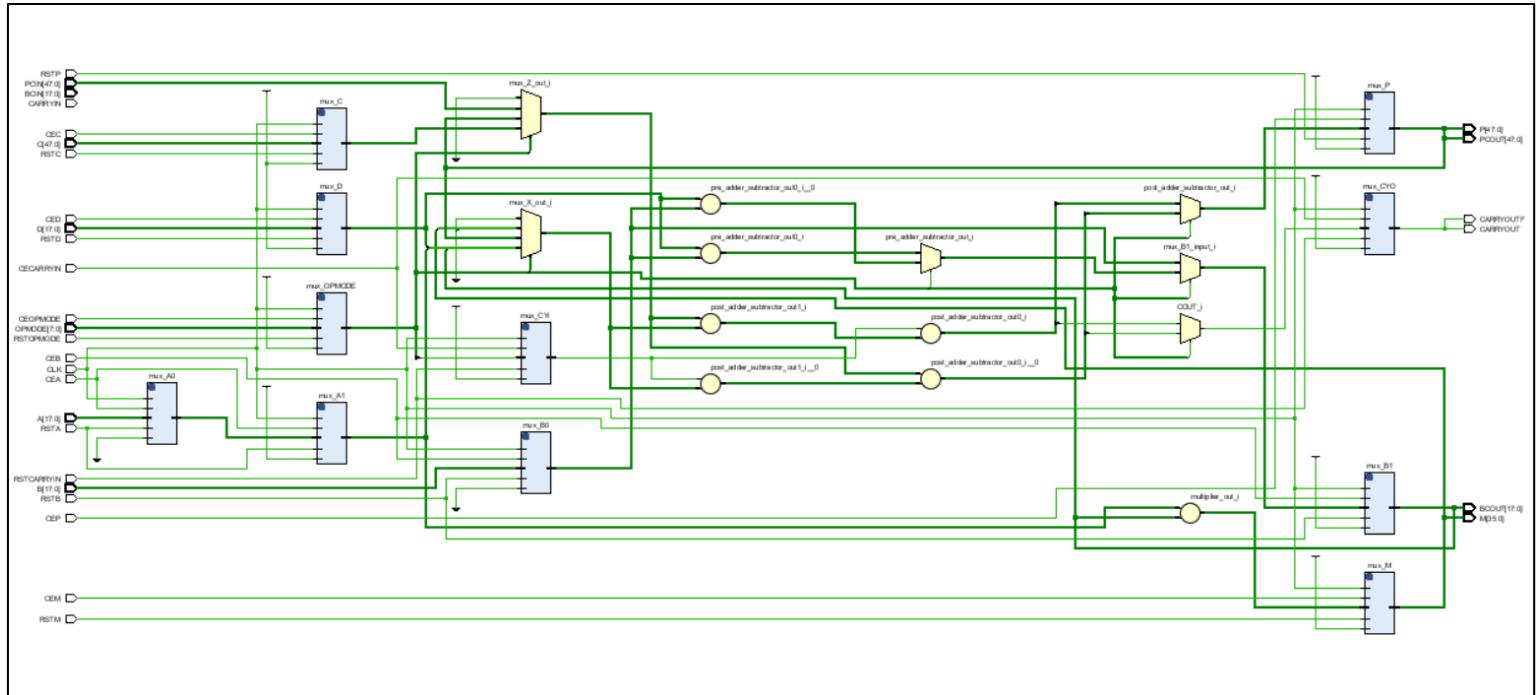
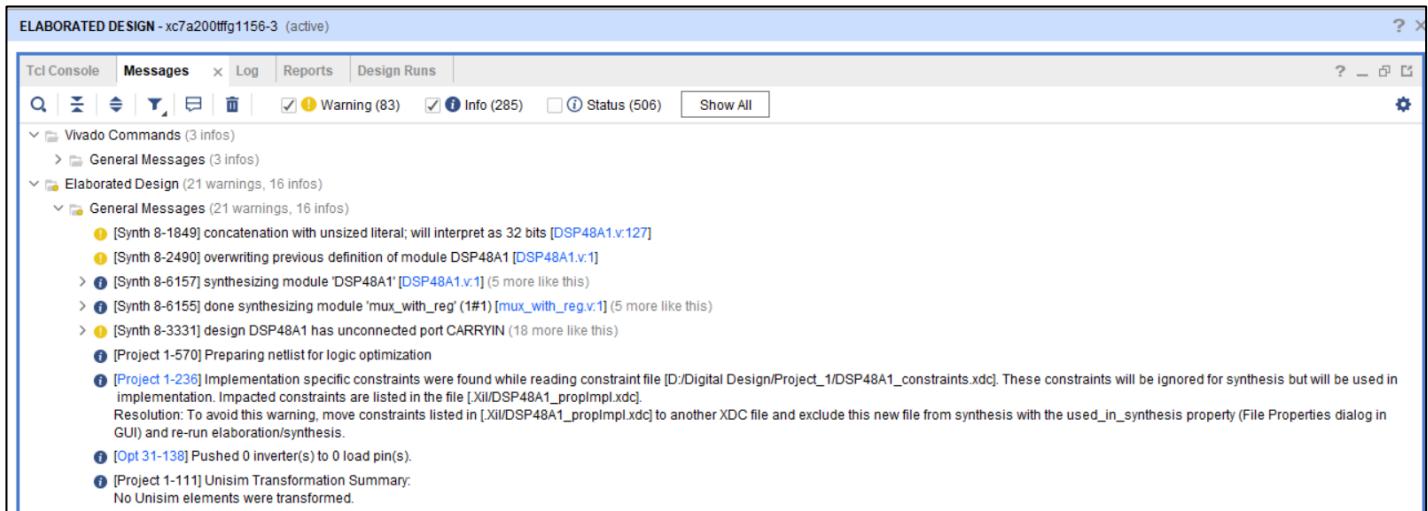
```
1 ## Clock signal
2 set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports CLK]
3 create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports CLK]
4
5 create_debug_core u_il_0 ila
6 set_property ALL_PROBE_SAME_MU true [get_debug_cores u_il_0]
7 set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_il_0]
8 set_property C_ADV_TRIGGER false [get_debug_cores u_il_0]
9 set_property C_DATA_DEPTH 1024 [get_debug_cores u_il_0]
10 set_property C_EN_STRG_QUAL false [get_debug_cores u_il_0]
11 set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_il_0]
12 set_property C_TRIGIN_EN false [get_debug_cores u_il_0]
13 set_property C_TRIGOUT_EN false [get_debug_cores u_il_0]
14 set_property port_width 1 [get_debug_ports u_il_0/clk]
15 connect_debug_port u_il_0/clk [get_nets [list CLK_IBUF_BUFG]]
16 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il_0/probe0]
17 set_property port_width 18 [get_debug_ports u_il_0/probe0]
18 connect_debug_port u_il_0/probe0 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]} {B_IBUF[3]} {B_IBUF[4]}
19 {B_IBUF[5]} {B_IBUF[6]} {B_IBUF[7]} {B_IBUF[8]} {B_IBUF[9]} {B_IBUF[10]} {B_IBUF[11]} {B_IBUF[12]} {B_IBUF[13]}
20 {B_IBUF[14]} {B_IBUF[15]} {B_IBUF[16]} {B_IBUF[17]}]]
21 create_debug_port u_il_0 probe
22 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il_0/probe1]
23 set_property port_width 36 [get_debug_ports u_il_0/probe1]
24 connect_debug_port u_il_0/probe1 [get_nets [list {M_OBUF[0]} {M_OBUF[1]} {M_OBUF[2]} {M_OBUF[3]} {M_OBUF[4]}
25 {M_OBUF[5]} {M_OBUF[6]} {M_OBUF[7]} {M_OBUF[8]} {M_OBUF[9]} {M_OBUF[10]} {M_OBUF[11]} {M_OBUF[12]} {M_OBUF[13]}
26 {M_OBUF[14]} {M_OBUF[15]} {M_OBUF[16]} {M_OBUF[17]} {M_OBUF[18]} {M_OBUF[19]} {M_OBUF[20]} {M_OBUF[21]} {M_OBUF[22]}
27 {M_OBUF[23]} {M_OBUF[24]} {M_OBUF[25]} {M_OBUF[26]} {M_OBUF[27]} {M_OBUF[28]} {M_OBUF[29]} {M_OBUF[30]} {M_OBUF[31]}
28 {M_OBUF[32]} {M_OBUF[33]} {M_OBUF[34]} {M_OBUF[35]}]]
29 create_debug_port u_il_0 probe
30 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il_0/probe2]
31 set_property port_width 18 [get_debug_ports u_il_0/probe2]
32 connect_debug_port u_il_0/probe2 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]} {A_IBUF[3]} {A_IBUF[4]}
33 {A_IBUF[5]} {A_IBUF[6]} {A_IBUF[7]} {A_IBUF[8]} {A_IBUF[9]} {A_IBUF[10]} {A_IBUF[11]} {A_IBUF[12]} {A_IBUF[13]}
34 {A_IBUF[14]} {A_IBUF[15]} {A_IBUF[16]} {A_IBUF[17]}]]
35 create_debug_port u_il_0 probe
36 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il_0/probe3]
37 set_property port_width 48 [get_debug_ports u_il_0/probe3]
38 connect_debug_port u_il_0/probe3 [get_nets [list {C_IBUF[0]} {C_IBUF[1]} {C_IBUF[2]} {C_IBUF[3]} {C_IBUF[4]}
39 {C_IBUF[5]} {C_IBUF[6]} {C_IBUF[7]} {C_IBUF[8]} {C_IBUF[9]} {C_IBUF[10]} {C_IBUF[11]} {C_IBUF[12]} {C_IBUF[13]}
40 {C_IBUF[14]} {C_IBUF[15]} {C_IBUF[16]} {C_IBUF[17]} {C_IBUF[18]} {C_IBUF[19]} {C_IBUF[20]} {C_IBUF[21]} {C_IBUF[22]}
41 {C_IBUF[23]} {C_IBUF[24]} {C_IBUF[25]} {C_IBUF[26]} {C_IBUF[27]} {C_IBUF[28]} {C_IBUF[29]} {C_IBUF[30]} {C_IBUF[31]}
42 {C_IBUF[32]} {C_IBUF[33]} {C_IBUF[34]} {C_IBUF[35]} {C_IBUF[36]} {C_IBUF[37]} {C_IBUF[38]} {C_IBUF[39]} {C_IBUF[40]}
43 {C_IBUF[41]} {C_IBUF[42]} {C_IBUF[43]} {C_IBUF[44]} {C_IBUF[45]} {C_IBUF[46]} {C_IBUF[47]}]]
44 create_debug_port u_il_0 probe
45 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il_0/probe4]
46 set_property port_width 48 [get_debug_ports u_il_0/probe4]
47 connect_debug_port u_il_0/probe4 [get_nets [list {PCOUT_OBUF[0]} {PCOUT_OBUF[1]} {PCOUT_OBUF[2]} {PCOUT_OBUF[3]}
48 {PCOUT_OBUF[4]} {PCOUT_OBUF[5]} {PCOUT_OBUF[6]} {PCOUT_OBUF[7]} {PCOUT_OBUF[8]} {PCOUT_OBUF[9]} {PCOUT_OBUF[10]}
49 {PCOUT_OBUF[11]} {PCOUT_OBUF[12]} {PCOUT_OBUF[13]} {PCOUT_OBUF[14]} {PCOUT_OBUF[15]} {PCOUT_OBUF[16]} {PCOUT_OBUF[17]}
50 {PCOUT_OBUF[18]} {PCOUT_OBUF[19]} {PCOUT_OBUF[20]} {PCOUT_OBUF[21]} {PCOUT_OBUF[22]} {PCOUT_OBUF[23]} {PCOUT_OBUF[24]}
51 {PCOUT_OBUF[25]} {PCOUT_OBUF[26]} {PCOUT_OBUF[27]} {PCOUT_OBUF[28]} {PCOUT_OBUF[29]} {PCOUT_OBUF[30]} {PCOUT_OBUF[31]}
52 {PCOUT_OBUF[32]} {PCOUT_OBUF[33]} {PCOUT_OBUF[34]} {PCOUT_OBUF[35]} {PCOUT_OBUF[36]} {PCOUT_OBUF[37]} {PCOUT_OBUF[38]}
53 {PCOUT_OBUF[39]} {PCOUT_OBUF[40]} {PCOUT_OBUF[41]} {PCOUT_OBUF[42]} {PCOUT_OBUF[43]} {PCOUT_OBUF[44]} {PCOUT_OBUF[45]}
54 {PCOUT_OBUF[46]} {PCOUT_OBUF[47]}]]
55 create_debug_port u_il_0 probe
56 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il_0/probe5]
57 set_property port_width 8 [get_debug_ports u_il_0/probe5]
58 connect_debug_port u_il_0/probe5 [get_nets [list {OPMODE_IBUF[0]} {OPMODE_IBUF[1]} {OPMODE_IBUF[2]} {OPMODE_IBUF[3]}
59 {OPMODE_IBUF[4]} {OPMODE_IBUF[5]} {OPMODE_IBUF[6]} {OPMODE_IBUF[7]}]]
60 create_debug_port u_il_0 probe
61 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il_0/probe6]
62 set_property port_width 18 [get_debug_ports u_il_0/probe6]
63 connect_debug_port u_il_0/probe6 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]} {BCOUT_OBUF[2]} {BCOUT_OBUF[3]}
64 {BCOUT_OBUF[4]} {BCOUT_OBUF[5]} {BCOUT_OBUF[6]} {BCOUT_OBUF[7]} {BCOUT_OBUF[8]} {BCOUT_OBUF[9]} {BCOUT_OBUF[10]}
65 {BCOUT_OBUF[11]} {BCOUT_OBUF[12]} {BCOUT_OBUF[13]} {BCOUT_OBUF[14]} {BCOUT_OBUF[15]} {BCOUT_OBUF[16]} {BCOUT_OBUF[17]}]]
66 create_debug_port u_il_0 probe
67 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il_0/probe7]
68 set_property port_width 18 [get_debug_ports u_il_0/probe7]
69 connect_debug_port u_il_0/probe7 [get_nets [list {D_IBUF[0]} {D_IBUF[1]} {D_IBUF[2]} {D_IBUF[3]} {D_IBUF[4]} {D_IBUF[5]}
70 {D_IBUF[6]} {D_IBUF[7]} {D_IBUF[8]} {D_IBUF[9]} {D_IBUF[10]} {D_IBUF[11]} {D_IBUF[12]} {D_IBUF[13]} {D_IBUF[14]} {D_IBUF[15]}
71 {D_IBUF[16]} {D_IBUF[17]}]]
72 create_debug_port u_il_0 probe
73 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il_0/probe8]
74 set_property port_width 48 [get_debug_ports u_il_0/probe8]
75 connect_debug_port u_il_0/probe8 [get_nets [list {PCIN_IBUF[0]} {PCIN_IBUF[1]} {PCIN_IBUF[2]} {PCIN_IBUF[3]} {PCIN_IBUF[4]}
76 {PCIN_IBUF[5]} {PCIN_IBUF[6]} {PCIN_IBUF[7]} {PCIN_IBUF[8]} {PCIN_IBUF[9]} {PCIN_IBUF[10]} {PCIN_IBUF[11]} {PCIN_IBUF[12]}
77 {PCIN_IBUF[13]} {PCIN_IBUF[14]} {PCIN_IBUF[15]} {PCIN_IBUF[16]} {PCIN_IBUF[17]} {PCIN_IBUF[18]} {PCIN_IBUF[19]} {PCIN_IBUF[20]}
78 {PCIN_IBUF[21]} {PCIN_IBUF[22]} {PCIN_IBUF[23]} {PCIN_IBUF[24]} {PCIN_IBUF[25]} {PCIN_IBUF[26]} {PCIN_IBUF[27]} {PCIN_IBUF[28]}
79 {PCIN_IBUF[29]} {PCIN_IBUF[30]} {PCIN_IBUF[31]} {PCIN_IBUF[32]} {PCIN_IBUF[33]} {PCIN_IBUF[34]} {PCIN_IBUF[35]} {PCIN_IBUF[36]}
80 {PCIN_IBUF[37]} {PCIN_IBUF[38]} {PCIN_IBUF[39]} {PCIN_IBUF[40]} {PCIN_IBUF[41]} {PCIN_IBUF[42]} {PCIN_IBUF[43]} {PCIN_IBUF[44]}
81 {PCIN_IBUF[45]} {PCIN_IBUF[46]} {PCIN_IBUF[47]}]]
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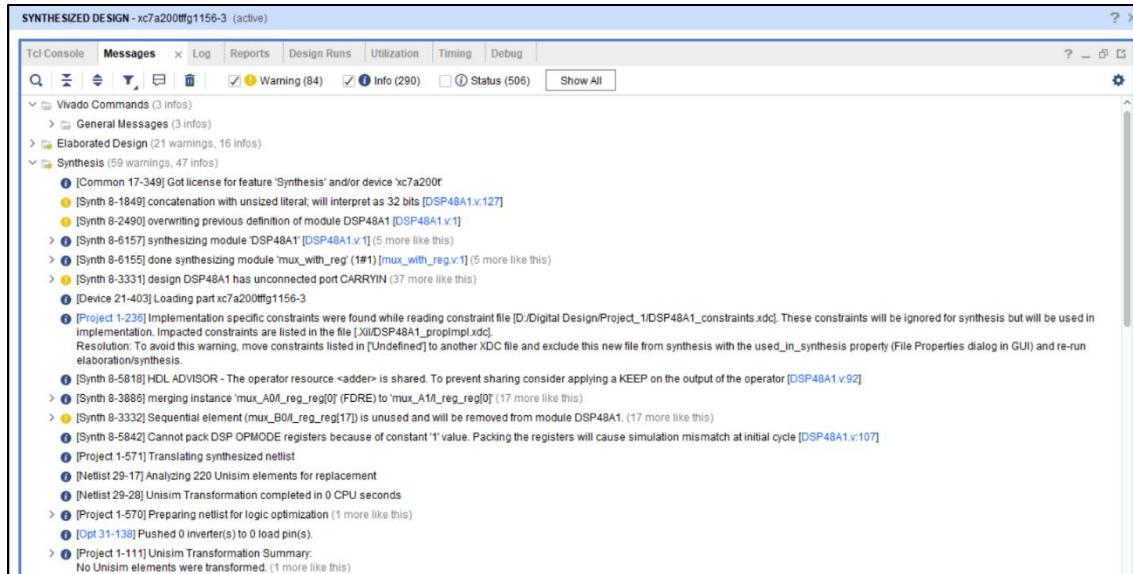
82 create_debug_port u_ila_0 probe
83 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
84 set_property port_width 1 [get_debug_ports u_ila_0/probe9]
85 connect_debug_port u_ila_0/probe9 [get_nets [list CARRYOUTF_OBUF]]
86 create_debug_port u_ila_0 probe
87 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe10]
88 set_property port_width 1 [get_debug_ports u_ila_0/probe10]
89 connect_debug_port u_ila_0/probe10 [get_nets [list CEA_IBUF]]
90 create_debug_port u_ila_0 probe
91 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
92 set_property port_width 1 [get_debug_ports u_ila_0/probe11]
93 connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
94 create_debug_port u_ila_0 probe
95 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
96 set_property port_width 1 [get_debug_ports u_ila_0/probe12]
97 connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
98 create_debug_port u_ila_0 probe
99 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
100 set_property port_width 1 [get_debug_ports u_ila_0/probe13]
101 connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
102 create_debug_port u_ila_0 probe
103 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
104 set_property port_width 1 [get_debug_ports u_ila_0/probe14]
105 connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
106 create_debug_port u_ila_0 probe
107 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
108 set_property port_width 1 [get_debug_ports u_ila_0/probe15]
109 connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
110 create_debug_port u_ila_0 probe
111 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
112 set_property port_width 1 [get_debug_ports u_ila_0/probe16]
113 connect_debug_port u_ila_0/probe16 [get_nets [list CEOPMODE_IBUF]]
114 create_debug_port u_ila_0 probe
115 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
116 set_property port_width 1 [get_debug_ports u_ila_0/probe17]
117 connect_debug_port u_ila_0/probe17 [get_nets [list CEP_IBUF]]
118 create_debug_port u_ila_0 probe
119 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
120 set_property port_width 1 [get_debug_ports u_ila_0/probe18]
121 connect_debug_port u_ila_0/probe18 [get_nets [list CLK_IBUF]]
122 create_debug_port u_ila_0 probe
123 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
124 set_property port_width 1 [get_debug_ports u_ila_0/probe19]
125 connect_debug_port u_ila_0/probe19 [get_nets [list RSTA_IBUF]]
126 create_debug_port u_ila_0 probe
127 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
128 set_property port_width 1 [get_debug_ports u_ila_0/probe20]
129 connect_debug_port u_ila_0/probe20 [get_nets [list RSTB_IBUF]]
130 create_debug_port u_ila_0 probe
131 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
132 set_property port_width 1 [get_debug_ports u_ila_0/probe21]
133 connect_debug_port u_ila_0/probe21 [get_nets [list RSTC_IBUF]]
134 create_debug_port u_ila_0 probe
135 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
136 set_property port_width 1 [get_debug_ports u_ila_0/probe22]
137 connect_debug_port u_ila_0/probe22 [get_nets [list RSTCARRYIN_IBUF]]
138 create_debug_port u_ila_0 probe
139 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
140 set_property port_width 1 [get_debug_ports u_ila_0/probe23]
141 connect_debug_port u_ila_0/probe23 [get_nets [list RSTOPMODE_IBUF]]
142 create_debug_port u_ila_0 probe
143 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
144 set_property port_width 1 [get_debug_ports u_ila_0/probe24]
145 connect_debug_port u_ila_0/probe24 [get_nets [list RSTM_IBUF]]
146 create_debug_port u_ila_0 probe
147 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
148 set_property port_width 1 [get_debug_ports u_ila_0/probe25]
149 connect_debug_port u_ila_0/probe25 [get_nets [list RSTD_IBUF]]
150 create_debug_port u_ila_0 probe
151 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
152 set_property port_width 1 [get_debug_ports u_ila_0/probe26]
153 connect_debug_port u_ila_0/probe26 [get_nets [list RSTP_IBUF]]
154 set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
155 set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
156 set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
157 connect_debug_port dbg_hub/clk [get_nets CLK_IBUF_BUFG]
158

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6. Elaboration



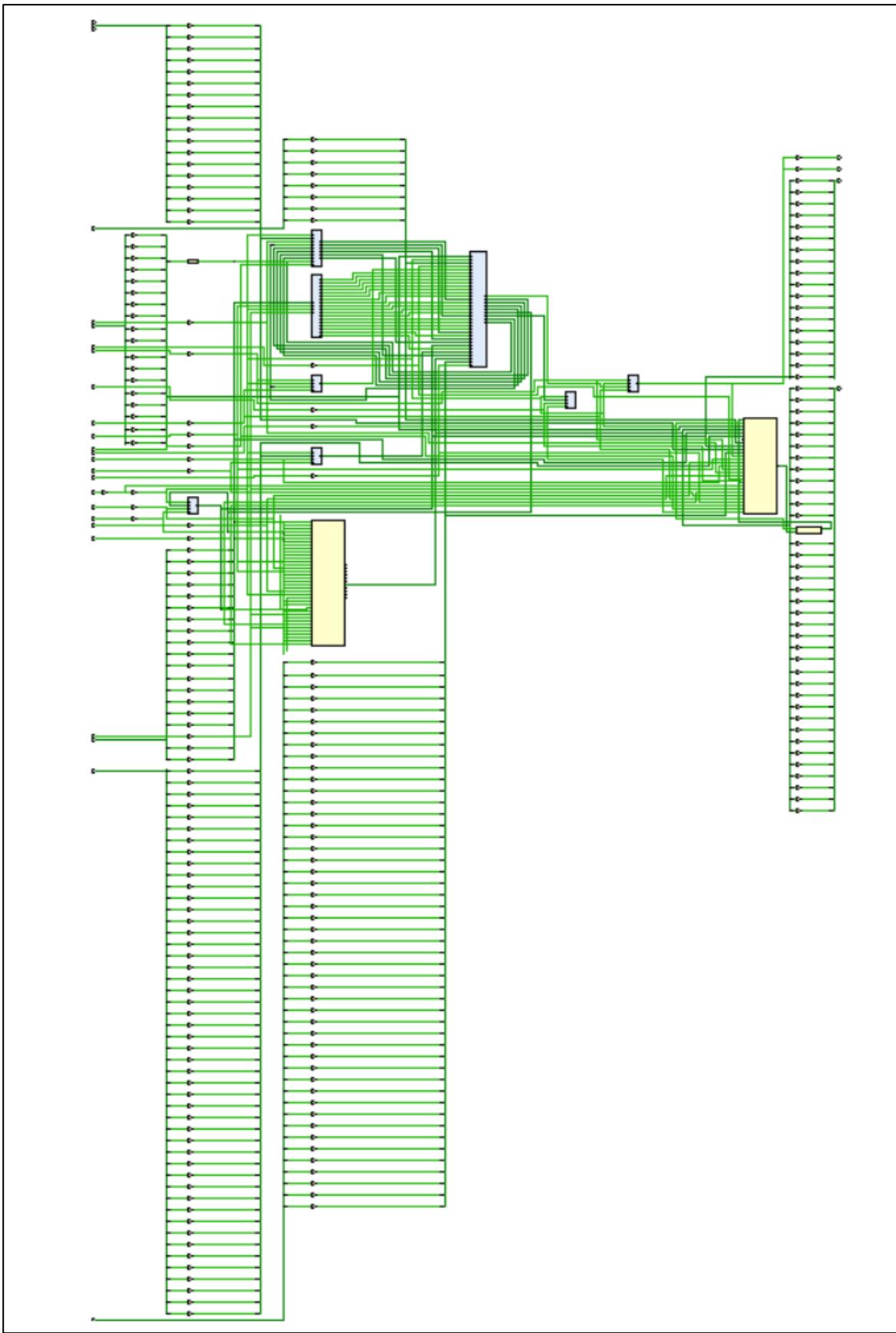
7. Synthesis



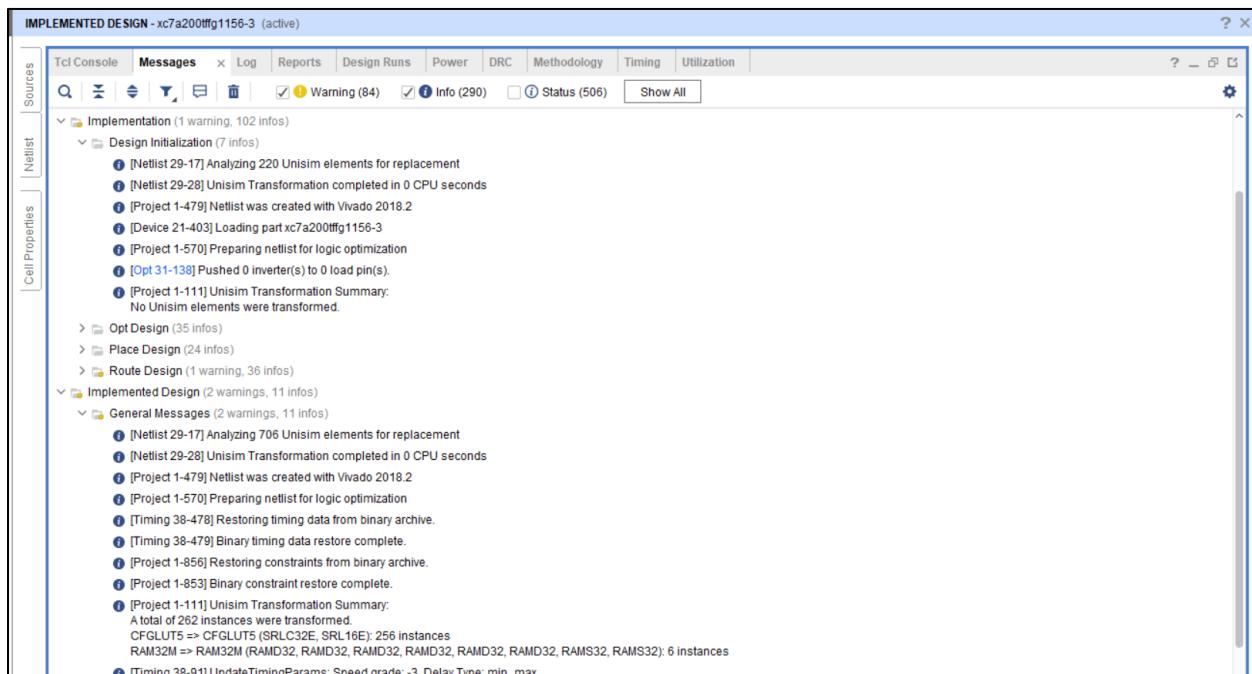
Name	1	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N DSP48A1		255	160	1	327	1
dbg_hub (dbg_hub_CV)		0	0	0	0	0
mux_A1 (mux_with_re...		0	18	0	0	0
mux_B1 (mux_with_re...		0	18	0	0	0
mux_C (mux_with_reg...		0	48	0	0	0
mux_CYI (mux_with_re...		1	1	0	0	0
mux_CYO (mux_with_r...		0	1	0	0	0
mux_D (mux_with_reg...		0	18	0	0	0
mux_OPMODE (mux_...		253	8	0	0	0
mux_P (mux_with_reg...		0	48	0	0	0
u_il_0 (u_il_0_CV)		0	0	0	0	0

Design Timing Summary					
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.213 ns	Worst Hold Slack (WHS):	0.182 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	87	Total Number of Endpoints:	87	Total Number of Endpoints:	162

All user specified timing constraints are met.



8. Implementation



Name	1	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSP s (740)	Bonded IOB (500)	BUFGCTRL (32)	BSCAN2 (4)
N DSP48A1		2728	4225	97	12	1571	2254	474	1543	8	1	327	2	1
> dbg_hub (dbg_hub)		476	727	0	0	263	452	24	305	0	0	0	1	1
mux_A1 (mux_with_reg...)	0	18	0	0	6	0	0	0	0	0	0	0	0	0
mux_B1 (mux_with_reg...)	0	18	0	0	7	0	0	0	0	0	0	0	0	0
mux_C (mux_with_reg...)	0	48	0	0	17	0	0	0	0	0	0	0	0	0
mux_CY1 (mux_with_re...	1	1	0	0	1	1	0	0	1	0	0	0	0	0
mux_CYO (mux_with_r...	0	1	0	0	1	0	0	0	0	0	0	0	0	0
mux_D (mux_with_reg...)	0	18	0	0	9	0	0	0	0	0	0	0	0	0
mux_OPMODE (mux_w...	253	8	0	0	79	253	0	0	0	0	0	0	0	0
mux_P (mux_with_reg...)	0	48	0	0	12	0	0	0	0	0	0	0	0	0
> u_ilia_0 (u_ilia_0)	1997	3338	97	12	1222	1547	450	1210	8	0	0	0	0	0

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.116 ns	Worst Hold Slack (WHS): 0.016 ns	Worst Pulse Width Slack (WPWS): 3.950 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 8058	Total Number of Endpoints: 8042	Total Number of Endpoints: 5136

All user specified timing constraints are met.

