UVM Synchronous FIFO Project

by

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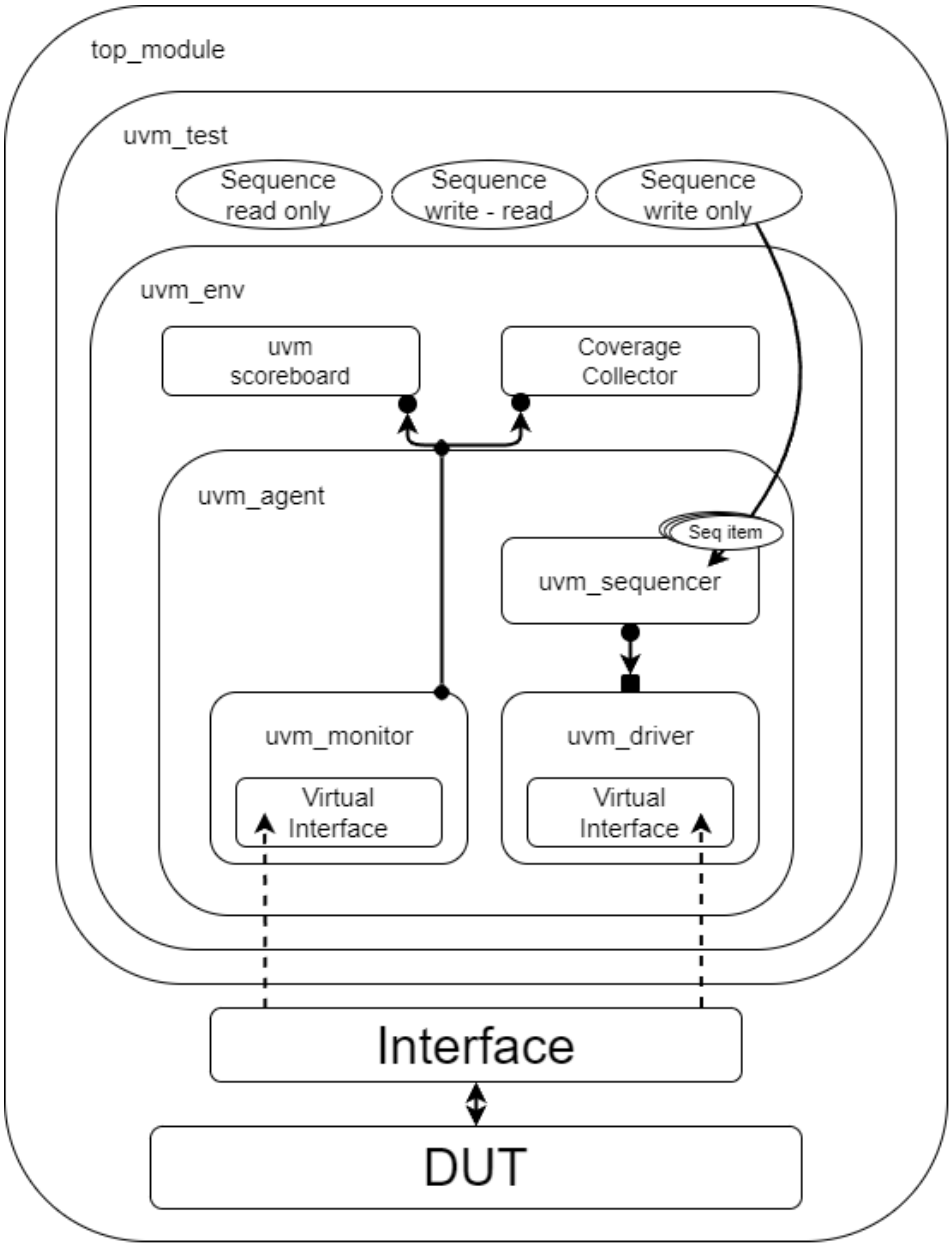
➔ Verification plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
RESET	When the reset is asserted, the output UnderFlow, OverFlow, and wr_ack should be low	Directed at the start of the sim, then randomized with constraint that drive the reset to be off most of the simulation time.	-	A checker and Immediate assertion to check for the async reset functionality
WRITE_1	When the wr_en is asserted and if the fifo is not full, the data_in should be stored in the fifo, the output wr_ack should be high	Randomization under constraints on the wr_en signal to be on 70% of the time by default	cross coverage to cover the wr_ack, and full flags with wr_en and rd_en	A cheker and a concurrent assertion to check the wr_ack flag and Immediate assertion to check full flag
WRITE_2	When the wr_en is asserted and the full flag is high, the data_in will not be writen, the output overflow flag should be high	Randomization under constraints on the wr_en signal to be on 70% of the time by default	cross coverage to cover the overflow with wr_en and rd_en	A cheker and a concurrent assertion to check the overflow signal
WRITE_3	When fifo is almost full (only one empty space inside the fifo), the output almostfull flag should be high	Randomization under constraints on the wr_en signal to be on 70% of the time by default	cross coverage to cover the almostfull flag with wr_en and rd_en	A cheker and a Immediate assertion to check the almostfull flag
READ_1	When the rd_en is asserted, the output data_out should be shown the value stored in the fifo if it was not empty, the output underflow should be high if the fifo is empty	Randomization under constraints on the rd_en signal to be on 30% of the time by default	cross coverage to cover empty flag with wr_en and rd_en	A cheker to check the data_out and a Immediate assertion to check the empty flag
READ_2	When the rd_en is asserted and the empty flag is high, the output underflow should be high	Randomization under constraints on the rd_en signal to be on 30% of the time by default	cross coverage to cover the underflow flag with wr_en and rd_en	A cheker and a concurrent assertion to check the underflow flag
READ_3	When fifo is almost empty(only one value inside the fifo), the output almostempty flag should be high	Randomization under constraints on the rd_en signal to be on 30% of the time by default	cross coverage to cover the almost empty flag with wr_en and rd_en	A cheker and a Immediate assertion to check the almost empty flag
WRITE_READ_1	When the wr_en and rd_en are asserted the and full flag is high, the fifo should preform the read operation only, the internal count should decrease	Randomization under constraints on the wr_en and rd_en signals to be on 70% and 30%	cross coverage to cover full flag with wr_en and rd_en	concurrent assertion to check the result
WRITE_READ_2	When the wr_en and rd_en are asserted the and empty flag is high, the fifo should preform the write operation only, the internal count should increase	Randomization under constraints on the wr_en and rd_en signals to be on 70% and 30%	cross coverage to cover empty flag with wr_en and rd_en	concurrent assertion to check the result
WRITE_READ_3	When the wr_en and rd_en are asserted the and full/empty flag are low, the fifo should preform the write and read operation in the same time, the internal count should remain the same	Randomization under constraints on the wr_en and rd_en signals to be on 70% and 30%	-	concurrent assertion to check the result

➔ Assertions table

Feature	Assertion
Whenever the FIFO has no empty space, full flag should be high	if(count == FIFO_DEPTH) assert (full);
Whenever the FIFO has only one empty space, almostfull flag should be high	if(count == FIFO_DEPTH-1) assert (almostfull);
Whenever the FIFO has no item, empty flag should be high	if(!count) assert (empty);
Whenever the FIFO has only one item, almostempty flag should be high	if(count == 1) assert (almostempty);
Whenever wr_en is asserted and the FIFO is not full, wr_ack flag should be high	@(posedge clk) (wr_en && !full) |=> wr_ack;
Whenever wr_en is asserted and the FIFO is full, overflow flag should be high	@(posedge clk) (wr_en && full) |=> overflow;
Whenever rd_en is asserted and the FIFO is empty, underflow flag should be high	@(posedge clk) (rd_en && empty) |=> underflow;
Whenever wr_en is asserted and rd_en is deasserted and the FIFO is not full, internal counter should increase	@(posedge clk) ((wr_en && !full) && (!rd_en || empty)) |=> count == ($past(count) + 1);
Whenever wr_en is deasserted and rd_en is asserted and the FIFO is not empty, internal counter should decrease	@(posedge clk) ((rd_en && !empty) && (!wr_en || full)) |=> count == ($past(count) - 1);
Whenever wr_en and rd_en asserted in the same time and the FIFO neither full nor empty, internal counter still the same	@(posedge clk) (wr_en && rd_en && !full && !empty) |=> count == $past(count);

➔ UVM Structure Diagram



➔ UVM Structure Details

TOP:

- Instantiate the DUT and interface.
- Bind the assertion with the DUT.
- Store the interface as virtual interface inside the db.
- Start the test.

Test:

- Get the virtual interface from the db and store it again as a config obj.
- Build the sequences and the env.
- Start the sequences.

Env:

- Build the agent, scoreboard, coverage collector.
- Connect the scoreboard and coverage collector analysis export with the agent analysis port.

Monitor, Scoreboard and Coverage collector:

- After the monitor sample the interface data at the negative edge of the clk it broadcasts it as an obj. of the seq_item using the analysis port to the scoreboard and coverage collector.
- The scoreboard and coverage collector store the received date initially in there internal FIFO.

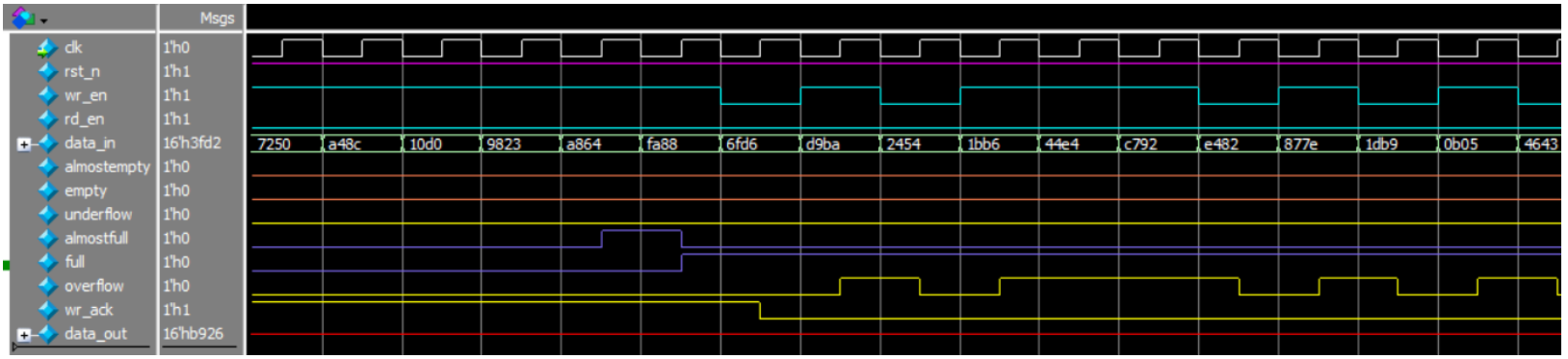
Agent:

- Build sequencer, driver, and monitor
- Get the config obj and use it the connect the monitor and driver with the virtual interface.
- connect the driver port with the sequencer export.
- connect the monitor analysis port with the agent analysis port.

Driver, Sequence and Sequencer:

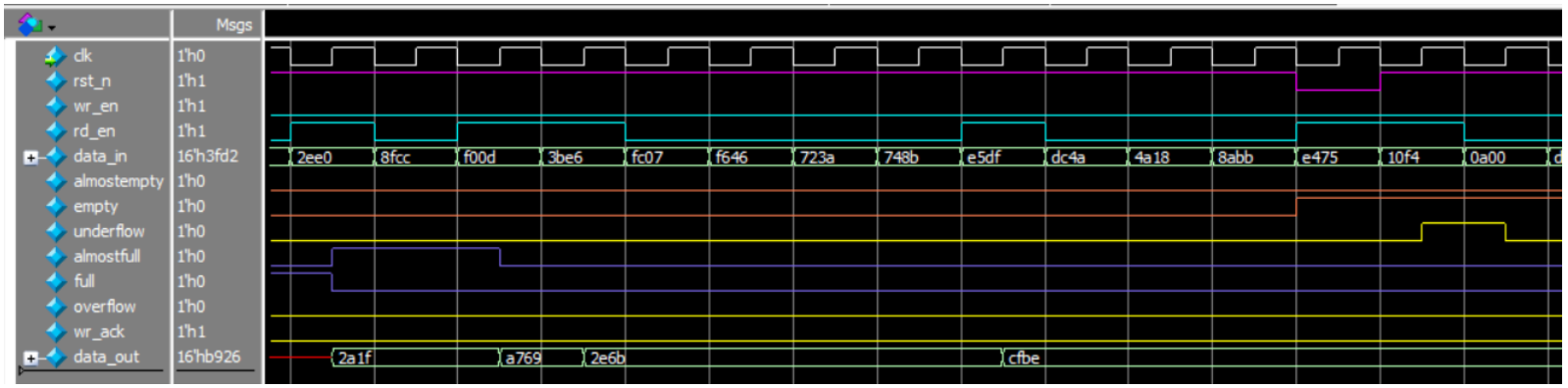
- After the Test start a sequence it sends its data to the sequencer. And the sequence waits until the date is used before sending again.
- The driver start by pulling the data from the sequencer, and use it to driver the DUT after the data is used the driver send to the sequencer that it finished and start pulling new data again

➔ Waveform



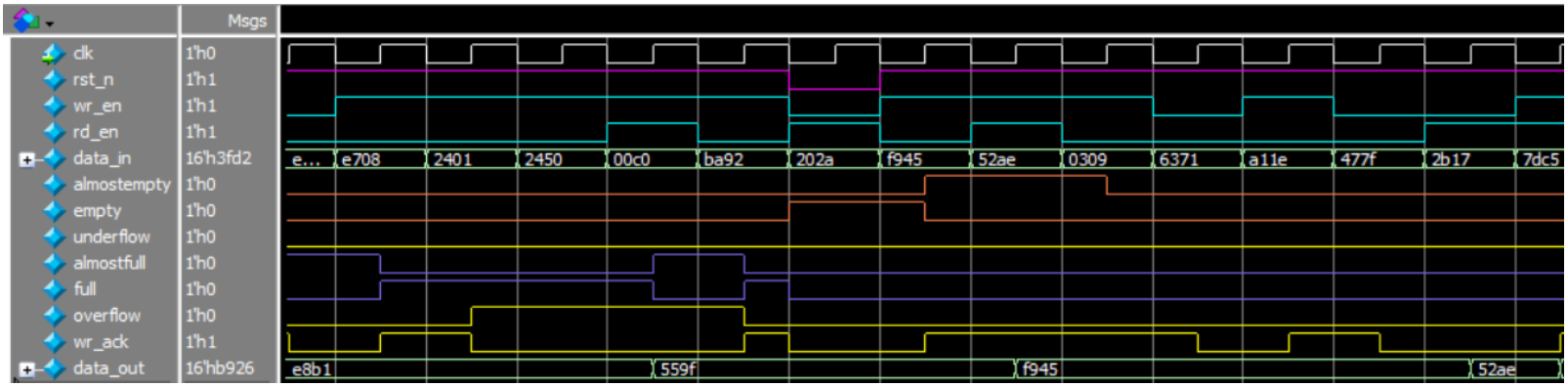
Write only sequence

wr_en = random, rd_en = 0



Read only sequence

wr_en = 0, rd_en = random



Read_Write sequence

wr_en = random, rd_en = random

➔ Bugs

- Add: reset for wr_ack, overflow and underflow
- Move: overflow, and underflow flags control outside the else branch
- Fix: almostfull flag to be high only when ((count ==FIFO_DEPTH - 1))
- ADD: two missing cases for the counter
  -re_en =1, wr_en = 1, empty = 1 => count = count +1
  -re_en =1, wr_en = 1, full = 1 => count = count -1
- Fix: Changing underflow flag from comb. to seq.

➔ Code Coverage

```
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        27        27         0   100.00%

================================Branch Details================================

Branch Coverage for instance /top/DUT
```

```
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      27        27         0   100.00%

================================Statement Details========================

Statement Coverage for instance /top/DUT --
```

```
================================================================================
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         86        86         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /top/FIFO_if --
```

➔ Functional Coverage

Digital Verification - coverage_rpt.txt

```
COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------
 TYPE /FIFO_cover_pkg/FIFO_cover/cvr                96.42%        100          -    Uncovered
    covered/total bins:                                 90         98          -
    missing/total bins:                                  8         98          -
    % Hit:                                          91.83%        100          -
    Coverpoint #seq_item.wr_en__0#                 100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                    9588          1          -    Covered
        bin auto[1]                                    8412          1          -    Covered
    Coverpoint #seq_item.rd_en__1#                 100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   14516          1          -    Covered
        bin auto[1]                                    3484          1          -    Covered
    Coverpoint #seq_item.underflow__2#             100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   16207          1          -    Covered
        bin auto[1]                                    1793          1          -    Covered
    Coverpoint #seq_item.wr_en__3#                 100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                    9588          1          -    Covered
        bin auto[1]                                    8412          1          -    Covered
    Coverpoint #seq_item.rd_en__4#                 100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   14516          1          -    Covered
        bin auto[1]                                    3484          1          -    Covered
    Coverpoint #seq_item.almostempty__5#           100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   17561          1          -    Covered
        bin auto[1]                                     431          1          -    Covered
    Coverpoint #seq_item.wr_en__6#                 100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                    9588          1          -    Covered
        bin auto[1]                                    8412          1          -    Covered
    Coverpoint #seq_item.rd_en__7#                 100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   14516          1          -    Covered
        bin auto[1]                                    3484          1          -    Covered
    Coverpoint #seq_item.almostfull__8#            100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   16285          1          -    Covered
        bin auto[1]                                    1707          1          -    Covered
    Coverpoint #seq_item.wr_en__9#                 100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                    9588          1          -    Covered
        bin auto[1]                                    8412          1          -    Covered
    Coverpoint #seq_item.rd_en__10#                100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   14516          1          -    Covered
        bin auto[1]                                    3484          1          -    Covered
    Coverpoint #seq_item.empty__11#                100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   11610          1          -    Covered
        bin auto[1]                                    6382          1          -    Covered
    Coverpoint #seq_item.wr_en__12#                100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                    9588          1          -    Covered
        bin auto[1]                                    8412          1          -    Covered
    Coverpoint #seq_item.rd_en__13#                100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   14516          1          -    Covered
        bin auto[1]                                    3484          1          -    Covered
    Coverpoint #seq_item.overflow__14#             100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   13067          1          -    Covered
        bin auto[1]                                    4933          1          -    Covered
    Coverpoint #seq_item.wr_en__15#                100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                    9588          1          -    Covered
        bin auto[1]                                    8412          1          -    Covered
    Coverpoint #seq_item.rd_en__16#                100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   14516          1          -    Covered
        bin auto[1]                                    3484          1          -    Covered
    Coverpoint #seq_item.full__17#                 100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   10778          1          -    Covered
        bin auto[1]                                    7214          1          -    Covered
    Coverpoint #seq_item.wr_en__18#                100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                    9588          1          -    Covered
        bin auto[1]                                    8412          1          -    Covered
    Coverpoint #seq_item.rd_en__19#                100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   14516          1          -    Covered
        bin auto[1]                                    3484          1          -    Covered
    Coverpoint #seq_item.wr_ack__20#               100.00%        100          -    Covered
        covered/total bins:                               2          2          -
        missing/total bins:                               0          2          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                   14707          1          -    Covered
        bin auto[1]                                    3293          1          -    Covered
    Cross wr_ack                                    75.00%        100          -    Uncovered
        covered/total bins:                               6          8          -
        missing/total bins:                               2          8          -
        % Hit:                                      75.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>               677          1          -    Covered
            bin <auto[1],auto[0],auto[1]>              2616          1          -    Covered
            bin <auto[1],auto[1],auto[0]>               520          1          -    Covered
            bin <auto[0],auto[1],auto[0]>              2287          1          -    Covered
            bin <auto[1],auto[0],auto[0]>              4599          1          -    Covered
            bin <auto[0],auto[0],auto[0]>              7301          1          -    Covered
            bin <auto[0],*,auto[1]>                       0          1          2    ZERO
    Cross full                                      75.00%        100          -    Uncovered
        covered/total bins:                               6          8          -
        missing/total bins:                               2          8          -
        % Hit:                                      75.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[0],auto[1]>              5295          1          -    Covered
            bin <auto[0],auto[0],auto[1]>              1919          1          -    Covered
            bin <auto[1],auto[1],auto[0]>              1197          1          -    Covered
            bin <auto[0],auto[1],auto[0]>              2287          1          -    Covered
            bin <auto[1],auto[0],auto[0]>              1913          1          -    Covered
            bin <auto[0],auto[0],auto[0]>              5381          1          -    Covered
            bin <*,auto[1],auto[1]>                       0          1          2    ZERO
    Cross overflow                                  75.00%        100          -    Uncovered
        covered/total bins:                               6          8          -
        missing/total bins:                               2          8          -
        % Hit:                                      75.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>              498          1          -    Covered
            bin <auto[1],auto[0],auto[1]>              4435          1          -    Covered
            bin <auto[1],auto[1],auto[0]>               699          1          -    Covered
            bin <auto[0],auto[1],auto[0]>              2287          1          -    Covered
            bin <auto[1],auto[0],auto[0]>              2780          1          -    Covered
            bin <auto[0],auto[0],auto[0]>              7301          1          -    Covered
            bin <auto[0],*,auto[1]>                       0          1          2    ZERO
    Cross empty                                     100.00%        100          -    Covered
        covered/total bins:                               8          8          -
        missing/total bins:                               0          8          -
        % Hit:                                      100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>               22          1          -    Covered
            bin <auto[0],auto[1],auto[1]>              1818          1          -    Covered
            bin <auto[1],auto[0],auto[1]>               157          1          -    Covered
            bin <auto[0],auto[0],auto[1]>              4385          1          -    Covered
            bin <auto[1],auto[1],auto[0]>              1175          1          -    Covered
            bin <auto[0],auto[1],auto[0]>               469          1          -    Covered
            bin <auto[1],auto[0],auto[0]>              7051          1          -    Covered
            bin <auto[0],auto[0],auto[0]>              2915          1          -    Covered
    Cross almostfull                                100.00%        100          -    Covered
        covered/total bins:                               8          8          -
        missing/total bins:                               0          8          -
        % Hit:                                      100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>              812          1          -    Covered
            bin <auto[0],auto[1],auto[1]>              217          1          -    Covered
            bin <auto[1],auto[0],auto[1]>              334          1          -    Covered
            bin <auto[0],auto[0],auto[1]>              344          1          -    Covered
            bin <auto[1],auto[1],auto[0]>              385          1          -    Covered
            bin <auto[0],auto[1],auto[0]>              2070          1          -    Covered
            bin <auto[1],auto[0],auto[0]>              6874          1          -    Covered
            bin <auto[0],auto[0],auto[0]>              6956          1          -    Covered
    Cross almostempty                               100.00%        100          -    Covered
        covered/total bins:                               8          8          -
        missing/total bins:                               0          8          -
        % Hit:                                      100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>               75          1          -    Covered
            bin <auto[0],auto[1],auto[1]>               27          1          -    Covered
            bin <auto[1],auto[0],auto[1]>              227          1          -    Covered
            bin <auto[0],auto[0],auto[1]>              102          1          -    Covered
            bin <auto[1],auto[1],auto[0]>              1122          1          -    Covered
            bin <auto[0],auto[1],auto[0]>              2260          1          -    Covered
            bin <auto[1],auto[0],auto[0]>              6981          1          -    Covered
            bin <auto[0],auto[0],auto[0]>              7198          1          -    Covered
    Cross underflow                                 75.00%        100          -    Uncovered
        covered/total bins:                               6          8          -
        missing/total bins:                               2          8          -
        % Hit:                                      75.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>               39          1          -    Covered
            bin <auto[0],auto[1],auto[1]>              1754          1          -    Covered
            bin <auto[1],auto[1],auto[0]>              1158          1          -    Covered
            bin <auto[0],auto[1],auto[0]>               533          1          -    Covered
            bin <auto[1],auto[0],auto[0]>              7215          1          -    Covered
            bin <auto[0],auto[0],auto[0]>              7301          1          -    Covered
            bin <*,auto[0],auto[1]>                       0          1          2    ZERO

TOTAL COVERGROUP COVERAGE: 96.42%  COVERGROUP TYPES: 1
```

➔ Assertion Coverage

Digital Verification - coverage_rpt.txt

```
DIRECTIVE COVERAGE:
--------------------------------------------------------------------------------------------
Name                                     Design Design   Lang File(Line)      Hits Status
                                         Unit   UnitType
--------------------------------------------------------------------------------------------
/top/DUT/FIFO_SVA_inst/overflow_cover    FIFO_SVA Verilog  SVA  FIFO_SVA.sv(86) 4825 Covered
/top/DUT/FIFO_SVA_inst/underflow_cover   FIFO_SVA Verilog  SVA  FIFO_SVA.sv(87) 1749 Covered
/top/DUT/FIFO_SVA_inst/wr_ack_cover      FIFO_SVA Verilog  SVA  FIFO_SVA.sv(88) 3222 Covered
/top/DUT/FIFO_SVA_inst/count_up_pr_cover FIFO_SVA Verilog  SVA  FIFO_SVA.sv(89) 2599 Covered
/top/DUT/FIFO_SVA_inst/count_down_pr_cover
                                         FIFO_SVA Verilog  SVA  FIFO_SVA.sv(90)  969 Covered
/top/DUT/FIFO_SVA_inst/count_same_pr_cover
                                         FIFO_SVA Verilog  SVA  FIFO_SVA.sv(91)  623 Covered

TOTAL DIRECTIVE COVERAGE: 100.00%  COVERS: 6

ASSERTION RESULTS:
---------------------------------------------------------------------
Name                 File(Line)                  Failure      Pass
                                                 Count        Count
---------------------------------------------------------------------
/top/DUT/FIFO_SVA_inst/wr_ack_reset_assertion
                     FIFO_SVA.sv(5)                    0          1
/top/DUT/FIFO_SVA_inst/overflow_reset_assertion
                     FIFO_SVA.sv(6)                    0          1
/top/DUT/FIFO_SVA_inst/underflow_reset_assertion
                     FIFO_SVA.sv(7)                    0          1
/top/DUT/FIFO_SVA_inst/wr_ptr_reset_assertion
                     FIFO_SVA.sv(8)                    0          1
/top/DUT/FIFO_SVA_inst/rd_ptr_reset_assertion
                     FIFO_SVA.sv(9)                    0          1
/top/DUT/FIFO_SVA_inst/count_reset_assertion
                     FIFO_SVA.sv(10)                   0          1
/top/DUT/FIFO_SVA_inst/full_assertion
                     FIFO_SVA.sv(17)                   0          1
/top/DUT/FIFO_SVA_inst/almostfull_assertion
                     FIFO_SVA.sv(23)                   0          1
/top/DUT/FIFO_SVA_inst/empty_assertion
                     FIFO_SVA.sv(29)                   0          1
/top/DUT/FIFO_SVA_inst/almostempty_assertion
                     FIFO_SVA.sv(35)                   0          1
/top/DUT/FIFO_SVA_inst/overflow_assertion
                     FIFO_SVA.sv(79)                   0          1
/top/DUT/FIFO_SVA_inst/underflow_assertion
                     FIFO_SVA.sv(80)                   0          1
/top/DUT/FIFO_SVA_inst/wr_ack_assertion
                     FIFO_SVA.sv(81)                   0          1
/top/DUT/FIFO_SVA_inst/count_up_pr_assertion
                     FIFO_SVA.sv(82)                   0          1
/top/DUT/FIFO_SVA_inst/count_down_pr_assertion
                     FIFO_SVA.sv(83)                   0          1
/top/DUT/FIFO_SVA_inst/count_same_pr_assertion
                     FIFO_SVA.sv(84)                   0          1
/FIFO_read_only_sequence_pkg/FIFO_read_only_sequence/body/#ublk#18055399#14/immed__19
                     FIFO_read_only_sequence.sv(19)
                                                       0          1
/FIFO_write_only_sequence_pkg/FIFO_write_only_sequence/body/#ublk#39281767#14/immed__19
                     FIFO_write_only_sequence.sv(19)
                                                       0          1
/FIFO_write_read_sequence_pkg/FIFO_write_read_sequence/body/#ublk#33908887#14/immed__17
                     FIFO_write_read_sequence.sv(17)
                                                       0          1

Total Coverage By Instance (filtered view): 85.86%
```