

UVM Synchronous FIFO Project

by

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Under the guidance of **Eng. Kareem Waseem**

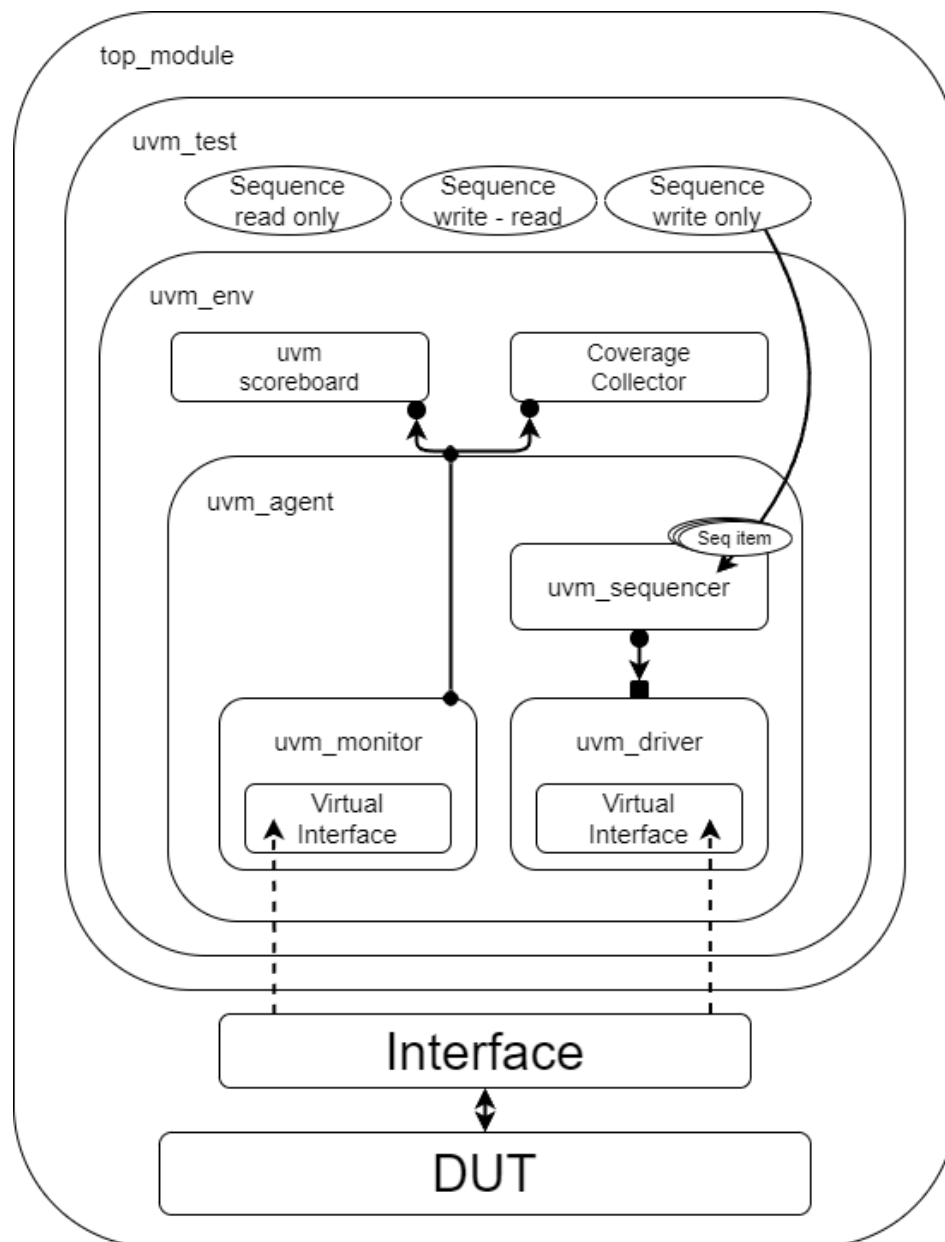
→ Verification plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
RESET	When the reset is asserted, the output UnderFlow, Overflow, and wr_ack should be low	Directed at the start of the sim, then randomized with constraint that drive the reset to be off most of the simulation time	-	A checker and Immediate assertion to check for the async reset functionality
WRITE_1	When the wr_en is asserted and if the fifo is not full, the data_in should be stored in the fifo, the output wr_ack should be high	Randomization under constraints on the wr_en signal to be on 70% of the time by default	cross coverage to cover the wr_ack, and full flags with wr_en and rd_en	A checker and a concurrent assertion to check the wr_ack flag and Immediate assertion to check full flag
WRITE_2	When the wr_en is asserted and the full flag is high, the data_in will not be written, the output overflow flag should be high	Randomization under constraints on the wr_en signal to be on 70% of the time by default	cross coverage to cover the overflow with wr_en and rd_en	A checker and a concurrent assertion to check the overflow signal
WRITE_3	When fifo is almost full (only one empty space inside the fifo), the output almostfull flag should be high	Randomization under constraints on the wr_en signal to be on 70% of the time by default	cross coverage to cover the almostfull flag with wr_en and rd_en	A checker and a Immediate assertion to check the almostfull flag
READ_1	When the rd_en is asserted, the output data_out should be shown the value stored in the fifo if it was not empty, the output underflow should be high if the fifo is empty	Randomization under constraints on the rd_en signal to be on 30% of the time by default	cross coverage to cover empty flag with wr_en and rd_en	A checker to check the data_out and a Immediate assertion to check the empty flag
READ_2	When the rd_en is asserted and the empty flag is high, the output underflow should be high	Randomization under constraints on the rd_en signal to be on 30% of the time by default	cross coverage to cover the underflow flag with wr_en and rd_en	A checker and a concurrent assertion to check the underflow flag
READ_3	When fifo is almost empty(only one value inside the fifo), the output almostempty flag should be high	Randomization under constraints on the rd_en signal to be on 30% of the time by default	cross coverage to cover the almost empty flag with wr_en and rd_en	A checker and a Immediate assertion to check the almost empty flag
WRITE_READ_1	When the wr_en and rd_en are asserted the and full flag is high, the fifo should preform the read operation only, the internal count should decrease	Randomization under constraints on the wr_en and rd_en signals to be on 70% and 30%	cross coverage to cover full flag with wr_en and rd_en	concurrent assertion to check the result
WRITE_READ_2	When the wr_en and rd_en are asserted the and empty flag is high, the fifo should preform the write operation only, the internal count should increase	Randomization under constraints on the wr_en and rd_en signals to be on 70% and 30%	cross coverage to cover empty flag with wr_en and rd_en	concurrent assertion to check the result
WRITE_READ_3	When the wr_en and rd_en are asserted the and full/empty flag are low, the fifo should preform the write and read operation in the same time, the internal count should remain the same	Randomization under constraints on the wr_en and rd_en signals to be on 70% and 30%	-	concurrent assertion to check the result

→ Assertions table

Feature	Assertion
Whenever the FIFO has no empty space, full flag should be high	if(count == FIFO_DEPTH) assert (full);
Whenever the FIFO has only one empty space, almostfull flag should be high	if(count == FIFO_DEPTH-1) assert (almostfull);
Whenever the FIFO has no item, empty flag should be high	if(!count) assert (empty);
Whenever the FIFO has only one item, almostempty flag should be high	if(count == 1) assert (almostempty);
Whenever wr_en is asserted and the FIFO is not full, wr_ack flag should be high	@(posedge clk) (wr_en && !full) >= wr_ack;
Whenever wr_en is asserted and the FIFO is full, overflow flag should be high	@(posedge clk) (wr_en && full) >= overflow;
Whenever rd_en is asserted and the FIFO is empty, underflow flag should be high	@(posedge clk) (rd_en && empty) >= underflow;
Whenever wr_en is asserted and rd_en is deasserted and the FIFO is not full, internal counter should increase	@(posedge clk) ((wr_en && !full) && (!rd_en empty)) >= count == (\$past(count) + 1);
Whenever wr_en is deasserted and rd_en is asserted and the FIFO is not empty, internal counter should decrease	@(posedge clk) ((rd_en && !empty) && (!wr_en full)) >= count == (\$past(count) - 1);
Whenever wr_en and rd_en asserted in the same time and the FIFO neither full nor empty, internal counter still the same	@(posedge clk) (wr_en && rd_en && !full && !empty) >= count == \$past(count);

→ UVM Structure Diagram



→ UVM Structure Details

TOP:

- Instantiate the DUT and interface.
- Bind the assertion with the DUT.
- Store the interface as virtual interface inside the db.
- Start the test.

Test:

- Get the virtual interface from the db and store it again as a config obj.
- Build the sequences and the env.
- Start the sequences.

Env:

- Build the agent, scoreboard, coverage collector.
- Connect the scoreboard and coverage collector analysis export with the agent analysis port.

Monitor, Scoreboard and Coverage collector:

- After the monitor sample the interface data at the negative edge of the clk it broadcasts it as an obj. of the seq_item using the analysis port to the scoreboard and coverage collector.
- The scoreboard and coverage collector store the received data initially in their internal FIFO.

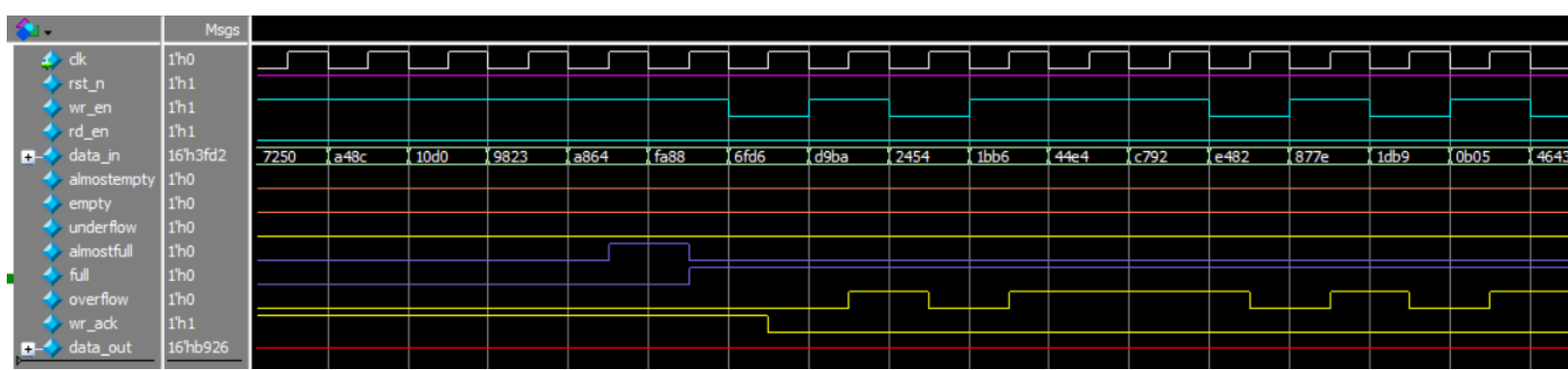
Agent:

- Build sequencer, driver, and monitor
- Get the config obj and use it to connect the monitor and driver with the virtual interface.
- connect the driver port with the sequencer export.
- connect the monitor analysis port with the agent analysis port.

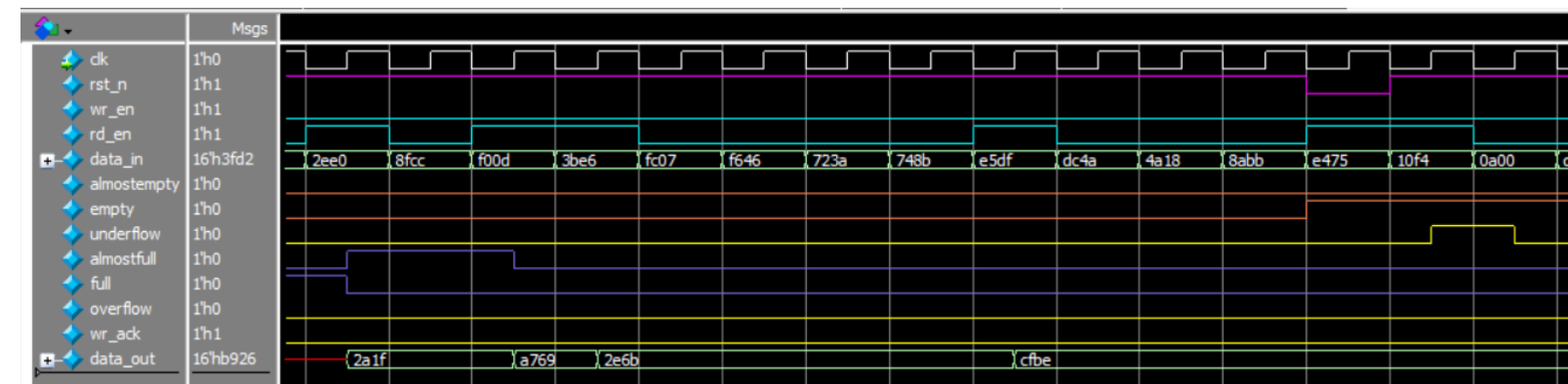
Driver, Sequence and Sequencer:

- After the Test start a sequence it sends its data to the sequencer. And the sequence waits until the data is used before sending again.
- The driver starts by pulling the data from the sequencer, and uses it to drive the DUT. After the data is used, the driver sends to the sequencer that it finished and starts pulling new data again.

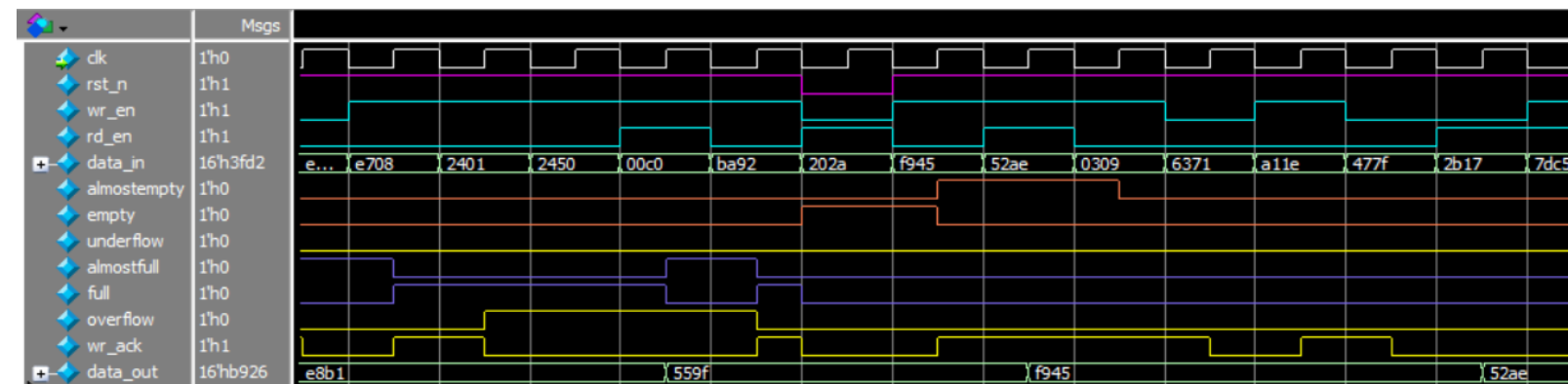
→ Waveform



Write only sequence
 wr_en = random, rd_en = 0



Read only sequence
 wr_en = 0, rd_en = random



Read_Write sequence
 wr_en = random, rd_en = random

→ Bugs

- ▶ **Add:** reset for wr_ack, overflow and underflow
- ▶ **Move:** overflow, and underflow flags control outside the else branch
- ▶ **Fix:** almostfull flag to be high only when ((count == FIFO_DEPTH - 1))
- ▶ **ADD:** two missing cases for the counter
 - re_en = 1, wr_en = 1, empty = 1 => count = count + 1
 - re_en = 1, wr_en = 1, full = 1 => count = count - 1
- ▶ **Fix:** Changing underflow flag from comb. to seq.

→ Code Coverage

```

280 Branch Coverage:
281   Enabled Coverage          Bins    Hits    Misses  Coverage
282   -----
283   Branches                  27      27        0   100.00%
284
285   =====Branch Details=====
286
287 Branch Coverage for instance /top/DUT
288

```

```

596 Statement Coverage:
597   Enabled Coverage          Bins    Hits    Misses  Coverage
598   -----
599   Statements                27      27        0   100.00%
600
601   =====Statement Details=====
602
603 Statement Coverage for instance /top/DUT --
604

```

```

6   =====
7 Toggle Coverage:
8   Enabled Coverage          Bins    Hits    Misses  Coverage
9   -----
10  Toggles                   86      86        0   100.00%
11
12  =====Toggle Details=====
13
14 Toggle Coverage for instance /top/FIFO_if --
15

```

➔ Functional Coverage

Digital Verification - coverage_rpt.txt				
3303	COVERGROUP COVERAGE:			
3304	-----			
3305	Covergroup	Metric	Goal	Bins Status
3306	-----			
3307	-----			
3308	TYPE /FIFO_cover_pkg/FIFO_cover/cvr	96.42%	100	- Uncovered
3309	covered/total bins:	90	98	-
3310	missing/total bins:	8	98	-
3311	% Hit:	91.83%	100	-
3312	Coverpoint #seq_item.wr_en_0#	100.00%	100	- Covered
3313	covered/total bins:	2	2	-
3314	missing/total bins:	0	2	-
3315	% Hit:	100.00%	100	-
3316	bin auto[0]	9588	1	- Covered
3317	bin auto[1]	8412	1	- Covered
3318	Coverpoint #seq_item.rd_en_1#	100.00%	100	- Covered
3319	covered/total bins:	2	2	-
3320	missing/total bins:	0	2	-
3321	% Hit:	100.00%	100	-
3322	bin auto[0]	14516	1	- Covered
3323	bin auto[1]	3484	1	- Covered
3324	Coverpoint #seq_item.underflow_2#	100.00%	100	- Covered
3325	covered/total bins:	2	2	-
3326	missing/total bins:	0	2	-
3327	% Hit:	100.00%	100	-
3328	bin auto[0]	16207	1	- Covered
3329	bin auto[1]	1793	1	- Covered
3330	Coverpoint #seq_item.wr_en_3#	100.00%	100	- Covered
3331	covered/total bins:	2	2	-
3332	missing/total bins:	0	2	-
3333	% Hit:	100.00%	100	-
3334	bin auto[0]	9588	1	- Covered
3335	bin auto[1]	8412	1	- Covered
3336	Coverpoint #seq_item.rd_en_4#	100.00%	100	- Covered
3337	covered/total bins:	2	2	-
3338	missing/total bins:	0	2	-
3339	% Hit:	100.00%	100	-
3340	bin auto[0]	14516	1	- Covered
3341	bin auto[1]	3484	1	- Covered
3342	Coverpoint #seq_item.almostempty_5#	100.00%	100	- Covered
3343	covered/total bins:	2	2	-
3344	missing/total bins:	0	2	-
3345	% Hit:	100.00%	100	-
3346	bin auto[0]	17561	1	- Covered
3347	bin auto[1]	431	1	- Covered
3348	Coverpoint #seq_item.wr_en_6#	100.00%	100	- Covered
3349	covered/total bins:	2	2	-
3350	missing/total bins:	0	2	-
3351	% Hit:	100.00%	100	-
3352	bin auto[0]	9588	1	- Covered
3353	bin auto[1]	8412	1	- Covered
3354	Coverpoint #seq_item.rd_en_7#	100.00%	100	- Covered
3355	covered/total bins:	2	2	-
3356	missing/total bins:	0	2	-
3357	% Hit:	100.00%	100	-
3358	bin auto[0]	14516	1	- Covered
3359	bin auto[1]	3484	1	- Covered
3360	Coverpoint #seq_item.almostfull_8#	100.00%	100	- Covered
3361	covered/total bins:	2	2	-
3362	missing/total bins:	0	2	-
3363	% Hit:	100.00%	100	-
3364	bin auto[0]	16285	1	- Covered
3365	bin auto[1]	1707	1	- Covered
3366	Coverpoint #seq_item.wr_en_9#	100.00%	100	- Covered
3367	covered/total bins:	2	2	-
3368	missing/total bins:	0	2	-
3369	% Hit:	100.00%	100	-
3370	bin auto[0]	9588	1	- Covered
3371	bin auto[1]	8412	1	- Covered
3372	Coverpoint #seq_item.rd_en_10#	100.00%	100	- Covered
3373	covered/total bins:	2	2	-
3374	missing/total bins:	0	2	-
3375	% Hit:	100.00%	100	-
3376	bin auto[0]	14516	1	- Covered
3377	bin auto[1]	3484	1	- Covered
3378	Coverpoint #seq_item.empty_11#	100.00%	100	- Covered
3379	covered/total bins:	2	2	-
3380	missing/total bins:	0	2	-
3381	% Hit:	100.00%	100	-
3382	bin auto[0]	11610	1	- Covered
3383	bin auto[1]	6382	1	- Covered
3384	Coverpoint #seq_item.wr_en_12#	100.00%	100	- Covered
3385	covered/total bins:	2	2	-
3386	missing/total bins:	0	2	-
3387	% Hit:	100.00%	100	-
3388	bin auto[0]	9588	1	- Covered
3389	bin auto[1]	8412	1	- Covered
3390	Coverpoint #seq_item.rd_en_13#	100.00%	100	- Covered
3391	covered/total bins:	2	2	-
3392	missing/total bins:	0	2	-
3393	% Hit:	100.00%	100	-
3394	bin auto[0]	14516	1	- Covered
3395	bin auto[1]	3484	1	- Covered
3396	Coverpoint #seq_item.overflow_14#	100.00%	100	- Covered
3397	covered/total bins:	2	2	-
3398	missing/total bins:	0	2	-
3399	% Hit:	100.00%	100	-
3400	bin auto[0]	13067	1	- Covered
3401	bin auto[1]	4933	1	- Covered
3402	Coverpoint #seq_item.wr_en_15#	100.00%	100	- Covered
3403	covered/total bins:	2	2	-
3404	missing/total bins:	0	2	-
3405	% Hit:	100.00%	100	-
3406	bin auto[0]	9588	1	- Covered
3407	bin auto[1]	8412	1	- Covered
3408	Coverpoint #seq_item.rd_en_16#	100.00%	100	- Covered
3409	covered/total bins:	2	2	-
3410	missing/total bins:	0	2	-
3411	% Hit:	100.00%	100	-
3412	bin auto[0]	14516	1	- Covered
3413	bin auto[1]	3484	1	- Covered
3414	Coverpoint #seq_item.full_17#	100.00%	100	- Covered
3415	covered/total bins:	2	2	-
3416	missing/total bins:	0	2	-
3417	% Hit:	100.00%	100	-
3418	bin auto[0]	10778	1	- Covered
3419	bin auto[1]	7214	1	- Covered

3420	Coverpoint #seq_item.wr_en_18#	100.00%	100	- Covered
3421	covered/total bins:	2	2	-
3422	missing/total bins:	0	2	-
3423	% Hit:	100.00%	100	-
3424	bin auto[0]	9588	1	- Covered
3425	bin auto[1]	8412	1	- Covered
3426	Coverpoint #seq_item.rd_en_19#	100.00%	100	- Covered
3427	covered/total bins:	2	2	-
3428	missing/total bins:	0	2	-
3429	% Hit:	100.00%	100	-
3430	bin auto[0]	14516	1	- Covered
3431	bin auto[1]	3484	1	- Covered
3432	Coverpoint #seq_item.wr_ack_20#	100.00%	100	- Covered
3433	covered/total bins:	2	2	-
3434	missing/total bins:	0	2	-
3435	% Hit:	100.00%	100	-
3436	bin auto[0]	14707	1	- Covered
3437	bin auto[1]	3293	1	- Covered
3438	Cross wr_ack	75.00%	100	- Uncovered
3439	covered/total bins:	6	8	-
3440	missing/total bins:	2	8	-
3441	% Hit:	75.00%	100	-
3442	Auto, Default and User Defined Bins:			
3443	bin <auto[1],auto[1],auto[1]>	677	1	- Covered
3444	bin <auto[1],auto[0],auto[1]>	2616	1	- Covered
3445	bin <auto[1],auto[1],auto[0]>	520	1	- Covered
3446	bin <auto[0],auto[1],auto[0]>	2287	1	- Covered
3447	bin <auto[1],auto[0],auto[0]>	4599	1	- Covered
3448	bin <auto[0],auto[0],auto[0]>	7301	1	- Covered
3449	bin <auto[0],*,auto[1]>	0	1	2 ZERO
3450	Cross full	75.00%	100	- Uncovered
3451	covered/total bins:	6	8	-
3452	missing/total bins:	2	8	-
3453	% Hit:	75.00%	100	-
3454	Auto, Default and User Defined Bins:			
3455	bin <auto[1],auto[0],auto[1]>	5295	1	- Covered
3456	bin <auto[0],auto[0],auto[1]>	1919	1	- Covered
3457	bin <auto[1],auto[1],auto[0]>	1197	1	- Covered
3458	bin <auto[0],auto[1],auto[0]>	2287	1	- Covered
3459	bin <auto[1],auto[0],auto[0]>	1913	1	- Covered
3460	bin <auto[0],auto[0],auto[0]>	5301	1	- Covered
3461	bin <*,auto[1],auto[1]>	0	1	2 ZERO
3462	Cross overflow	75.00%	100	- Uncovered
3463	covered/total bins:	6	8	-
3464	missing/total bins:	2	8	-
3465	% Hit:	75.00%	100	-
3466	Auto, Default and User Defined Bins:			
3467	bin <auto[1],auto[1],auto[1]>	498	1	- Covered
3468	bin <auto[1],auto[0],auto[1]>	4435	1	- Covered
3469	bin <auto[1],auto[1],auto[0]>	699	1	- Covered
3470	bin <auto[0],auto[1],auto[0]>	2287	1	- Covered
3471	bin <auto[1],auto[0],auto[0]>	2780	1	- Covered
3472	bin <auto[0],auto[0],auto[0]>	7301	1	- Covered
3473	bin <auto[0],*,auto[1]>	0	1	2 ZERO
3474	Cross empty	100.00%	100	- Covered
3475	covered/total bins:	8	8	-
3476	missing/total bins:	0	8	-
3477	% Hit:	100.00%	100	-
3478	Auto, Default and User Defined Bins:			
3479	bin <auto[1],auto[1],auto[1]>	22	1	- Covered
3480	bin <auto[0],auto[1],auto[1]>	1818	1	- Covered
3481	bin <auto[1],auto[0],auto[1]>	157	1	- Covered
3482	bin <auto[0],auto[0],auto[1]>	4385	1	- Covered
3483	bin <auto[1],auto[1],auto[0]>	1175	1	- Covered
3484	bin <auto[0],auto[1],auto[0]>	469	1	- Covered
3485	bin <auto[1],auto[0],auto[0]>	7051	1	- Covered
3486	bin <auto[0],auto[0],auto[0]>	2915	1	- Covered
3487	Cross almostfull	100.00%	100	- Covered
3488	covered/total bins:	8	8	-
3489	missing/total bins:	0	8	-
3490	% Hit:	100.00%	100	-
3491	Auto, Default and User Defined Bins:			
3492	bin <auto[1],auto[1],auto[1]>	812	1	- Covered
3493	bin <auto[0],auto[1],auto[1]>	217	1	- Covered
3494	bin <auto[1],auto[0],auto[1]>	334	1	- Covered
3495	bin <auto[0],auto[0],auto[1]>	344	1	- Covered
3496	bin <auto[1],auto[1],auto[0]>	385	1	- Covered
3497	bin <auto[0],auto[1],auto[0]>	2070	1	- Covered
3498	bin <auto[1],auto[0],auto[0]>	6874	1	- Covered
3499	bin <auto[0],auto[0],auto[0]>	6956	1	- Covered
3500	Cross almostempty	100.00%	100	- Covered
3501	covered/total bins:	8	8	-
3502	missing/total bins:	0	8	-
3503	% Hit:	100.00%	100	-
3504	Auto, Default and User Defined Bins:			
3505	bin <auto[1],auto[1],auto[1]>	75	1	- Covered
3506	bin <auto[0],auto[1],auto[1]>	27	1	- Covered
3507	bin <auto[1],auto[0],auto[1]>	227	1	- Covered
3508	bin <auto[0],auto[0],auto[1]>	102	1	- Covered
3509	bin <auto[1],auto[1],auto[0]>	1122	1	- Covered
3510	bin <auto[0],auto[1],auto[0]>	2260	1	- Covered
3511	bin <auto[1],auto[0],auto[0]>	6981	1	- Covered
3512	bin <auto[0],auto[0],auto[0]>	7198	1	- Covered
3513	Cross underflow	75.00%	100	- Uncovered
3514	covered/total bins:	6	8	-
3515	missing/total bins:	2	8	-
3516	% Hit:	75.00%	100	-
3517	Auto, Default and User Defined Bins:			
3518	bin <auto[1],auto[1],auto[1]>	39	1	- Covered
3519	bin <auto[0],auto[1],auto[1]>	1754	1	- Covered
3520	bin <auto[1],auto[1],auto[0]>	1158	1	- Covered
3521	bin <auto[0],auto[1],auto[0]>	533	1	- Covered
3522	bin <auto[1],auto[0],auto[0]>	7215	1	- Covered
3523	bin <auto[0],auto[0],auto[0]>	7301	1	- Covered
3524	bin <*,auto[0],auto[1]>	0	1	2 ZERO
3525				
3526	TOTAL COVERGROUP COVERAGE: 96.42% COVERGROUP TYPES: 1			

→ Assertion Coverage

```

3528 DIRECTIVE COVERAGE:
3529 -----
3530 Name                                Design Design  Lang File(Line)      Hits Status
3531 Unit      UnitType
3532 -----
3533 /top/DUT/FIFO_SVA_inst/overflow_cover  FIFO_SVA Verilog  SVA  FIFO_SVA.sv(86)  4825 Covered
3534 /top/DUT/FIFO_SVA_inst/underflow_cover FIFO_SVA Verilog  SVA  FIFO_SVA.sv(87)  1749 Covered
3535 /top/DUT/FIFO_SVA_inst/wr_ack_cover    FIFO_SVA Verilog  SVA  FIFO_SVA.sv(88)  3222 Covered
3536 /top/DUT/FIFO_SVA_inst/count_up_pr_cover FIFO_SVA Verilog  SVA  FIFO_SVA.sv(89)  2599 Covered
3537 /top/DUT/FIFO_SVA_inst/count_down_pr_cover
3538                                FIFO_SVA Verilog  SVA  FIFO_SVA.sv(90)   969 Covered
3539 /top/DUT/FIFO_SVA_inst/count_same_pr_cover
3540                                FIFO_SVA Verilog  SVA  FIFO_SVA.sv(91)   623 Covered
3541
3542 TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 6
3543
3544 ASSERTION RESULTS:
3545 -----
3546 Name                                File(Line)                                Failure    Pass
3547                                Count                                Count
3548 -----
3549 /top/DUT/FIFO_SVA_inst/wr_ack_reset_assertion
3550                                FIFO_SVA.sv(5)                                0          1
3551 /top/DUT/FIFO_SVA_inst/overflow_reset_assertion
3552                                FIFO_SVA.sv(6)                                0          1
3553 /top/DUT/FIFO_SVA_inst/underflow_reset_assertion
3554                                FIFO_SVA.sv(7)                                0          1
3555 /top/DUT/FIFO_SVA_inst/wr_ptr_reset_assertion
3556                                FIFO_SVA.sv(8)                                0          1
3557 /top/DUT/FIFO_SVA_inst/rd_ptr_reset_assertion
3558                                FIFO_SVA.sv(9)                                0          1
3559 /top/DUT/FIFO_SVA_inst/count_reset_assertion
3560                                FIFO_SVA.sv(10)                               0          1
3561 /top/DUT/FIFO_SVA_inst/full_assertion
3562                                FIFO_SVA.sv(17)                               0          1
3563 /top/DUT/FIFO_SVA_inst/almostfull_assertion
3564                                FIFO_SVA.sv(23)                               0          1
3565 /top/DUT/FIFO_SVA_inst/empty_assertion
3566                                FIFO_SVA.sv(29)                               0          1
3567 /top/DUT/FIFO_SVA_inst/almostempty_assertion
3568                                FIFO_SVA.sv(35)                               0          1
3569 /top/DUT/FIFO_SVA_inst/overflow_assertion
3570                                FIFO_SVA.sv(79)                               0          1
3571 /top/DUT/FIFO_SVA_inst/underflow_assertion
3572                                FIFO_SVA.sv(80)                               0          1
3573 /top/DUT/FIFO_SVA_inst/wr_ack_assertion
3574                                FIFO_SVA.sv(81)                               0          1
3575 /top/DUT/FIFO_SVA_inst/count_up_pr_assertion
3576                                FIFO_SVA.sv(82)                               0          1
3577 /top/DUT/FIFO_SVA_inst/count_down_pr_assertion
3578                                FIFO_SVA.sv(83)                               0          1
3579 /top/DUT/FIFO_SVA_inst/count_same_pr_assertion
3580                                FIFO_SVA.sv(84)                               0          1
3581 /FIFO_read_only_sequence_pkg/FIFO_read_only_sequence/body/#ublk#18055399#14/immed__19
3582                                FIFO_read_only_sequence.sv(19)                0          1
3583
3584 /FIFO_write_only_sequence_pkg/FIFO_write_only_sequence/body/#ublk#39281767#14/immed__19
3585                                FIFO_write_only_sequence.sv(19)                0          1
3586
3587 /FIFO_write_read_sequence_pkg/FIFO_write_read_sequence/body/#ublk#33908887#14/immed__17
3588                                FIFO_write_read_sequence.sv(17)                0          1
3589
3590
3591 Total Coverage By Instance (filtered view): 85.86%
```