Final Year Design Project Report

RISC V IMPLEMENTATION ON FPGA

B.S ELECTRICAL ENGINEERING, BATCH 2020

Internal Advisor

Name: Dr. Abid Muhammad Khan

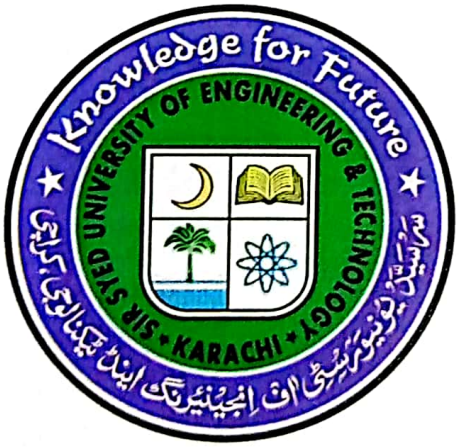
Designation: Professor

Deptt.: Electrical Engineering

Ssuet, Karachi

Submitted by

JAHANGIR SHAH	**2020-EL-050**
UMER ZAID	**2020-EL-059**
KHALID ANWER	**2020-EL-072**



DEPARTMENT OF ELECTRICAL ENGINEERING

SIR SYED UNIVERSITY OF ENGINEERING & TECHNOLOGY, KARACHI

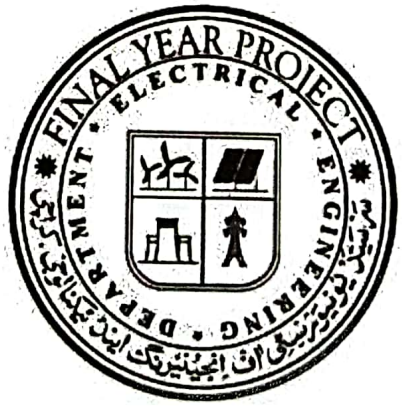
February 2024

RISC V IMPLEMENTATION ON FPGA

BY

JAHANGIR SHAH	**2020-EL-050**
UMER ZAID	**2020-EL-059**
KHALID ANWER	**2020-EL-072**

Report submitted in partial fulfillment of the
requirements for the degree of
Bachelor of Science in
ELECTRICAL ENGINEERING



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February 2024

DECLERATION

We confirm that this project report has done entirely by us. Any information or ideas from other sources are clearly mentioned along with their references. By submitting our report to the plagiarism checking software, we are confirming that our work follows the university's plagiarism rules explained in the student handbook. We understand that we may be held responsible if plagiarism software or examiners find parts that have copied without citing the source. We know that if an academic misconduct hearing finds us guilty of plagiarism, we could lose the credits for this module or face other penalties.

PROJECT TITLE: RISC V IMPLEMENTATION ON FPGA

Word count: 13,635

STUDENT NAME:

1) JAHANGIR SHAH

2) UMER ZAID

3) KHALID ANWER

Date of Submission:

Signature(s):

1) _____

2) _____

3) _____

I hereby declare that this project report entitled "RISC V IMPLEMENTATION ON FPGA" is an original work carried out by JAHANGIR SHAH, UMER ZAID, KHALID ANWER in partial fulfillment for the award of degree of Bachelor of Science in Electrical Engineering of Electrical Engineering Department, Sir Syed University of Engineering and Technology Karachi, Pakistan during the year 2024. The Project report has been approved as it satisfies the academic requirements in respect of project work prescribed for Bachelor of Science in Electrical Engineering.I also declare that it has not been previously and concurrently submitted for any other degree or other institutions.

Signature: _____

Internal Advisor: Dr. Abdul. M. Khan

Date: 27/2/2024

ACKNOWLEDGEMENT

We want to thank Sir Syed University of Engineering and Technology for supporting our project. This is a big achievement for us as undergraduate students.

We are very grateful to God for giving us the strength and ability to complete this report. We could not have finished our thesis without help from our group members, friends and encouragement from our family.

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We want to thank our parents as well. They always encouraged us to do our best. They helped us in tough time, cheered us up and stayed with us.

Sir Syed University of Engineering & Technology, Karachi
Electrical Engineering Department
Rubrics for FYDP Report Assessment (EL-499) Batch 2020S

Criteria No.	Criteria PLO (Percentage)	Excellent	Good	Fair	Poor
1	Writing Mechanics PLO-10 (10%)	The report covers all required project details / chapters and maintain reader's interest with a logical coherent flow. The structure is clear and concise.	The report covers all required project details / chapters. The structure is clear and concise.	The report shows some gaps in coverage of required project details / chapters. The structure contains repetitions and redundancies.	The report shows insufficient content to show that required project details / chapters are met. Plain listing of information without regards to structure and/or flow.
2	Literature Review and Problem statement PLO-2 (10%)	Literature is well-written and structured as per standards and covered all relevant material to the project. Problem statement is stated and covered sufficient justification. New reader can clearly understand its value and context. References are cited properly using a standard format	Literature is well-written but not properly structured as per standards and covered most of the material relevant to the project. Problem statement is stated and covered necessary justification with reference. References are cited using a standard format	Literature is not properly written and structured as per standards, but covered most of the material relevant to the project. Problem statement is stated but lacks necessary justification. References are cited using a standard format	Literature is poorly written, poorly structured and does not cover the relevant material to the project. Problem statement is vaguely stated without any justification. References are cited using a standard format.
3	Methodology PLO-3 (10%)	The methods, approaches, tools, techniques, algorithms, or other aspects of the solution are well-described with sufficient details and supporting diagrams.	The methods, approaches, tools, techniques, algorithms, or other aspects of the solution are well-described. However further explanation is required.	The methods, approaches, tools, techniques, algorithms, or other aspects of the solution are described but not in a convincing manner.	Some aspects of the solution are described briefly but much of the description is left out.

4	Implementation and Testing PLO-5 (20%)	Both implementation and testing of a system, are precisely performed with accuracy and provide all necessary details for the reader.	Both implementation and testing of a system, are performed with the necessary details for the reader.	Implementation of a system are performed with the necessary details for the reader. But testing of a system is not properly performed.	Both implementation and testing of a system, are not properly performed with lack of details.
5	Results & Conclusions PLO-4 (10%)	Report includes all key results of the project. Appropriate graphs, figures and tables are included for effective interpretation and explanation of the results. All important aspects of the project are well-summarized with the sense of closure and demonstrates the major outcome(s) of the project.	Report includes most of the key results of the project. Graphs, figures and tables are included for effective interpretation and explanation of the results. Most of the important aspects of the project are well-summarized with the sense of closure and demonstrates the outcome(s) of the project.	Includes few key results of the project. Graphs, figures and tables are included with limited interpretation and explanation of the results. Few aspects of the project are summarized with the sense of closure and demonstrates the outcome(s) of the project.	Key results of the project are missing. Graphs, figures and tables are not included. Important aspects of the project are not clearly summarized with.
6	Formatting Style and Similarity Index PLO- 8 (20%)	Formatting style of chapters, table of contents, title page, references and appendices are proper and relevant with an acceptable similarity index.	Formatting style of chapters, table of contents, title page, references and appendices are proper with only minor impact on flow of reading with acceptable similarity index	Formatting style is proper but figures and tables don't follow standard practice (caption figure number etc.) with high but acceptable similarity index	The formatting of the chapters may need improvement with very high similarity index.
7	Project Sustainability Impacts PLO-7 (20%)	The project provides engineering solutions in societal and environmental contexts and demonstrate excellent knowledge of and need for sustainable development.	The project provides engineering solutions in societal and environmental contexts and demonstrate reasonable knowledge of and need for sustainable development.	The project provides engineering solutions in societal and environmental contexts and demonstrate average knowledge of and need for sustainable development.	The project provides engineering solutions in societal and environmental contexts and demonstrate poor knowledge of and need for sustainable development.

FYDP Mapping with CEP & SDG

Complex Engineering Problem		
FYDP Title	**SDGs**	**Complex Solving Problem**
RISC-V IMPLEMENTATION ON FPGA	Goal # 9: Industry Innovation & Infrastructure	WP1 (Depth of Knowledge Required) WP3 (Depth of Analysis Required) WP7 (Interdependence)

ABSTRACT

The Reduced Instruction Set Computing FIVE (RISC-V) architecture, renowned for its open-source nature, has garnered significant attention in the area of computer architecture. The open-source RISC-V instruction set architecture offers new possibilities for research and education in computer architecture.

This work presents the implementation of the RISC-V integer base instruction set (RV32I) on a field-programmable gate array (FPGA). The data path and control logic is first modeled in Logisim to provide a reference design. Then the processor is coded in System Verilog and synthesized targeting a Xilinx FPGA using Vivado. Six representative RISC-V instructions have implemented. **R-type** for register operations, **I-type** for immediate values, **S-type** for store operations, **B-type** for conditional branches, **U-type** for setting large constants, and **J-type** for unconditional jumps. The processor successfully executed test programs using only these six instructions. This demonstrates the feasibility of realizing a simple RISC-V core on reconfigurable hardware. By leveraging open-source Electronic Design Automation (EDA) tools refer to software applications used to design and simulate electronic systems, including integrated circuits.and the customizable RISC-V ISA, this thesis enables hands-on exploration of computer architecture in an academic setting. The easily modifiable nature of the implementation developed here facilitates further RISC-V research and educational projects.

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