CS1021 Tutorial 4

Condition Code Flags

Q1 Translate following pseudo-code statement into a sequence of ARM assembly language instructions. Assume that x and y are signed integers and that x is in R1 and y in R2.

(i)
```
if ((x == 0x30) || (x == 0x31) || (x >= 0x40)) {
    y = 1;
} else {
    y = 0;
}
```

(ii)
```
if (((x >= 0x30) && (x <= 0x39)) || ((x >= 0x41) && (x <= 0x5a))) {
    y = 1;
  } else {
    y = 0;
}
```

Q2 For each ARM Assembly Language code segment below, determine the value stored in R0 and the state of the N (Negative), Z (Zero), C (Carry) and V (oVerflow) flags after the instructions have been executed

(i)
```
LDR     R0, =0x00000000
LDR     R1, =0x00000001
ADDS    R0, R0, R1          ; 0x00000001 N = 0, Z = 0, C = 0, V = 0 (0)
```

(ii)
```
LDR     R0, =0x00000001
LDR     R1, =0x00000000
SUBS    R0, R0, R1
```

(iii)
```
LDR     R0, =0x80000000
LDR     R1, =0x80000001
ADDS    R0, R0, R1
```

(iv)
```
LDR     R0, =0x00000000
LDR     R1, =0x00000000
SUBS    R0, R0, R1
```

(v)
```
LDR     R0, =0x00000000
LDR     R1, =0x00000000
ADDS    R0, R0, R1
```

(vi)
```
LDR     R0, =0x80000000
LDR     R1, =0x80000000
SUBS    R0, R0, R1
```

(vii)
```
LDR     R0, =0x80000000
LDR     R1, =0x80000000
ADDS    R0, R0, R1
```

(viii)
```
LDR     R0, =0x80000000
LDR     R1, =0x00000000
SUBS    R0, R0, R1
```

Q3 If x and y are signed 64-bit integers in R0:R1 and R2:R3 respectively and z is an integer in R4, translate the following pseudo-code statements into a sequence of ARM assembly language instructions

(i)
```
if (x == y) {
    z = 1;
} else {
    z = 0;
}
```

(ii)
```
if (x < y) {
    z = 1;
} else {
    z =0;
}
```