CS1026 II Assignment 11

Design a Verilog counter module

module Counter_1 (output reg [2: 0] Count, input clock, reset);

that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4, 0, 1, ….
changing on the rising clock edge.

Your design should output 0 on the negative edge of the reset signal.