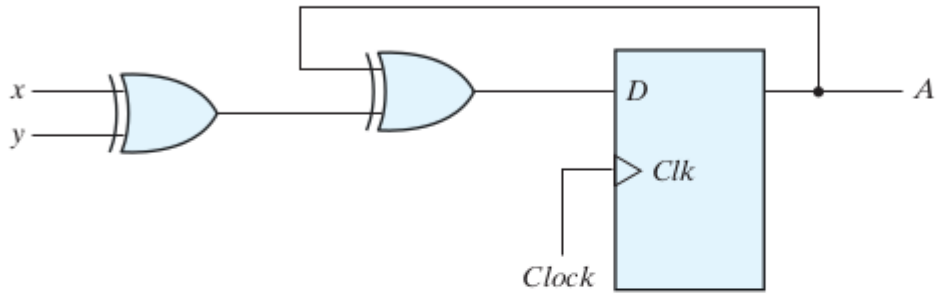
CS1026 II Assignment 7

Write a Verilog behavioural description

```
module OddFunction (output A, input x, y, clk, reset_b);
```

of the circuit below. Test data will change on the falling edge of the clock and your machine should change state on the rising edge.

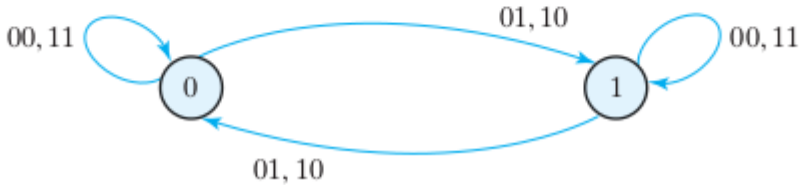
Your design should enter state 0 on the negative edge of the reset signal.



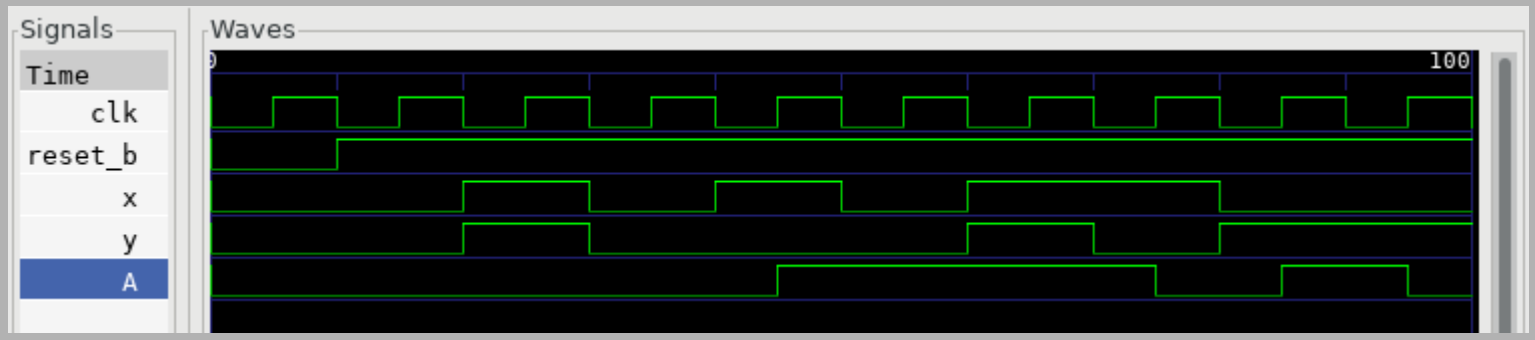
(a) Circuit diagram

Present state	Inputs	Next state
A	x y	A
0	0 0	0
0	0 1	1
0	1 0	1
0	1 1	0
1	0 0	1
1	0 1	0
1	1 0	0
1	1 1	1

(b) State table



(c) State diagram


Signals
Waves
Time
clk
reset_b
x
y
A
100