CS1026 II Assignment 5

Write a Verilog behavioural description

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module Compare (A, B, Y);
```

of a four-bit unsigned comparator with a six-bit output Y[5:0].

Bit 5 of Y is for “equals,” bit 4 for “not equal to,” bit 3 for “greater than,” bit 2 for “less than,” bit 1 for “greater than or equal,” and bit 0 for “less than or equal to.”