CS1026 II Assignment 4

Write a verilog dataflow description of a four-bit adder–subtractor of unsigned numbers.

module AdderSub (sum_diff, carry, A, B, select)

first output should be a 4 bit sum or difference, second is the carry.

The first two inputs should the 4 bit numbers to add and the final input is a select which tells the module whether to add (zero) or subtract (one).