CS1026 II Assignment 9

A synchronous finite state machine has an input x_in and an output y_out. When x_in changes from 0 to 1, the output y_out is to assert for three cycles, regardless of the value of x_in, and then de-assert for two cycles before the machine will respond to another assertion of x_in.

(a) Draw the state diagram of the machine.
(b) Write Verilog model of the machine.
module StateDiagram (output y_out, input x_in, clk, reset_b);

Test data will change on the falling edge of the clock and your machine should change state on the rising edge.

Your design should enter state 0 on the negative edge of the reset signal.