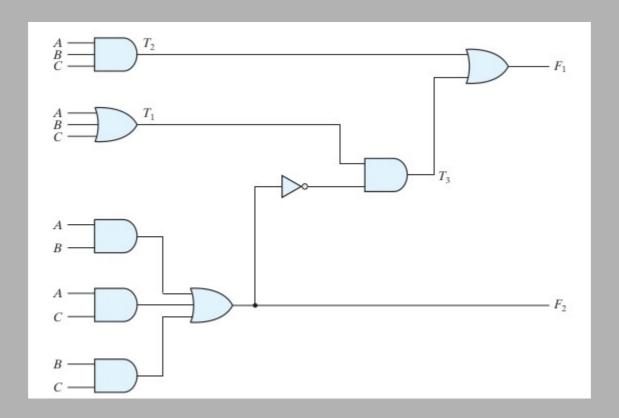
## CS1026 II Assignment 1

Write a verilog module Circuit\_1 (A, B, C, F1, F2); which implements a gate level description of the circuit below



CS1026 II 1