ECE 617: Computer-Aided Design (2)

Assignment 1: HDL Testbench

Digital System Modeling using HDL

Introduction: In this assignment, you are required to do an HDL (VHDL or Verilog) mini-project.

Objective: The objective of the assignment is to get the student experienced with HDL modeling, simulation and testbench creation.

Scope: Project scope includes developing HDL testbenches to a set of given non-trivial digital system designs.

Tools: Download and install ModelSim PE Student Edition. Refer to Modelsim_tutorial.VHDL.pdf

Statement:

1. You are given:
   - Example 22 for the D-flip-flop testbench, written in VHDL, on slides 53-55, in the VHDL1_overview lecture
   - An archive of the source code of all VHDL examples included in the VHDL lectures: examples.rar.
   - List of all examples: vhdl example list (google drive)

2. Select one example from the list:
   - Open the vhdl example list (google drive) by clicking on the file link.
   - Select only one of the given example designs in the given archive.
   - Write your name in front of the chosen example. The file is saved automatically and shared with everybody.
   - Only ONE student is allowed to choose an example. Each student must select a different example.

3. Develop a trestbench to it similar to the D-flip-flop testbench mentioned above. Use Assertions.

4. You need to decide whether to do the assignment in VHDL or Verilog.

Deliverables: A **single** zipped file **<*your_name_A1*>.zip/.rar** containing:

- The source code of all developed testbenches.
- A documentation (pdf) for the mini-project. It should include the following (at least):

1. Student name – Department
2. Design example name and location in the slides,
3. If you are doing the project in Verilog, include and document the code of the design example,
4. Test strategy (Table),
5. Testbench code,
6. Documentation for the testbench code,
7. ModelSim simulation results (snapshots) with comments, and
8. Names of all used tools.

Submission:

Email the single archive file to Mohamed.Dessouky@eng.asu.edu.eg.
Email subject **should be**: **ECE617 Assignment 1**.

Important Notes:

- Failure not to follow the above deliverables and submission procedures would result in assignment being neglected.
- The final documentation should be well written from the language and organization points of view. It must be precise and concise.
- Support the final documentation with neat diagrams and tables.
- Include a good list of references in the final documentation. Please cite every resource you use.
- To save you time, you do not need to reproduce figures/illustrations from resources. You could copy them as they are, if you wish. In that case, you must associate the copied material with a reference.
- Mini-projects are to be done individually. No groups are permitted.
- Do not copy testbenches and reports from your colleagues. Partially or fully copied testbenches or reports get **zero credit** for both students.

End of Assignment