Computer Architecture Project Report
Processor Design

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Instruction Format

Instructions Opcode

Mnemonic	15	14	13	12	11
NOP	0	0	0	0	0
NOT	0	0	0	0	1
NEG	0	0	0	1	0
INC	0	0	0	1	1
DEC	0	0	1	0	0
PUSH	0	0	1	0	1
POP	0	0	1	1	0
PROTECT	0	0	1	1	1
FREE	0	1	0	0	0
JZ	0	1	0	0	1
JMP	0	1	0	1	0
CALL	0	1	0	1	1
IN	0	1	1	0	0
OUT	0	1	1	0	1
ADD	0	1	1	1	0
SUB	0	1	1	1	1
SWAP	1	0	0	0	0
CMP	1	0	0	0	1
AND	1	0	0	1	0
OR	1	0	0	1	1
XOR	1	0	1	0	0
ADDI	1	0	1	0	1
BITSET	1	0	1	1	0
RCL	1	0	1	1	1
RCR	1	1	0	0	0
LDM	1	1	0	0	1
LDD	1	1	0	1	0
STD	1	1	0	1	1
RET	1	1	1	0	0
RTI	1	1	1	0	1

Instructions Bits Details

- R-type

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode					R_{dst}			R_{src1}			R_{src2}				

- I-type

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode					R_{dst}							EA<19:16>			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Immediate \ EA<15:0>															

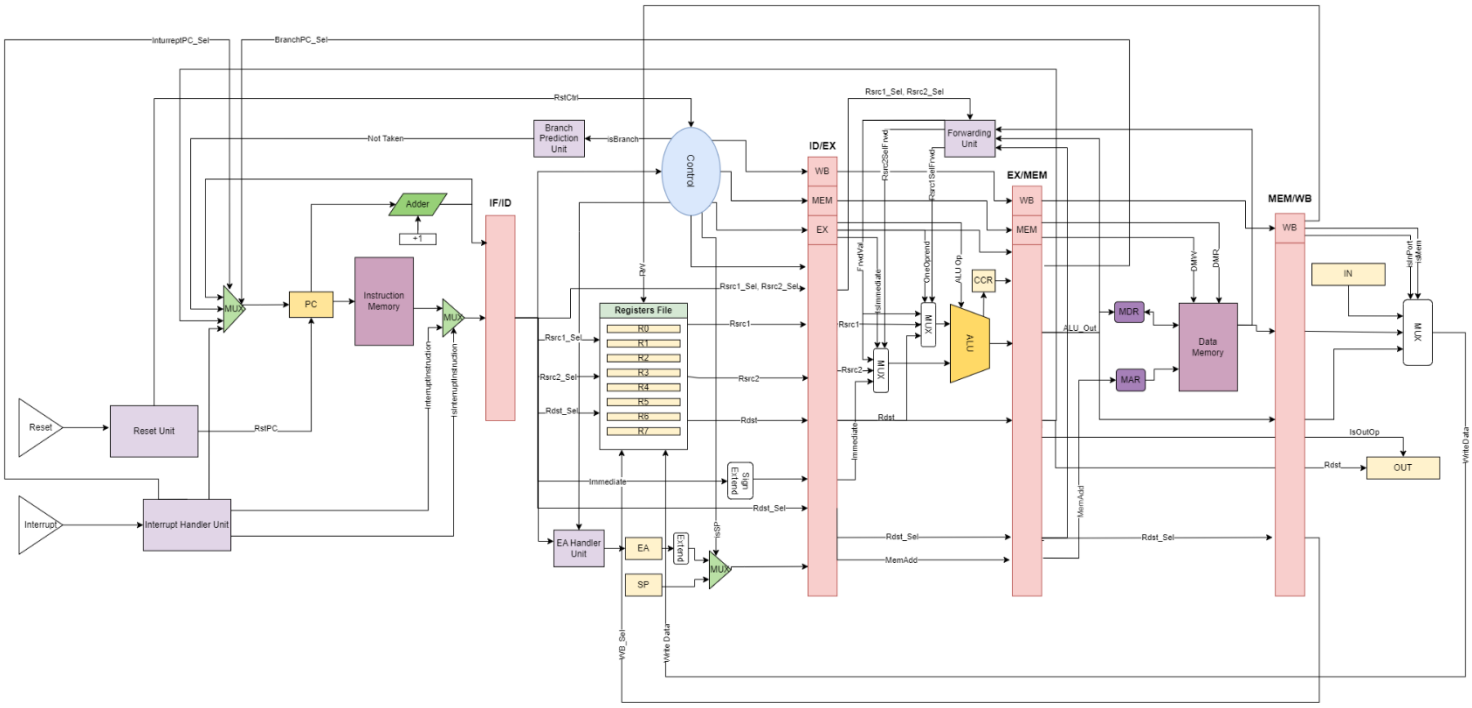
- J-type

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode								R_{dst}							

Control Signal Table

Mnemonic	Imm	StrOp	InOp	OutOp	MemOp	MR	MW	MP	MF	IsSP	Branch	FwdMem	FwdAlu	RW
NOP														
NOT														■
NEG														■
INC														■
DEC														■
PUSH										■				■
POP										■				■
PROTECT								■						
FREE									■					
JZ					■	■					■			
JMP					■	■					■			
CALL					■	■				■	■			
IN			■											
OUT				■										
ADD												■	■	■
SUB												■	■	■
SWAP					■		■			■		■	■	■
CMP												■	■	■
AND												■	■	■
OR												■	■	■
XOR												■	■	■
ADDI	■											■	■	■
BITSET	■											■	■	■
RCL	■											■	■	■
RCR	■											■	■	■
LDM	■											■	■	■
LDD	■				■	■						■	■	■
STD	■	■			■		■					■	■	■
RET					■	■				■	■			
RTI					■	■				■	■			
INT														
RESET														

Processor Schematic Diagram



processor design schematic diagram

Pipeline Stages Design

- IF/ID
  - Size: 16 bits
  - Input:
    - Instruction<15:0>
    - PC<31:0>
  - Connection
    - Control Unit Input: Instruction<15:11>
    - R_{dst} Selector: Instruction<10:8>
    - R_{src1} Selector: Instruction<7:5>
    - R_{src2} Selector: Instruction<4:2>
    - Immediate: Instruction<15:0>
    - EA<19:16>: Instruction<7:4>
    - EA<15:0>: Instruction<15:0>
    - PC<31:0>: PC_IF_ID<31:0>
- ID/EX
  - Size: 164 bits
  - Input:
    - Instruction<15:0>
    - SP_EA <31:0>
    - Rdst_sel_in <2:0>
    - Immediate_in <31:0>
    - Rsrc1_in
    - Rsrc2_in
    - Rdest_in <31:0>
    - isImmediate_in
    - ALU_OP_IN <4:0>
    - Mem_control_in <2:0>
    - WB_control_in <2:0>
    - isoneOp
    - memReadSig_in
    - regWriteSig_in
  - Connection:
    - MemAdr <31:0>
    - Rdst_sel_out <2:0>
    - Immediate_out <31:0>
    - Rsrc1_out
    - Rsrc2_out
    - Rdest_out <31:0>
    - isImmediate
    - ALU_OP <4:0>

    - Mem_control_out <2:0>
    - WB_control_out <2:0>
    - Instruction_out <15:0>
    - isOneOp_out
    - memReadSig_out
    - regWriteSig_out

- EX/MEM
  - Size: 66 bits
  - Input:
    - Rdst_sel_in<2:0>
    - MemAdr_in<31:0>
    - memReadSig_in
    - AluOutput<31:0>
    - regWriteSignal
  - Connection:
    - MemAdr_out<31:0>
    - Rdst_sel_out<2:0>
    - AluOutput<31:0>

- MEM/WB
  - Size: 66 bits
  - Input:
    - RDst_Sel<2:0>
    - ALUOutput<31:0>
    - readData<31:0>
    - dataReadSignal
    - regWriteSig
  - Connection:
    - RDst_Sel_out<2:0>
    - ALU_out<31:0>
    - readData_out<31:0>