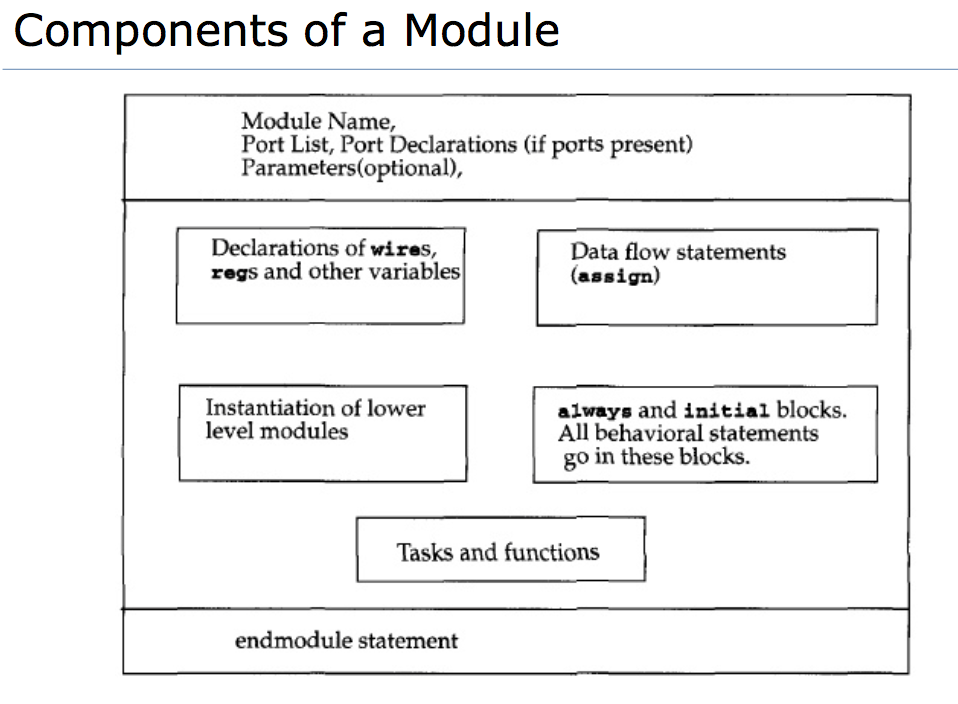
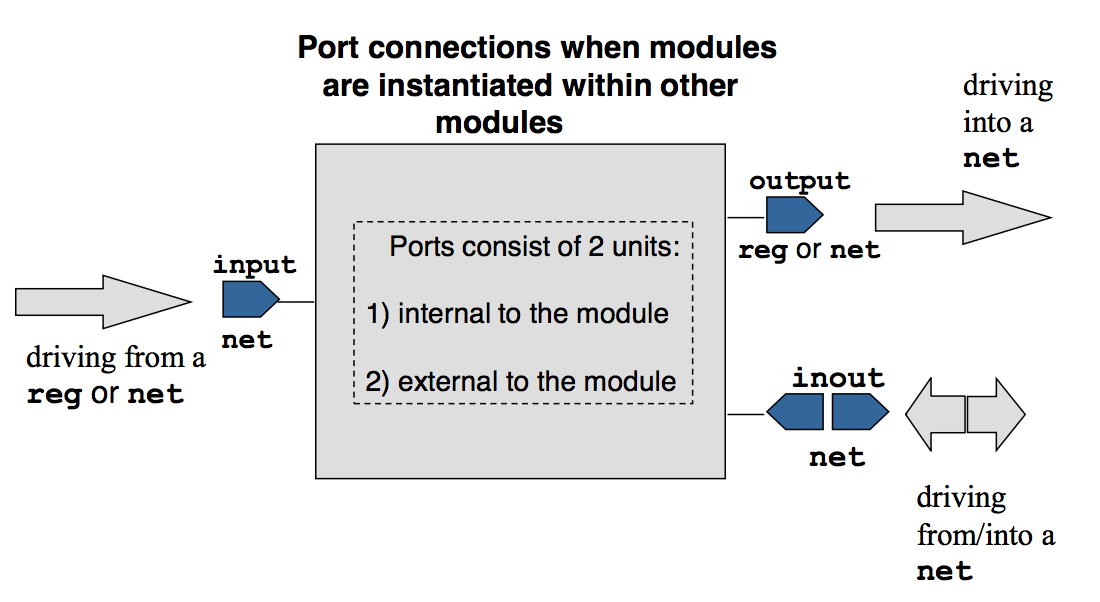
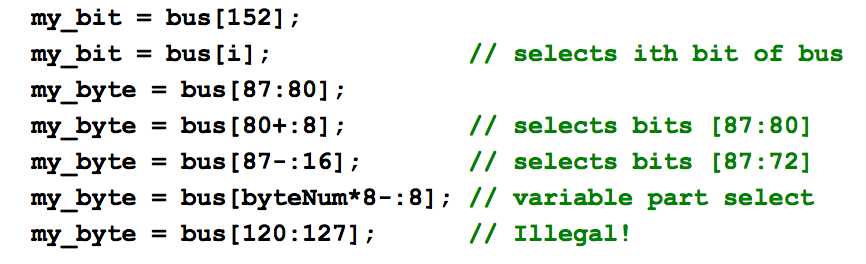
**ASIC Design Flow**: Func. Specs., HDL, Synthesis, Floorplanning, place & route, verify in circuit.

**FPGA**: Func. Specs., HDL, Synthesis, place & route, download and verify.

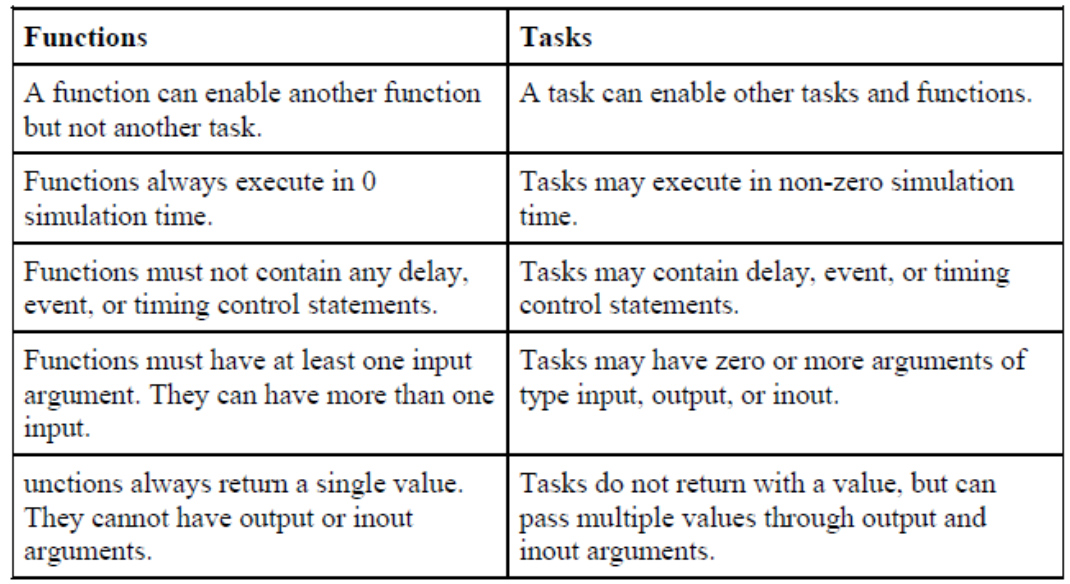
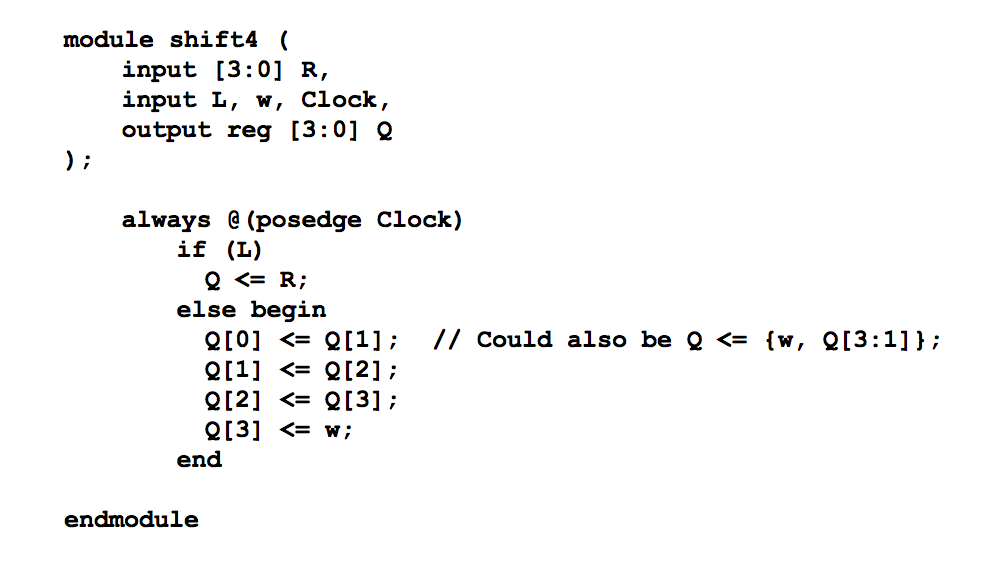
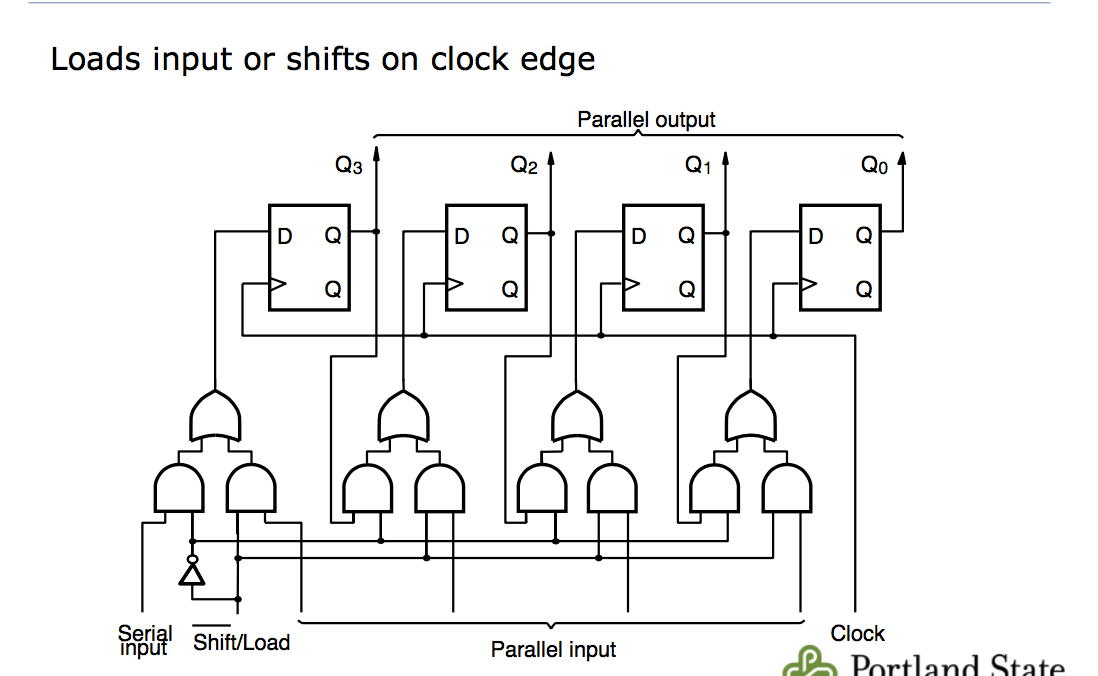
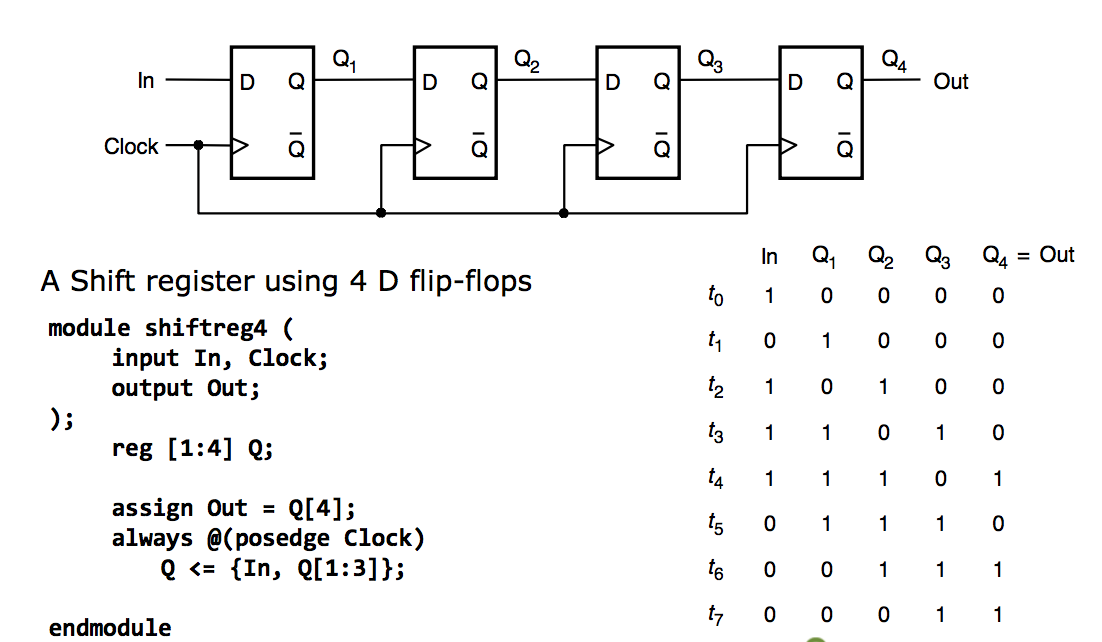
**A Verilog simulator** consists of a compiler, user interface, and event-based scheduler.

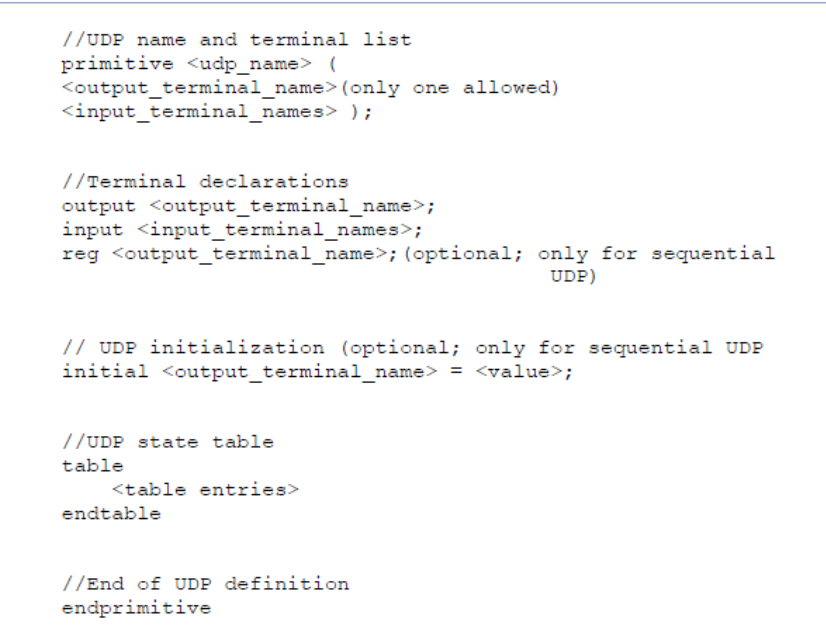
**Design Block, Stimulus Block**

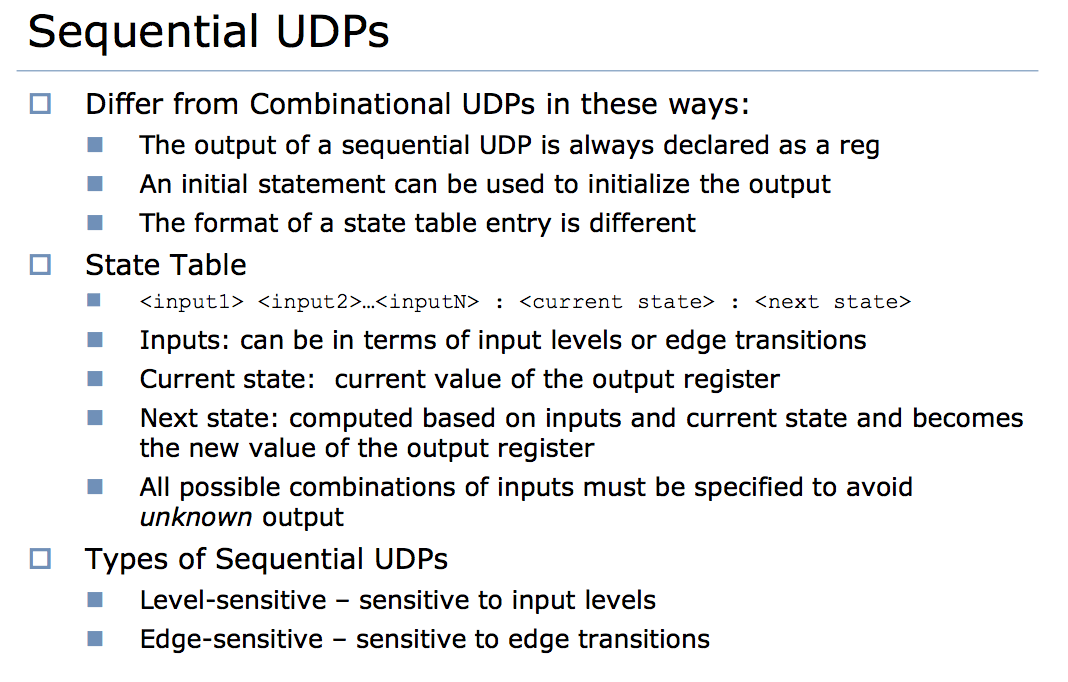
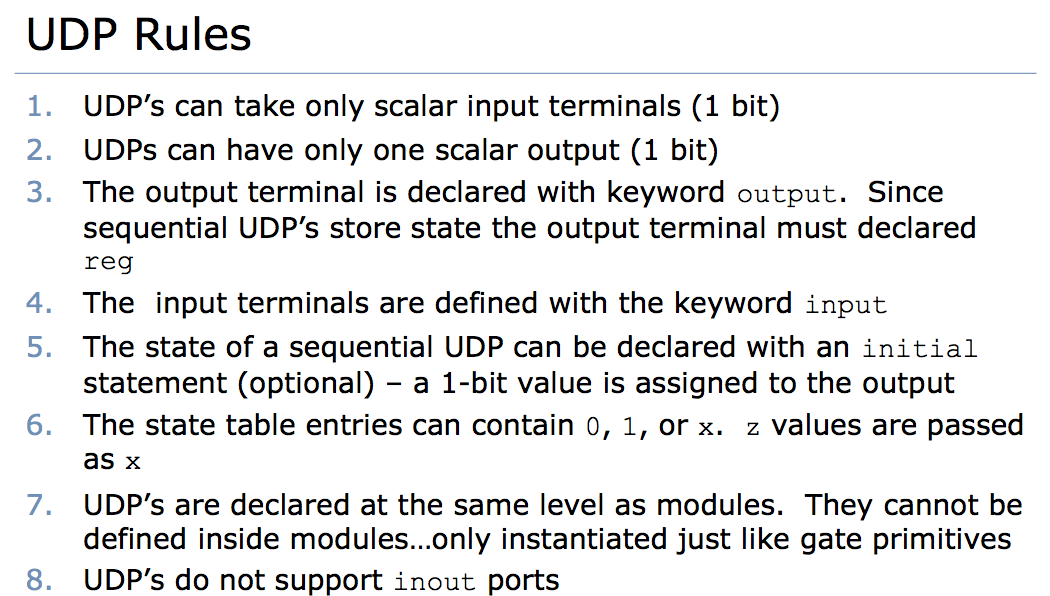
**Abstractions Levels:** Algorithmic, data flow, gate, switch, RTL.

**signed 8 bit:** -8sd104. Constant integers are signed by default. If width is specified, it’s not signed

~| Nor, ^ XOR, ^~ Xnor. **casex —>** treats all x and z as don’t cares (don’t check them). **casez** —> treats all z as don’t cares.

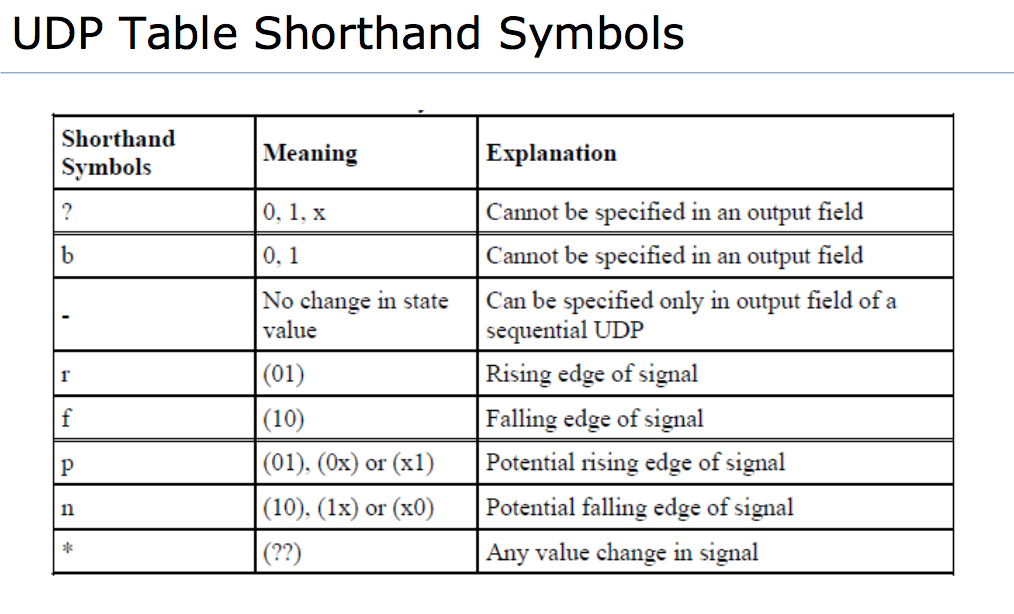
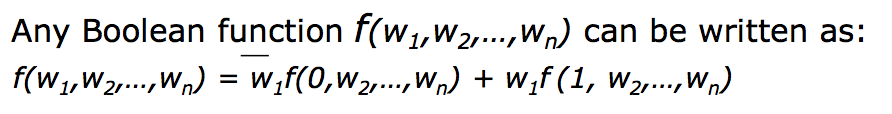
**Sequential block** —> begin end, **parallel block** —> fork join. **Named Blocks**

**Two Types of UDP:** Combinational and sequential.

****

**UDP has exactly one output.** min of 9 in for seq UDP and 10 in for comb UDP. **Events:** Named, Regular, Event OR Control, Level-Sensitive Control. wait() is used for level-sensitive. **Stimulus vectors – provide inputs to the model under test. Reference vectors –**

provide expected output from the model

under test...used to check (either manually or automatically) that the model is performing as expected. **`timescale** <ref time units>/<time precision>.100ns/1ns means sim. time tick is 100 ns and sim. time is rounded of to 1 ns increments. **I/O: Open up to 3 files at most.** **$readmem<b/h>(file\_name, mem\_name, start\_address, end\_address). $random(<seed>). Seed is integer, time, or reg. returns a 32-bit signed integer. {$random()} to generate positives. `ifndef <flag>** - compile code between `ifndef and the next `endif only when <flag> is not defined. `**ifdef <flag>** - compile code between `ifdef and the next `endif only when <flag> is defined. **`else** – optional. Specifies path if `ifndef or `ifdef is not taken. Each `ifndef or `ifdef can only have one `else associated with it. **`elsif** – optional. Specifies conditional path if `ifndef or `ifdef is not taken. Each `ifndef or `ifdef any number of `elsif associated with it. **3 kinds of events:** Regular, Non-blocking, Monitor events. **Races:** Read-write, write-write, always-initial. **Synthesis:** process of converting design expressed in RTL into a netlist of gates. **delay chain:** two or more string consecutive nodes with a single fan-in and fan-out to add delay to a path. **Use clock switch-ova instead of mux (logic). don’t use casex and use casez cautiously when synthesizing.** **Design Steps:** structure data path: func. units, identify control points: status and control signals needed, determine control strategy: FSM, decoders, etc, determine reset strategy: what gets initialized, and structure your code. **Divide and remainder synthesizable of power of 2. constant shifts —> wires only. variable shifts —> multiplexing logic. latches —> transparency problem. ROM —> registers in group must have equally spaced taps that are at least 3 registers apart. Seq UDP types —>** Level-sens., Edge-sens. **Reg Retiming:** regs must have same clk, ff may not have both async. set and reset, must be at least 2 levels. **Retiming** can’t change latency. **Soft cores** are slower and simpler than hardcores. **JTAG —> Joint Test Action Group.** TDI, TDO, TCK, TMS, TRST.