10 August 2024 6 صفر 1446

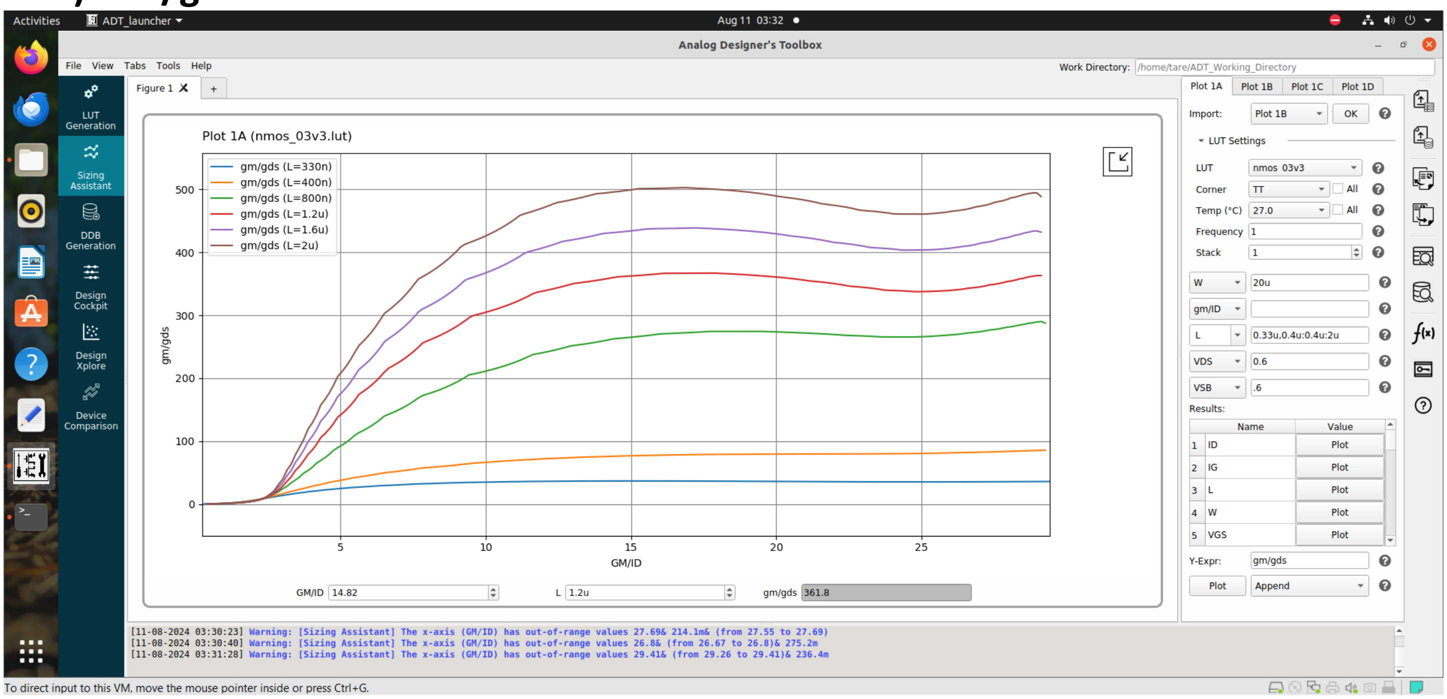
وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

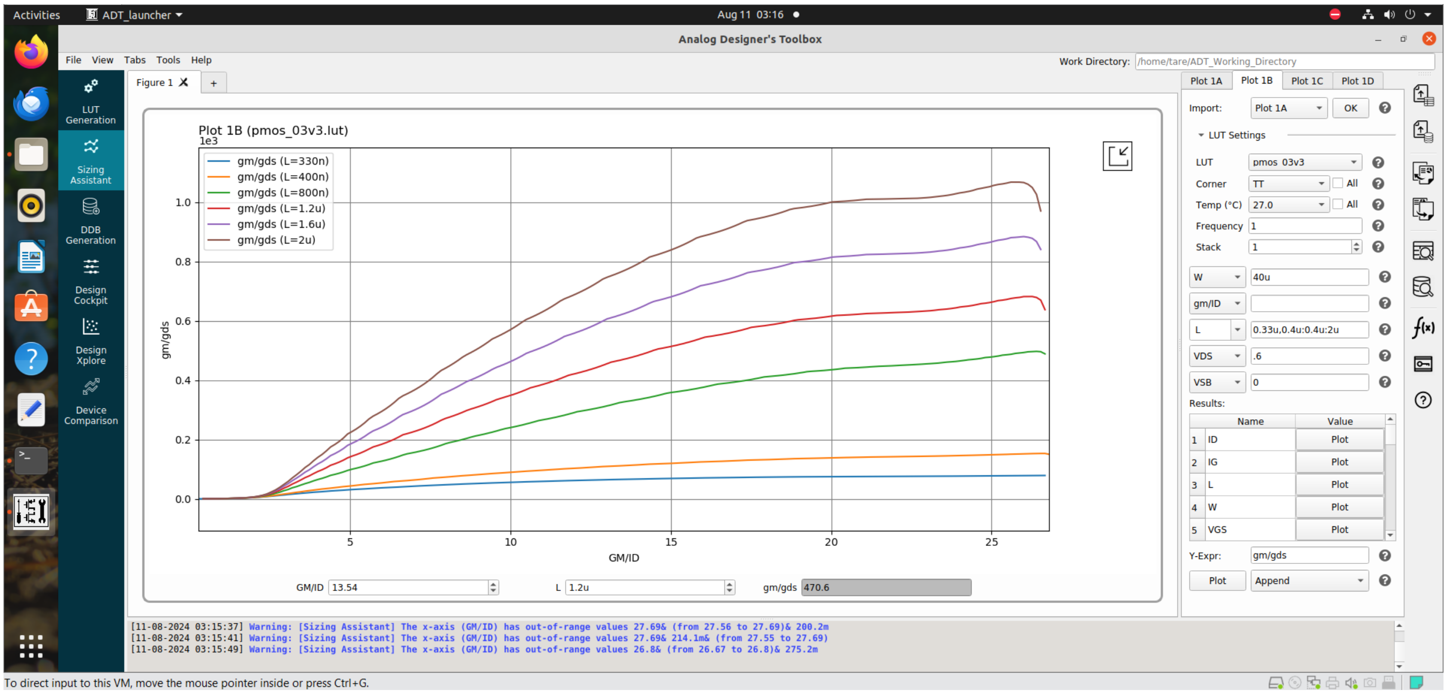
Analog IC Design – Xschem/Ngspice
Lab 07
Gm/ID Design Methodology

PART 1: gm/ID design charts

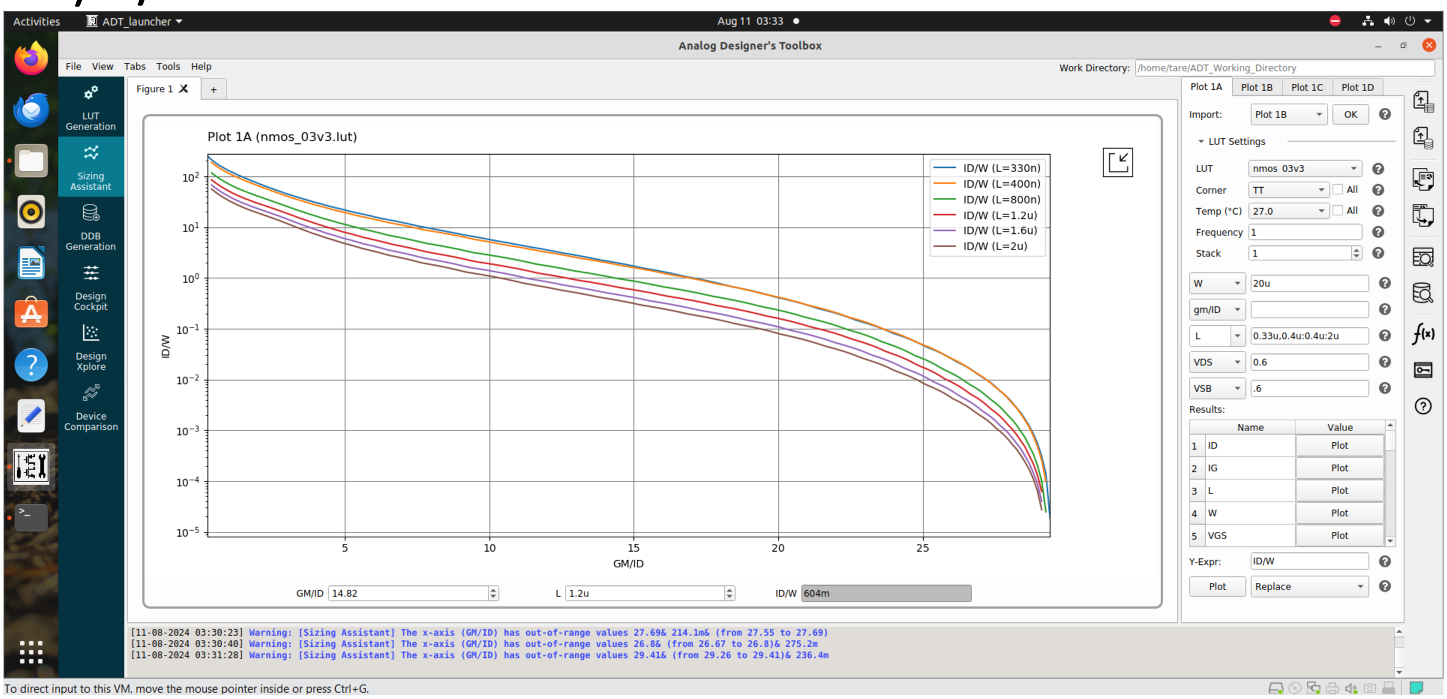
Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS = VDD/3 and L = 0.33u,0.4u:0.4u:2u:

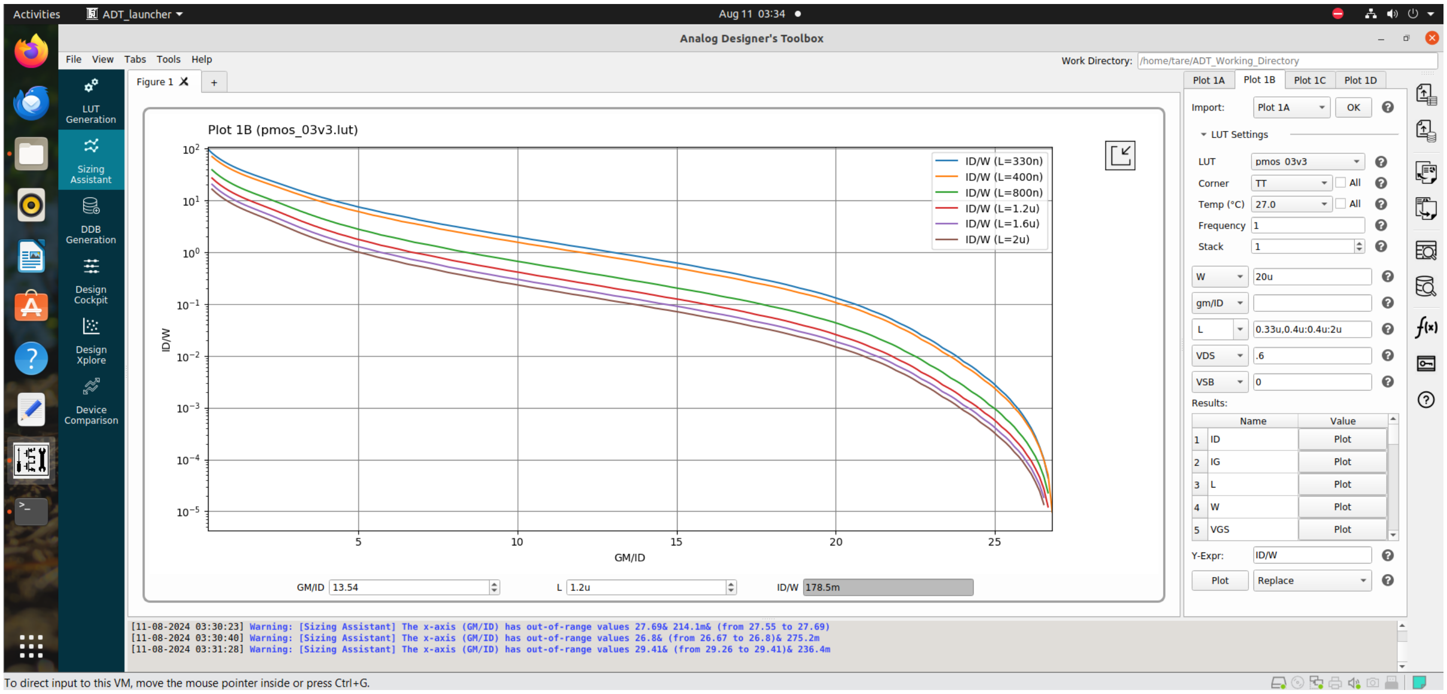
1) Gm/gds



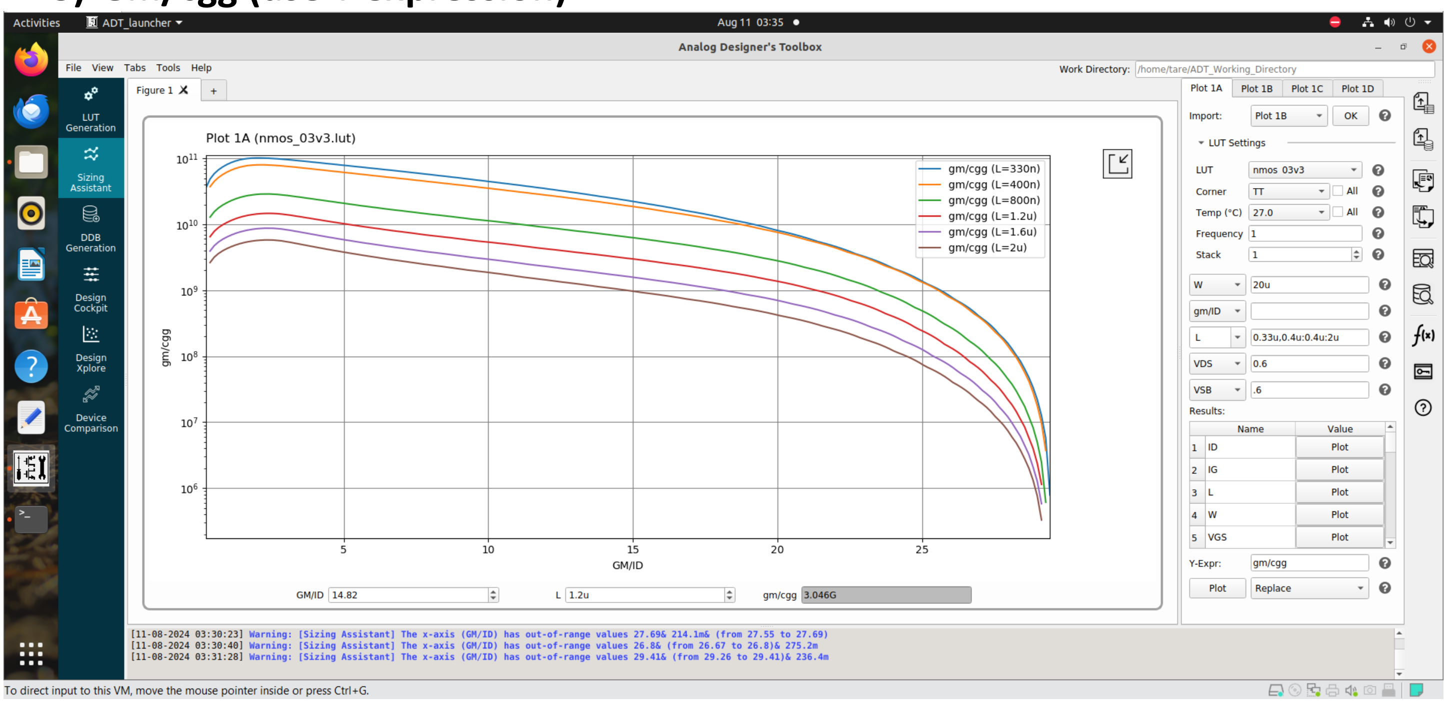

Analog Designer's Toolbox
Plot 1B (pmos_03v3.lut)
1e3
gm/gds (L=330n)
gm/gds (L=400n)
gm/gds (L=800n)
gm/gds (L=1.2u)
gm/gds (L=1.6u)
gm/gds (L=2u)
gm/gds
GM/ID
GM/ID 13.54
L 1.2u
gm/gds 470.6
LUT pmos 03v3
Corner TT
Temp (°C) 27.0
W 40u
L 0.33u,0.4u:0.4u:2u
VDS .6
VSB 0
Y-Expr: gm/gds
[11-08-2024 03:15:37] Warning: [Sizing Assistant] The x-axis (GM/ID) has out-of-range values 27.69& (from 27.56 to 27.69)& 200.2m
[11-08-2024 03:15:41] Warning: [Sizing Assistant] The x-axis (GM/ID) has out-of-range values 27.69& 214.1m& (from 27.55 to 27.69)
[11-08-2024 03:15:49] Warning: [Sizing Assistant] The x-axis (GM/ID) has out-of-range values 26.8& (from 26.67 to 26.8)& 275.2m
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

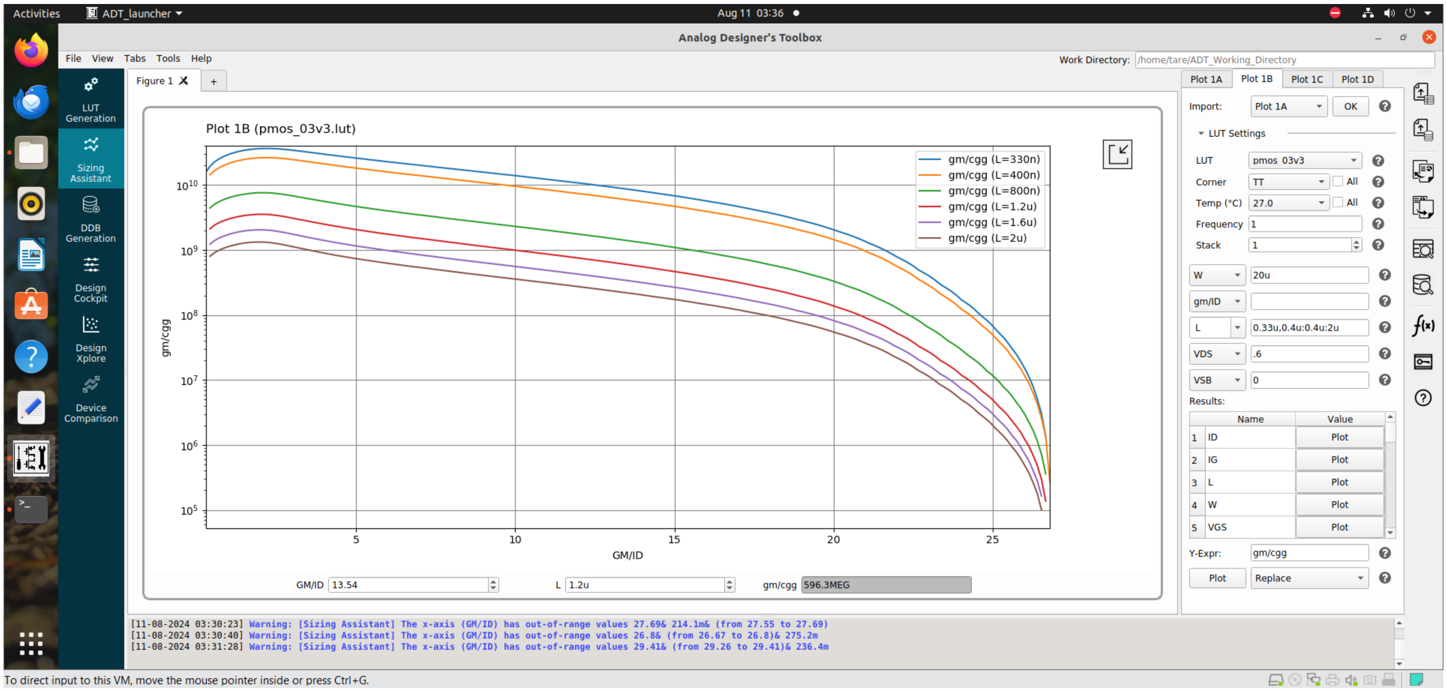
2) ID/W


Analog Designer's Toolbox
Plot 1A (nmos_03v3.lut)
ID/W (L=330n)
ID/W (L=400n)
ID/W (L=800n)
ID/W (L=1.2u)
ID/W (L=1.6u)
ID/W (L=2u)
ID/W
GM/ID
GM/ID 14.82
L 1.2u
ID/W 604m
LUT nmos 03v3
Corner TT
Temp (°C) 27.0
W 20u
L 0.33u,0.4u:0.4u:2u
VDS 0.6
VSB .6
Y-Expr: ID/W
[11-08-2024 03:30:23] Warning: [Sizing Assistant] The x-axis (GM/ID) has out-of-range values 27.69& 214.1m& (from 27.55 to 27.69)
[11-08-2024 03:30:40] Warning: [Sizing Assistant] The x-axis (GM/ID) has out-of-range values 26.8& (from 26.67 to 26.8)& 275.2m
[11-08-2024 03:31:28] Warning: [Sizing Assistant] The x-axis (GM/ID) has out-of-range values 29.41& (from 29.26 to 29.41)& 236.4m
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

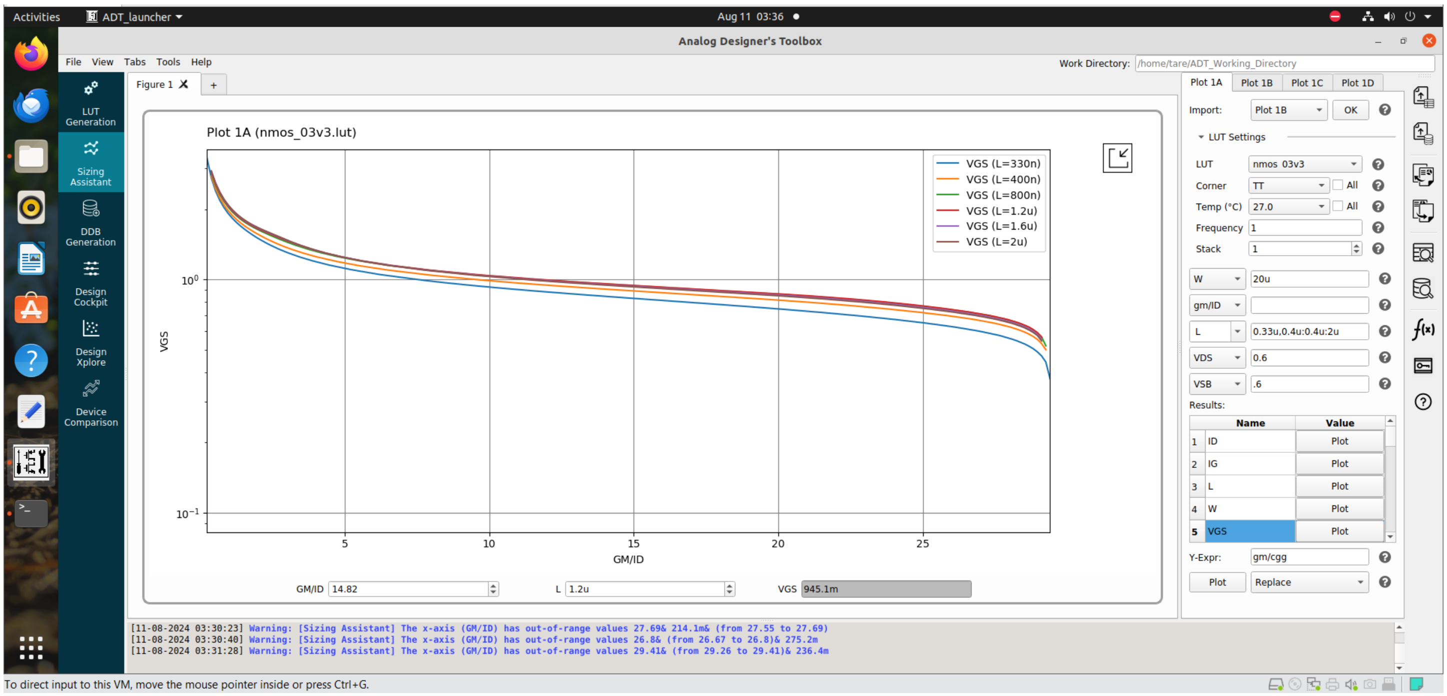


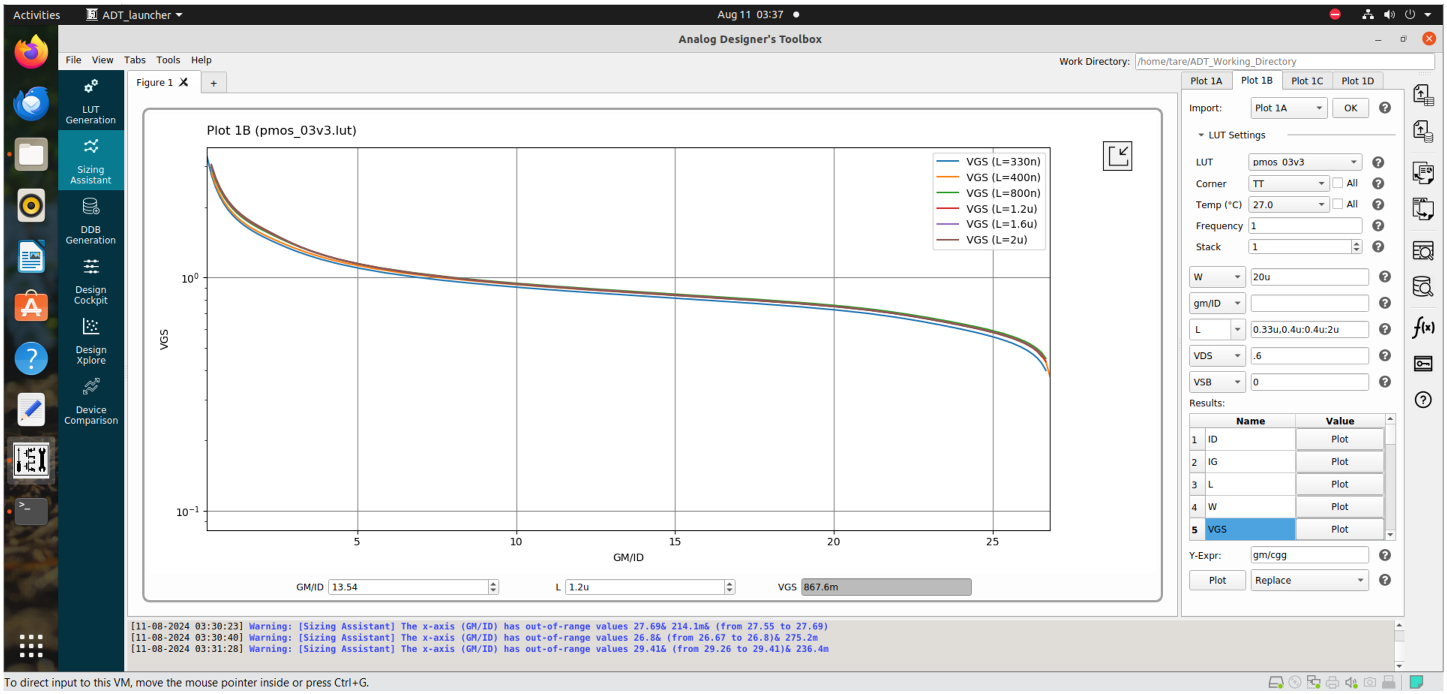
3) Gm/cgg (use Y expression)





4) VGS





Activities
ADT_launcher
Aug 11 03:37
Analog Designer's Toolbox
File View Tabs Tools Help
Work Directory: /home/tare/ADT_Working_Directory
LUT Generation
Sizing Assistant
DDB Generation
Design Cockpit
Design Xplore
Device Comparison
Figure 1
Plot 1B (pmos_03v3.lut)
VGS (L=330n)
VGS (L=400n)
VGS (L=800n)
VGS (L=1.2u)
VGS (L=1.6u)
VGS (L=2u)
VGS
GM/ID
GM/ID 13.54
L 1.2u
VGS 867.6m
Plot 1A
Plot 1B
Plot 1C
Plot 1D
Import: Plot 1A OK
LUT Settings
LUT pmos 03v3
Corner TT All
Temp (°C) 27.0 All
Frequency 1
Stack 1
W 20u
gm/ID
L 0.33u,0.4u:0.4u:2u
VDS .6
VSB 0
Results:
Name Value
1 ID Plot
2 IG Plot
3 L Plot
4 W Plot
5 VGS Plot
Y-Expr: gm/cgg
Plot Replace
[11-08-2024 03:30:23] Warning: [Sizing Assistant] The x-axis (GM/ID) has out-of-range values 27.69& 214.1m& (from 27.55 to 27.69)
[11-08-2024 03:30:40] Warning: [Sizing Assistant] The x-axis (GM/ID) has out-of-range values 26.8& (from 26.67 to 26.8)& 275.2m
[11-08-2024 03:31:28] Warning: [Sizing Assistant] The x-axis (GM/ID) has out-of-range values 29.41& (from 29.26 to 29.41)& 236.4m
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

Part 2: OTA Design

Use gm/ID methodology to design a diff input SE output operational transconductance amplifier (OTA) that achieves the following specs. Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own current mirror.

Technology	0.13 um CMOS	0.18 um CMOS
Supply Voltage	1.2V	1.8V
Load	5pF	5pF
Open Loop DC Voltage Gain	>= 34dB	>= 34dB
CMRR @ DC	>= 74dB	>= 74dB
Phase Margin	>= 70°	>= 70°
CM input range - low	<= 0.6V	<= 1V
CM input range - high	>= 1V	>= 1.5V
GBW	>= 10MHz	>= 10MHz

Report the following:

1) Detailed design procedure and hand analysis. You need to make reasonable assumptions using g_m/I_d methodology. You need to explain why you chose the architecture that you implemented.

    ✓ As the VICMmax near the VDD rail and the gain is high we will choose 5T_OTA with nmos input pair .

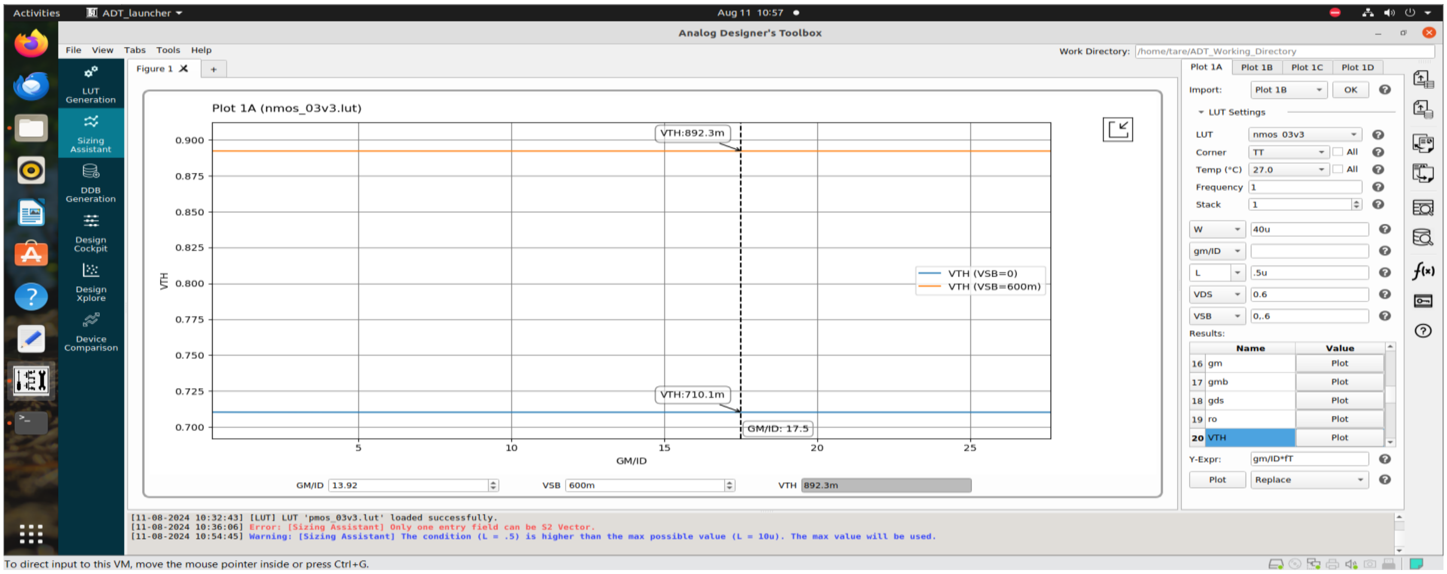
- As GBW≈$\frac{gm1,2}{2\pi * CL}$=10MHz ⟶ gm1,2=315uS ,as we not include the parasitic capacitances at the output node we use a slightly higher gm1,2 ⟶ gm1,2=350uS.
- As Av=gm1,2*(ro2||ro4) , assume ro1=ro2 ⟶ Av=gm1,2*($\frac{ro2}{2}$)=gm1,2/2*gds1,2

  As Av>=50 ⟶ gm1,2/gds1,2>=100.

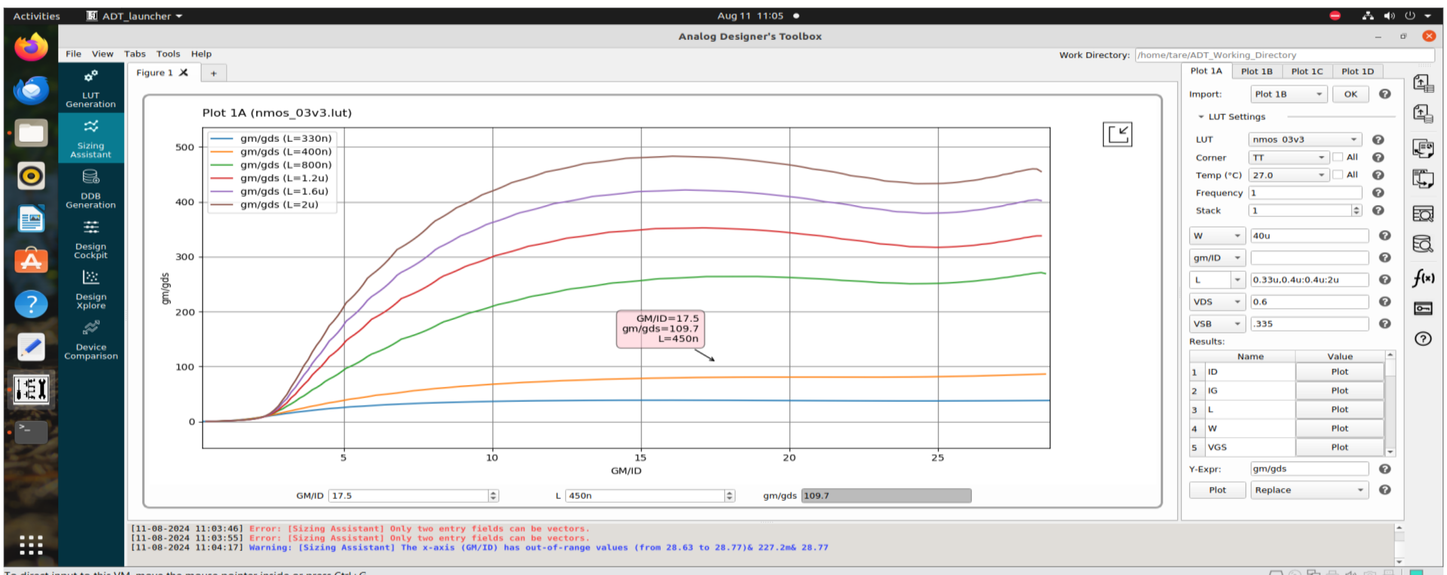
- As gm/ID=10:20 , if we assume ID=20uA ⟶ (gm/ID)1,2=17.5uA.
- As the source of the input pair is floating we should include body effect into account ,so that as gm/ID=17.5 ⟶ V*=115mV , as VTH0=710mV ,(VTH=892mV @VSB=.6V).

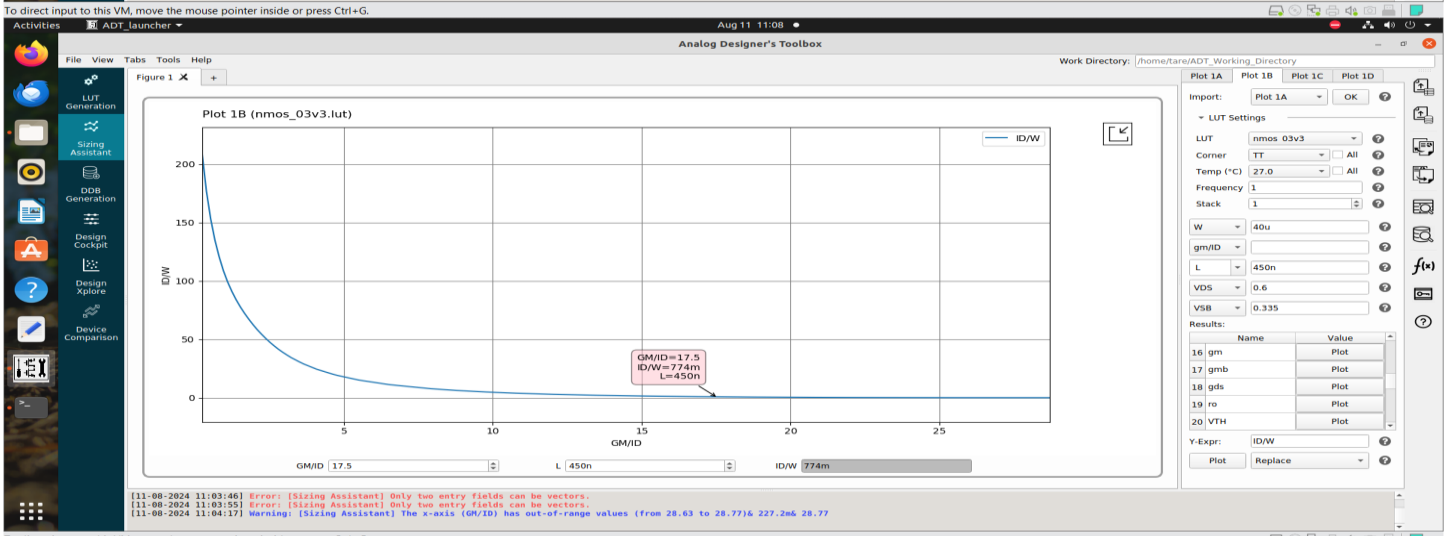
  So that we can estimate the value VSB , if VICM=1.25V ,V*1=115mV ,VTH≈.8V ,VGS1,2≈915mV

  Then VSB1=VDS5=.335V=335mV.

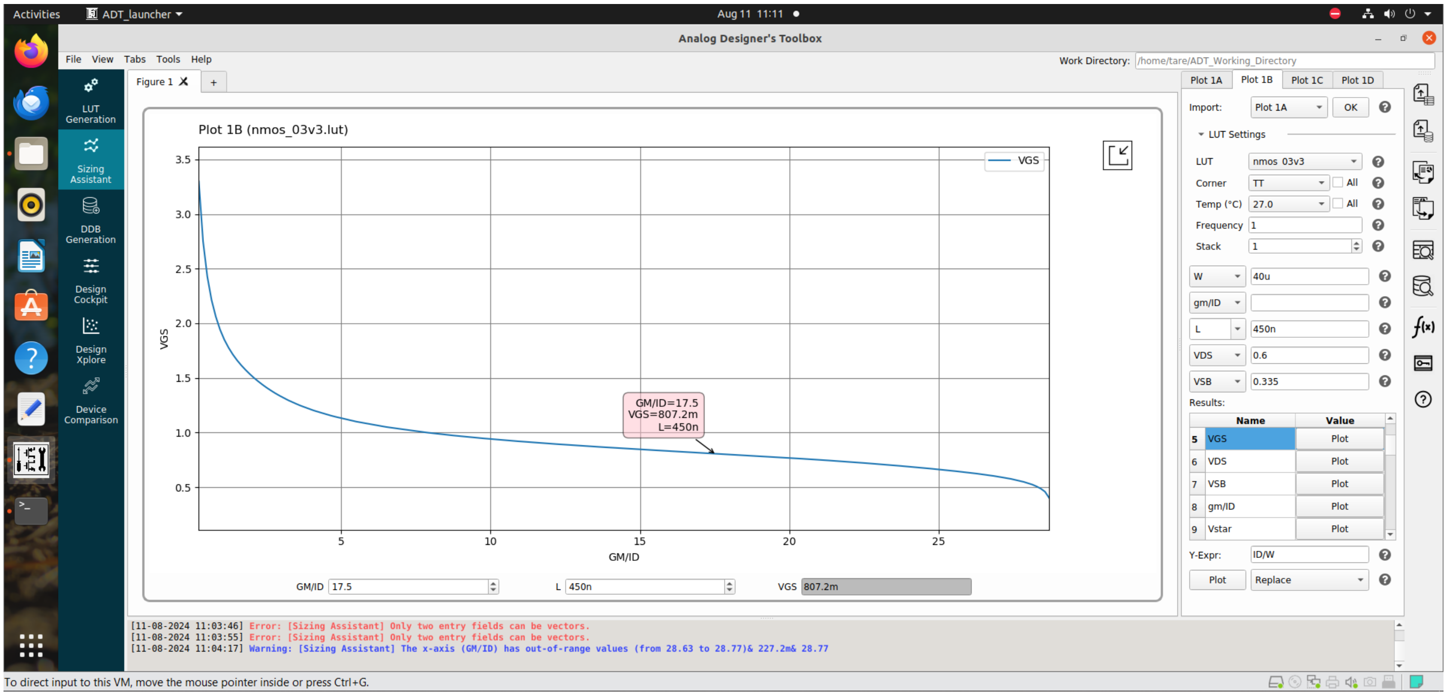


- To achieve (gm/gds)1,2>=100 , then L1,2=450nm.





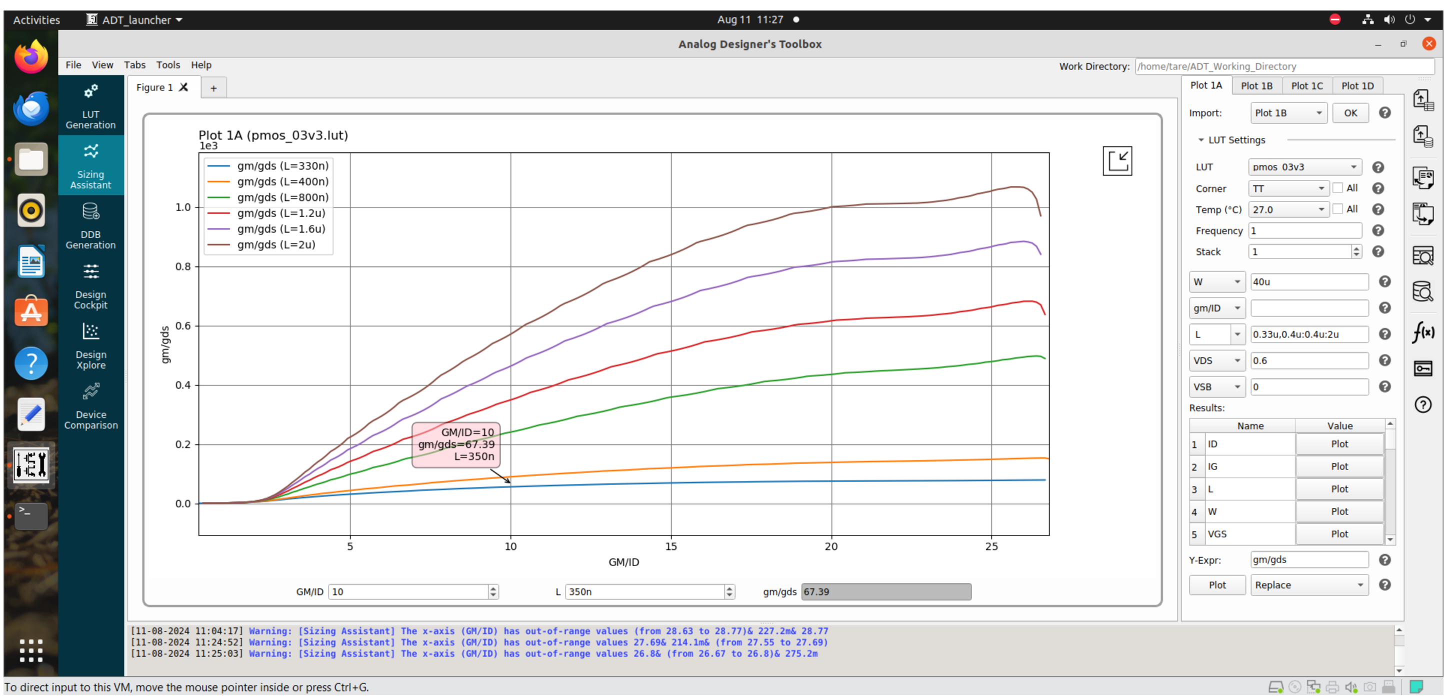
- As ID=20uA ,then W1,2=25.84um.

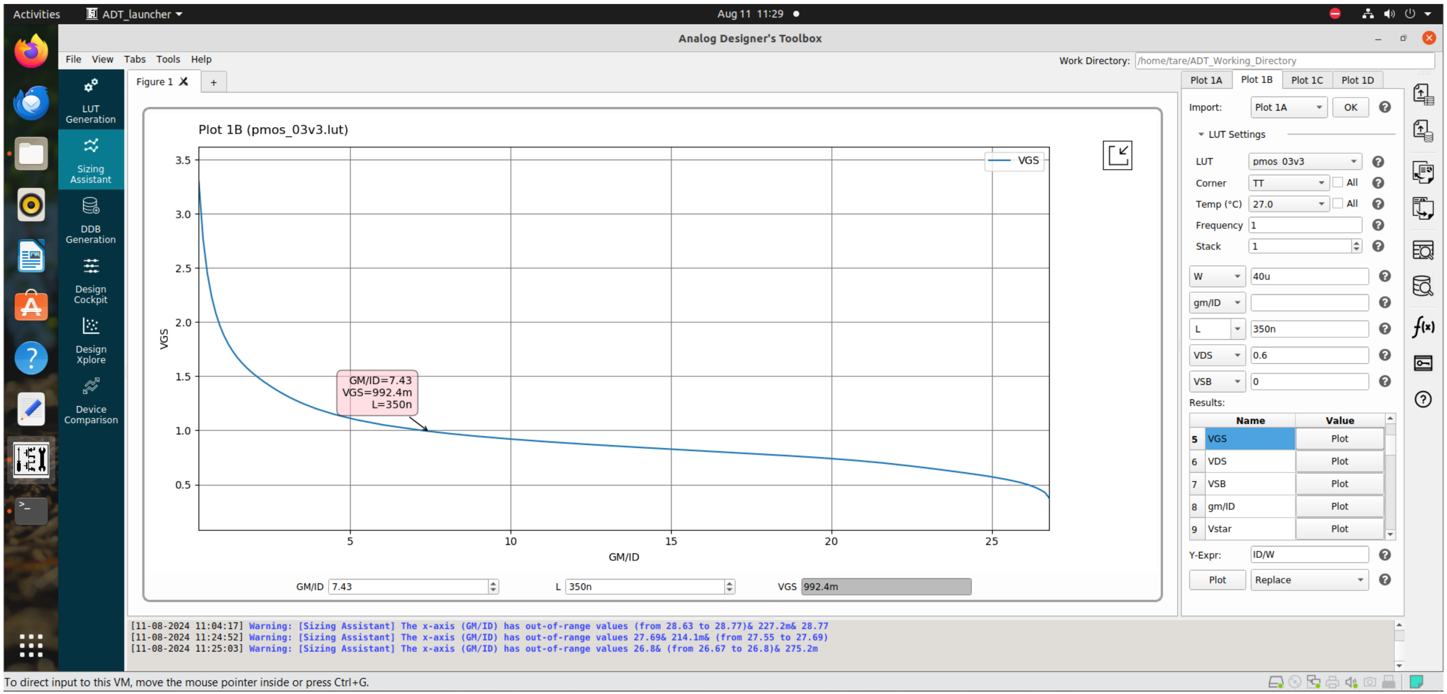


VGS1,2=807.3mV.

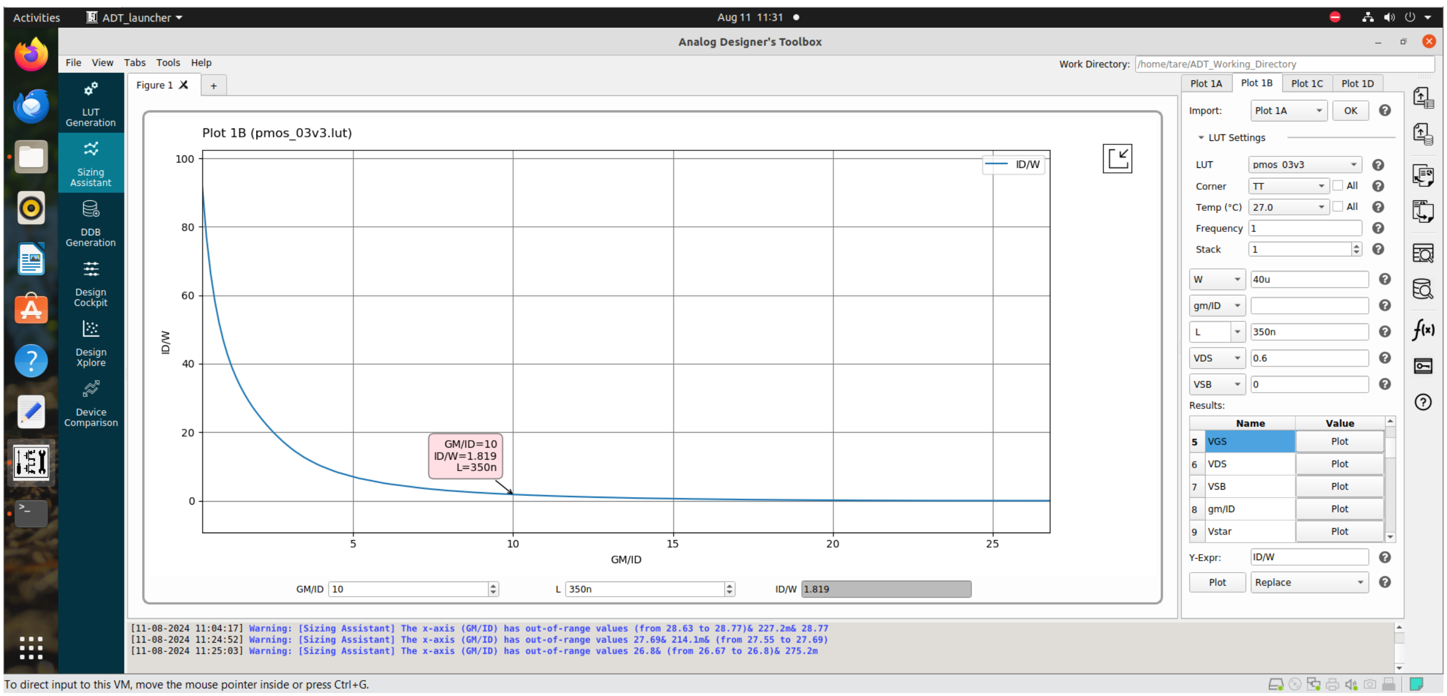
- As gds1,2=gds3,2=3.5uS , ID=20uA.
- As VICMmax=VDD-|VGS3,4|+(VGS1,2-V*1,2)>=1.5 , then |VGS3,4|=<.993V.
- For the load CM to achieve small area and large ro , we choose small gm/ID=10 (strong inversion) .
- So that gm =200uS, gm/gds=>58.

So that L3,4=350nm.





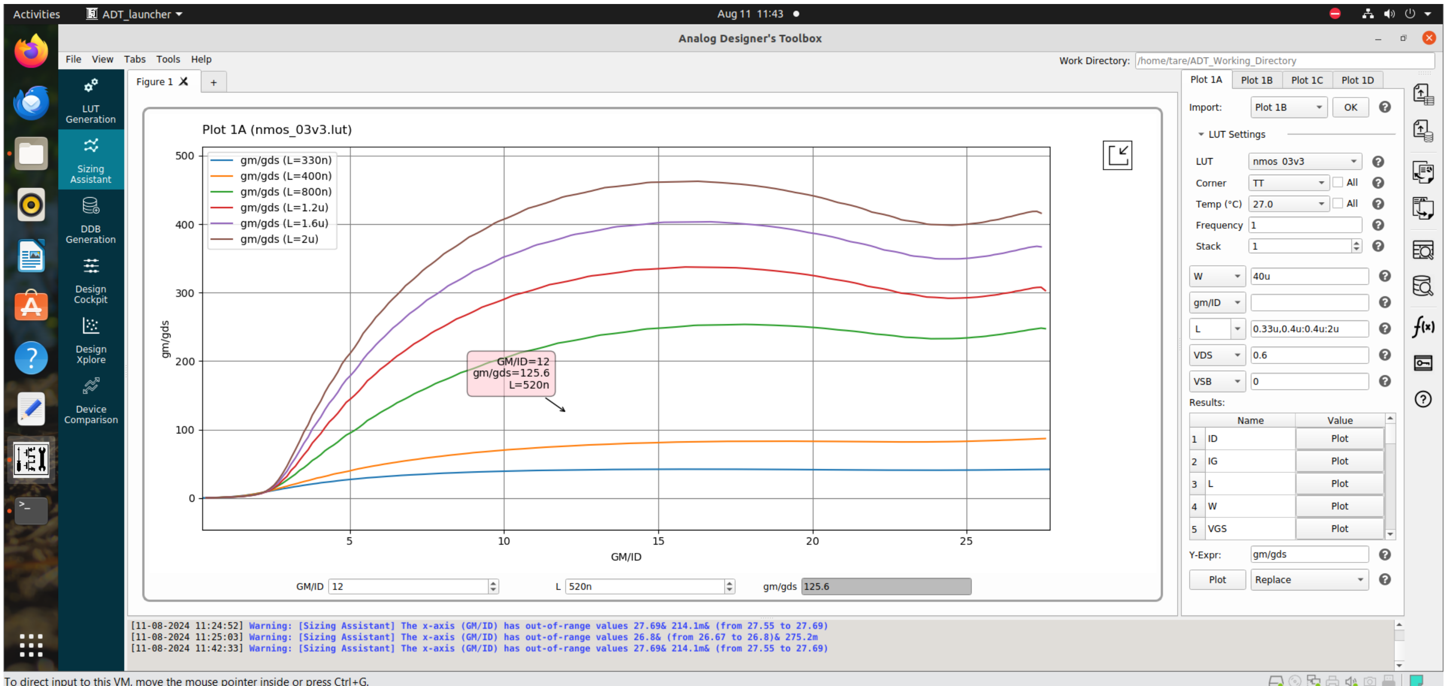
- The minimum (gm/ID)=7.43 ,so that (gm/ID)=10 is good choice.

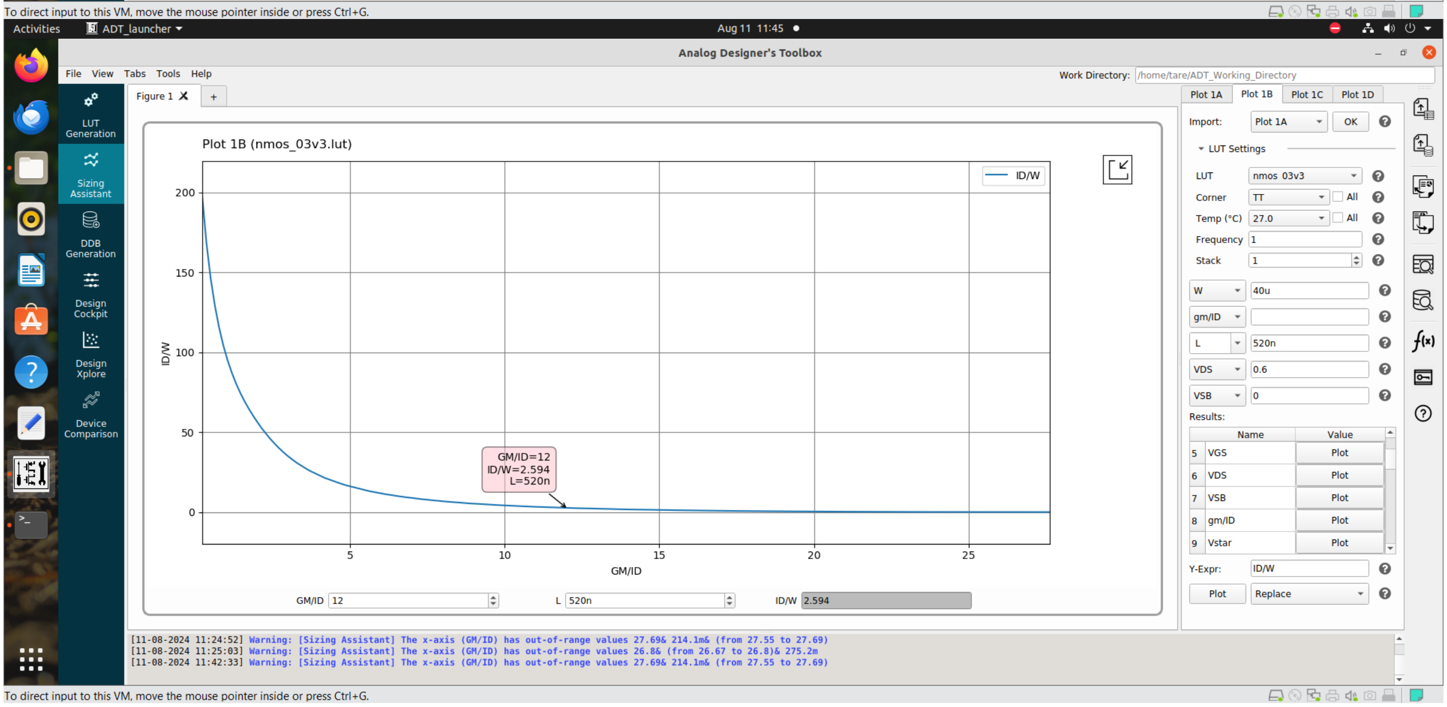


As ID=20um , W3,4=11um.

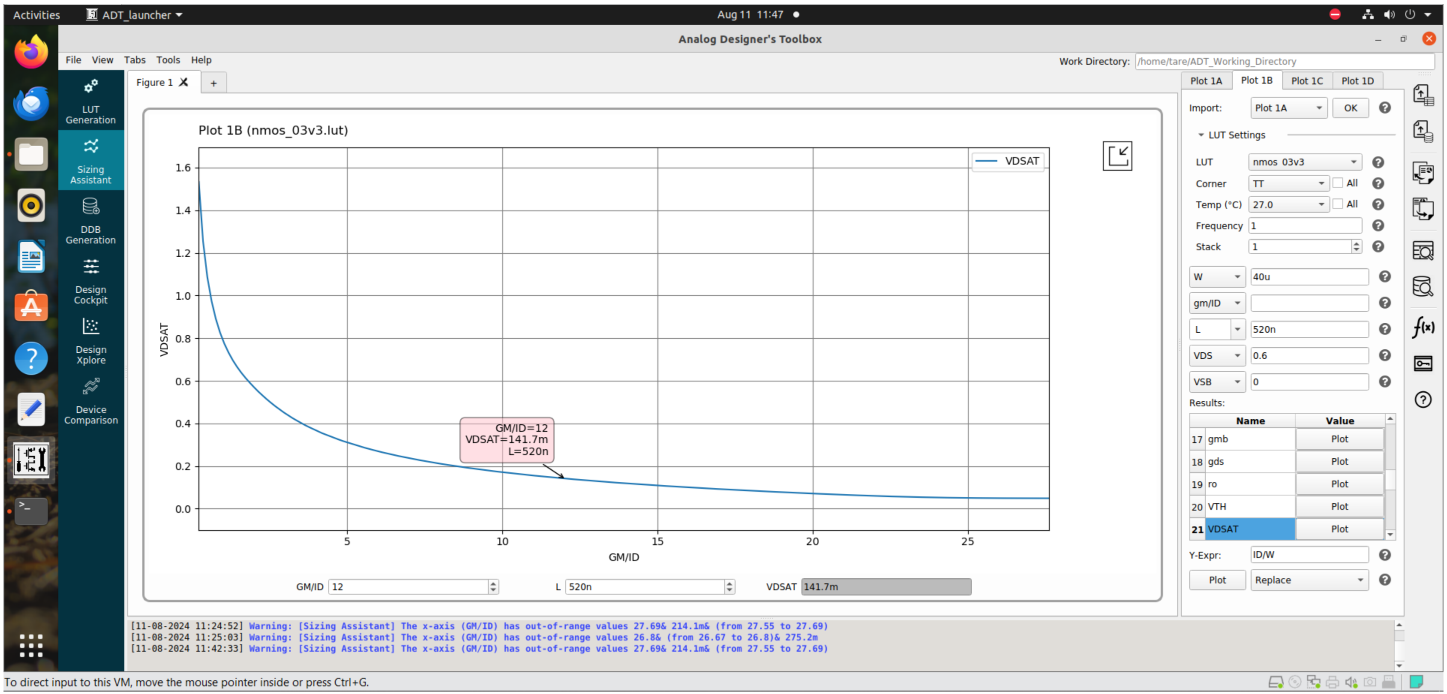
- As Avcm≈gds5/2gm3,4<=.01 , then gds5<=4uS .
- As VICMmim=VGS1,2+VDsat5<=1V , VDsat5<=192.8mV if we use V*5 as an estimate for VDsat5, then V*<= 192.8mV ⟶ (gm/ID)5>=10.4.
- If we choose (gm/ID)5=12 and ID=40uA , then gm=480uS ,(gm/gds)5>=120.

Then L5=520nm.





As ID=40uA ,W5=15.42um.

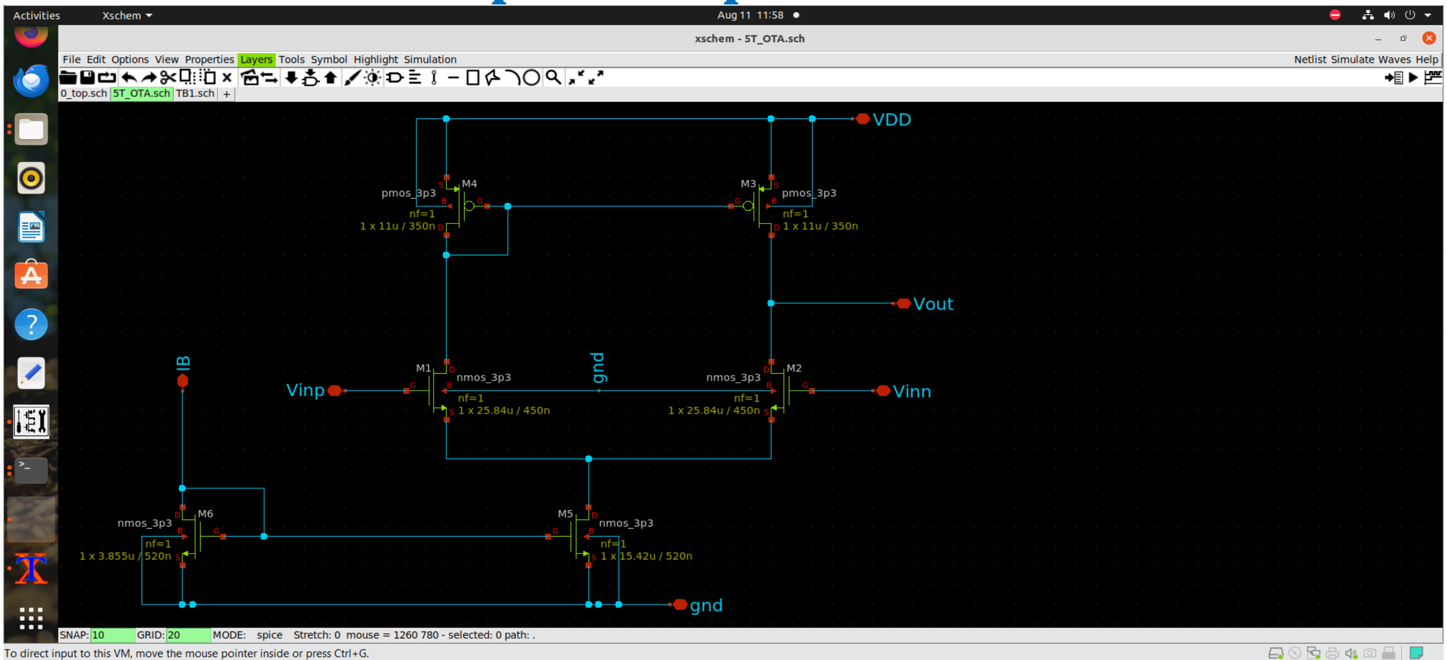


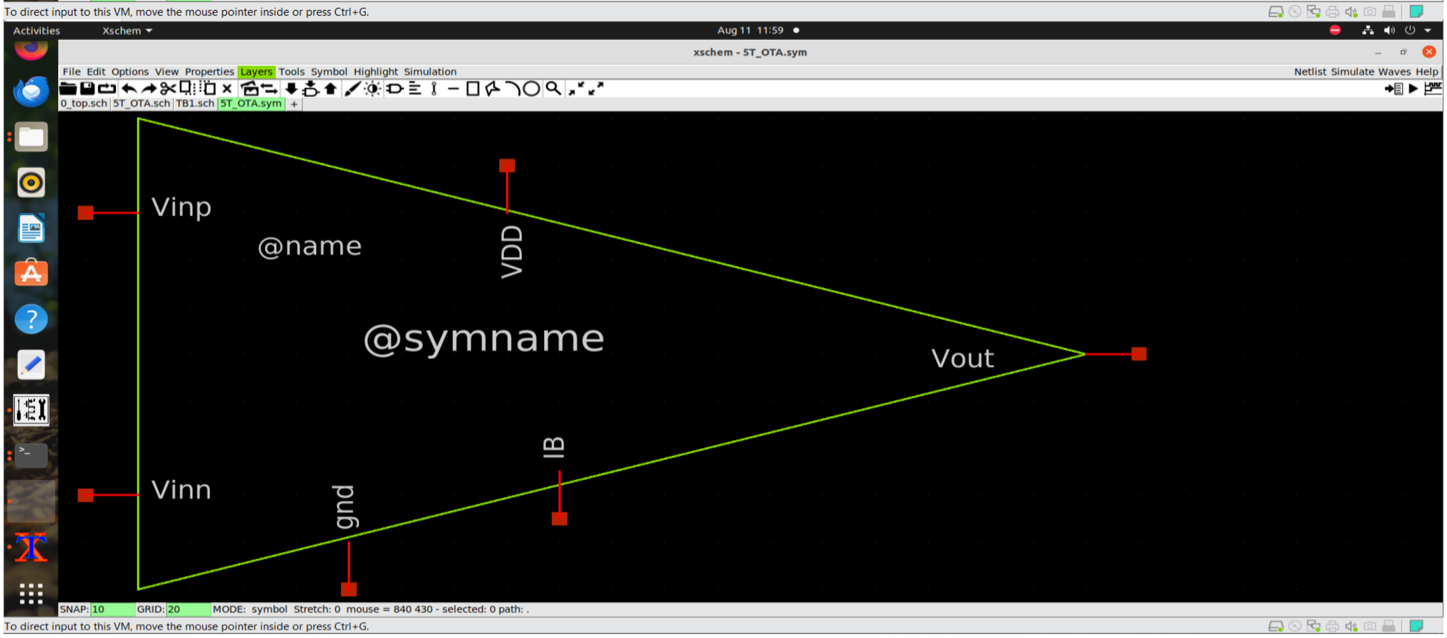
VDsat5=141.7mV ,which is meet the required spec.

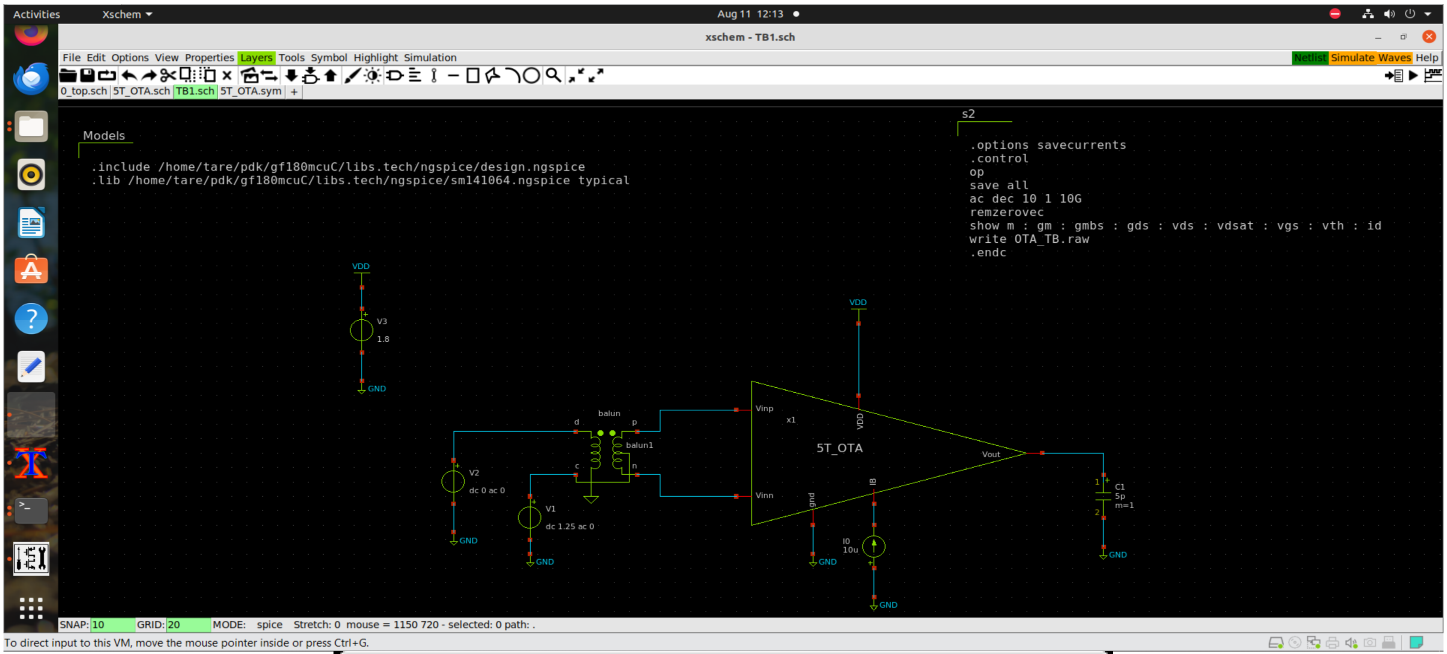
2) A table showing W, L, g_m, I_d , g_m/I_d , V_{dsat}, V_{ov}= V_{gs}-V_{th} , and V_*=2*g_m/I_d of all transistors (as calculated from gm/ID curves).

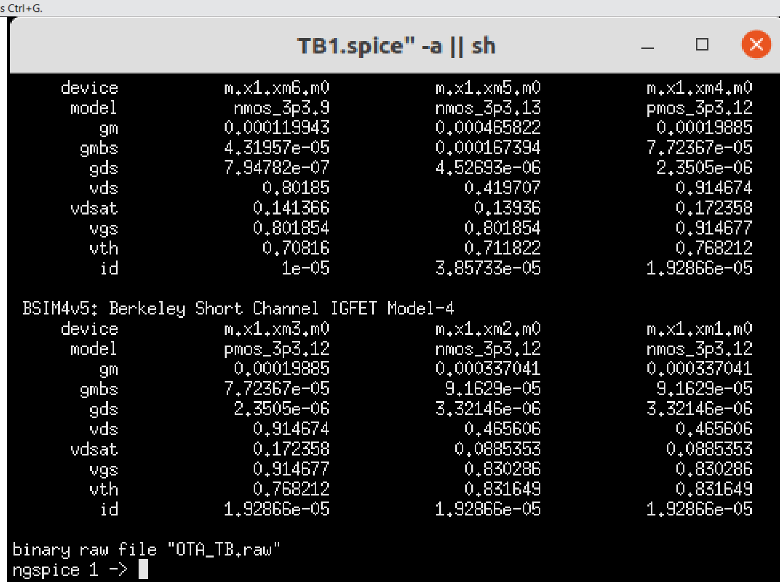
	M1,2	M3,4	M5
W	25.84um	11um	15.42um
L	450nm	350nm	520nm
Gm	350uS	200uS	480uS
ID	20uA	20uA	40uA
Gm/ID	17.5S/A	10S/A	12S/A
VDsat	89.09mV	178.8mV	141.7mV
Vov	1.4mV	153.9mV	94.1mV
V*	115mV	200mV	167mV

Part 3: Open - loop OTA simulation



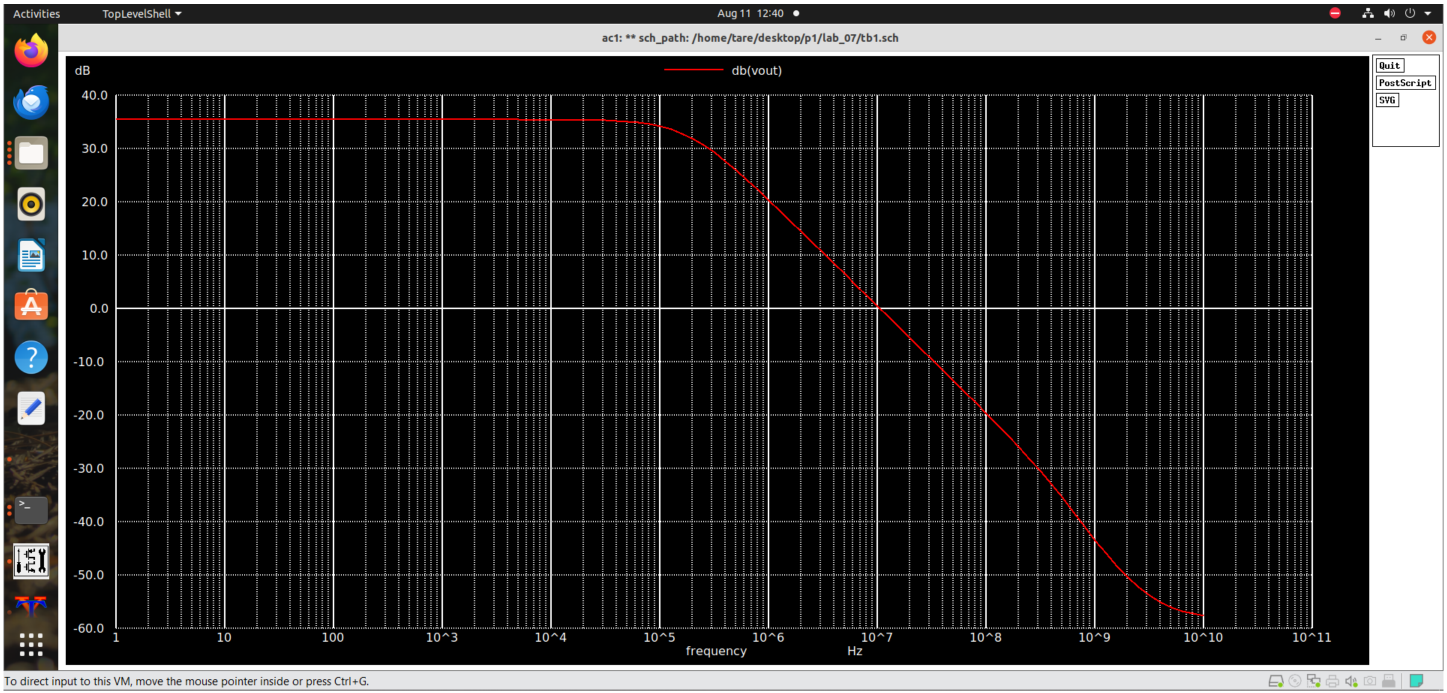


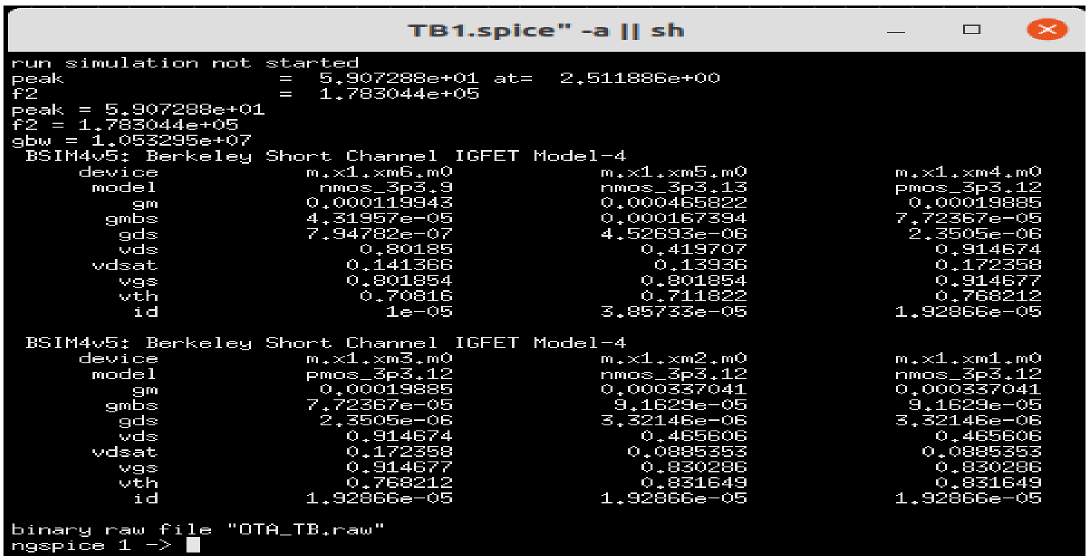




Create a testbench as shown above. Note that IDC connection (sinking or sourcing) in the test bench may be different from the one shown above depending on the type of your input pair (PMOS/NMOS). Report the following:

1) **Schematic of the OTA showing sizing of the transistors:**
   - **Use VICM at the middle of the CMIR and show the operating points.**
   - **Is the current (and gm) in the input pair exactly equal?**
     - ✓ **Yes ,gm of the input pair is exactly equal.**
   - **What is DC voltage at VOUT? Why?**
     - ✓ **Vout=VDD-VDS3=885.33mV , which is equal to the Voltage at the mirror node, as the output node follow the mirror node.**
2) **Diff small signal ccs:**
   - **Use AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).**
   - **Set VIDAC = 1 and VICMAC = 0.**
   - **Use VICM at the middle of the CMIR.**
   - **Plot diff gain (in dB) vs frequency.**





```
TB1.spice" -a || sh
run simulation not started
peak                 =  5.907288e+01 at=  2.511886e+00
f2                   =  1.783044e+05
peak = 5.907288e+01
f2 = 1.783044e+05
gbw = 1.053295e+07
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm6.m0          m.x1.xm5.m0          m.x1.xm4.m0
      model          nmos_3p3.9           nmos_3p3.13          pmos_3p3.12
         gm          0.000119943          0.000465822          0.00019885
       gmbs          4.31957e-05          0.000167394          7.72367e-05
        gds          7.94782e-07          4.52693e-06          2.3505e-06
        vds          0.80185              0.419707             0.914674
      vdsat          0.141366             0.13936              0.172358
        vgs          0.801854             0.801854             0.914677
        vth          0.70816              0.711822             0.768212
         id          1e-05                3.85733e-05          1.92866e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm3.m0          m.x1.xm2.m0          m.x1.xm1.m0
      model          pmos_3p3.12          nmos_3p3.12          nmos_3p3.12
         gm          0.00019885           0.000337041          0.000337041
       gmbs          7.72367e-05          9.1629e-05           9.1629e-05
        gds          2.3505e-06           3.32146e-06          3.32146e-06
        vds          0.914674             0.465606             0.465606
      vdsat          0.172358             0.0885353            0.0885353
        vgs          0.914677             0.830286             0.830286
        vth          0.768212             0.831649             0.831649
         id          1.92866e-05          1.92866e-05          1.92866e-05

binary raw file "OTA_TB.raw"
ngspice 1 ->
```

- **Compare simulation results with hand calculations in a table.**

Avd= $\frac{\mathbf{gm1,2}}{gds1,2+gds3,4}=\frac{\mathbf{337.04uS}}{3.32uS+2.35uS}$**=59.44V/V=35.48db.**

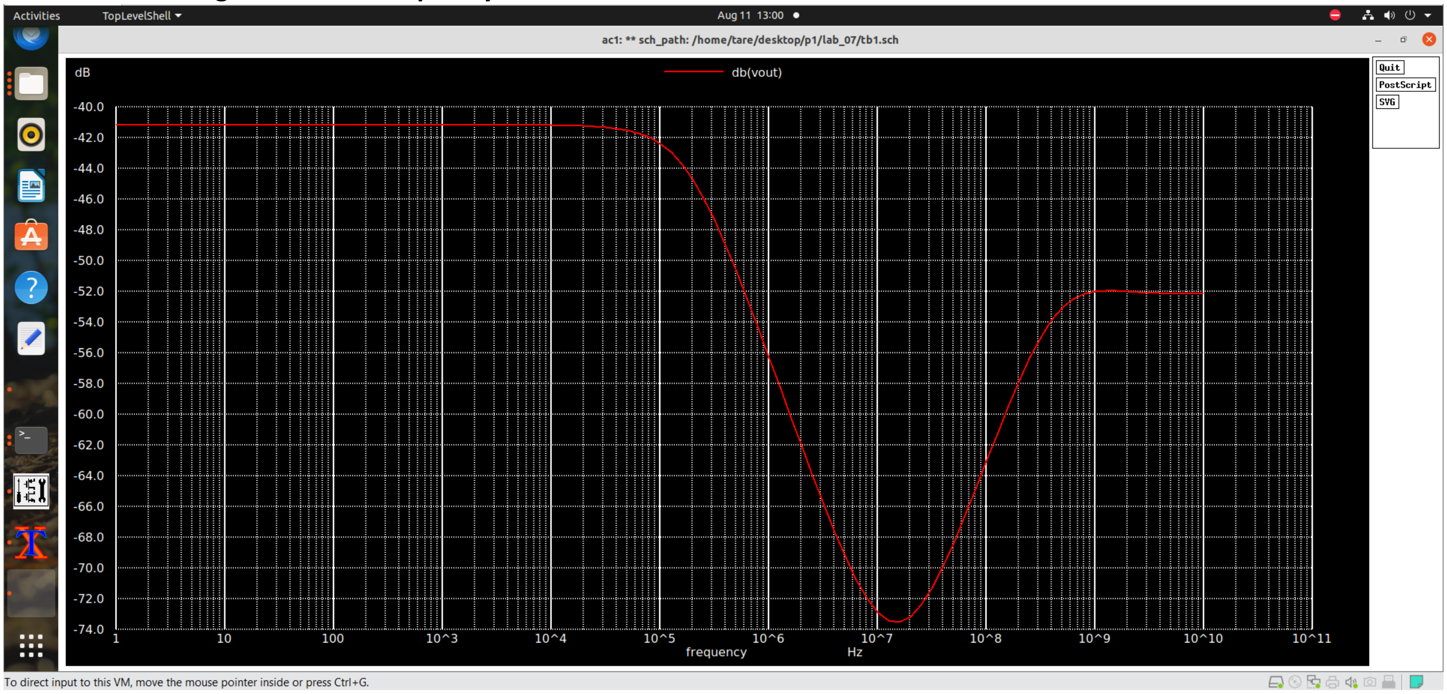
BW=$\frac{gds1,2+gds3,4}{2\pi*CL}=\frac{3.32uS+2.35uS}{2\pi*5pF}$**=180.48KHz.**

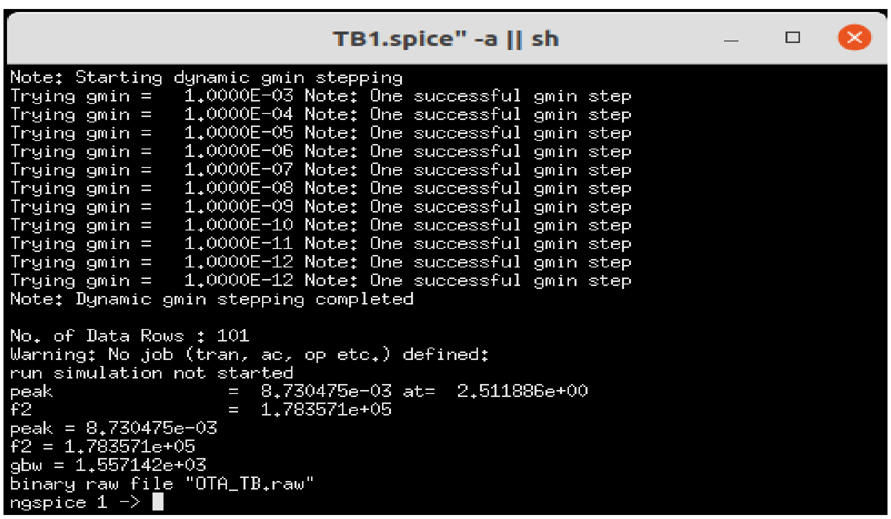
GBW=$\frac{gm1,2}{2\pi*CL}=\frac{\mathbf{337.04uS}}{2\pi*5pF}$ **=10.73MHz.**

	Hand Analysis	Simulation
Avd	**59.44V/V**	**59.07V/V**
BW	**180.48KHz**	**178.304MHz**
GBW	**10.73MHz**	**10.53MHz**

3) CM small signal ccs:

- **Use AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).**
- **Set VICMAC = 1 and VIDAC = 0.**
- **Use VICM at the middle of the CMIR.**
- **Plot CM gain in dB vs frequency.**





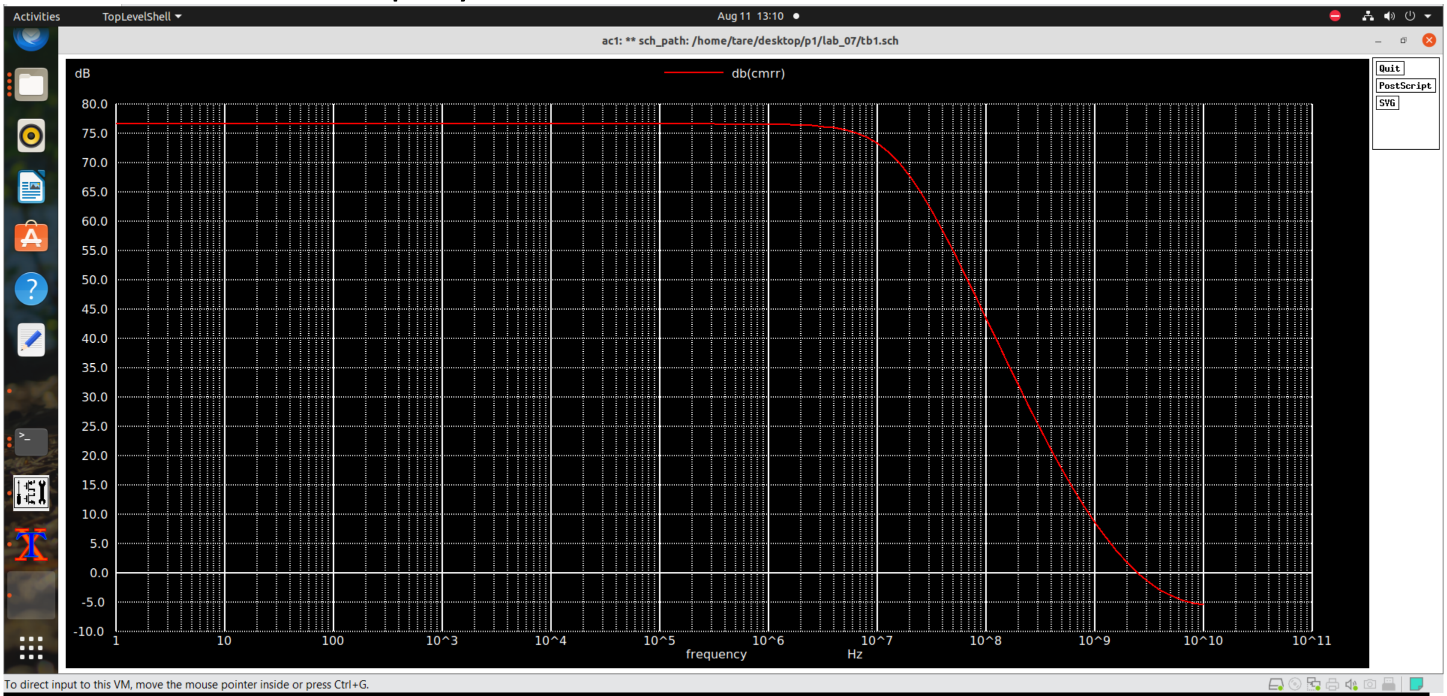
- **Compare simulation results with hand calculations in a table.**

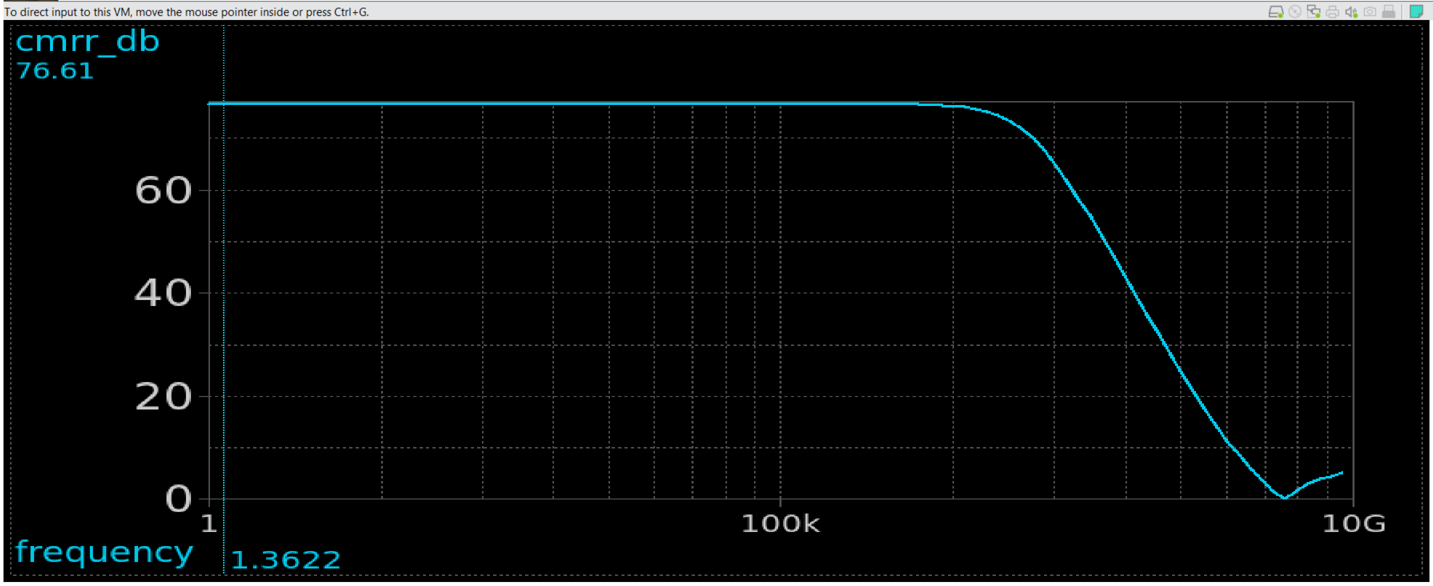
Avcm=$\frac{gds5}{2gm3,4}$**=**$\frac{4.53uS}{2*198.85uS}$ **=11.39mV/V=-38.86db.**

	Hand Analysis	Simulation
Avcm	11.39mV/V=-38.86db	8.37mV/V=-41.18db

4) CMRR:

- Use VICM at the middle of the CMIR.
- Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.



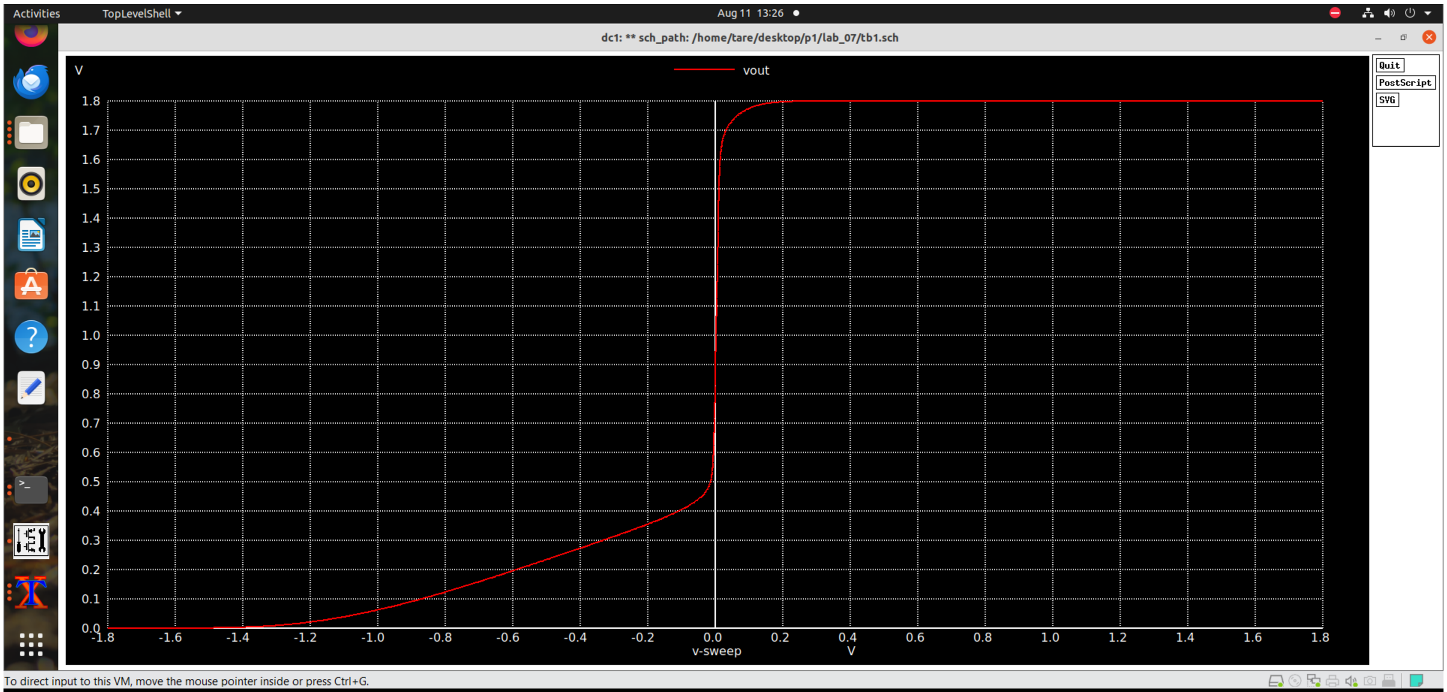


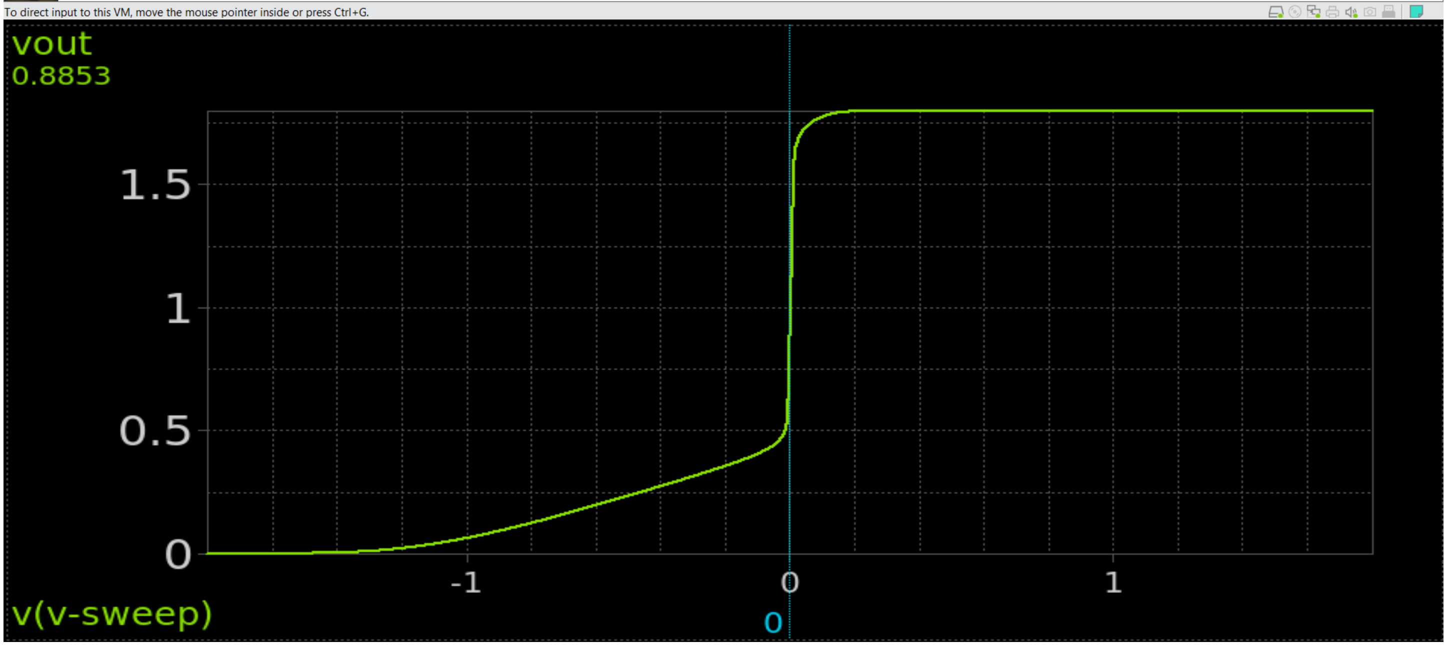
- Compare simulation results with hand calculations in a table.

	Hand Analysis	Simulation
CMRR	5.22KV/V=74.35db	76.61db

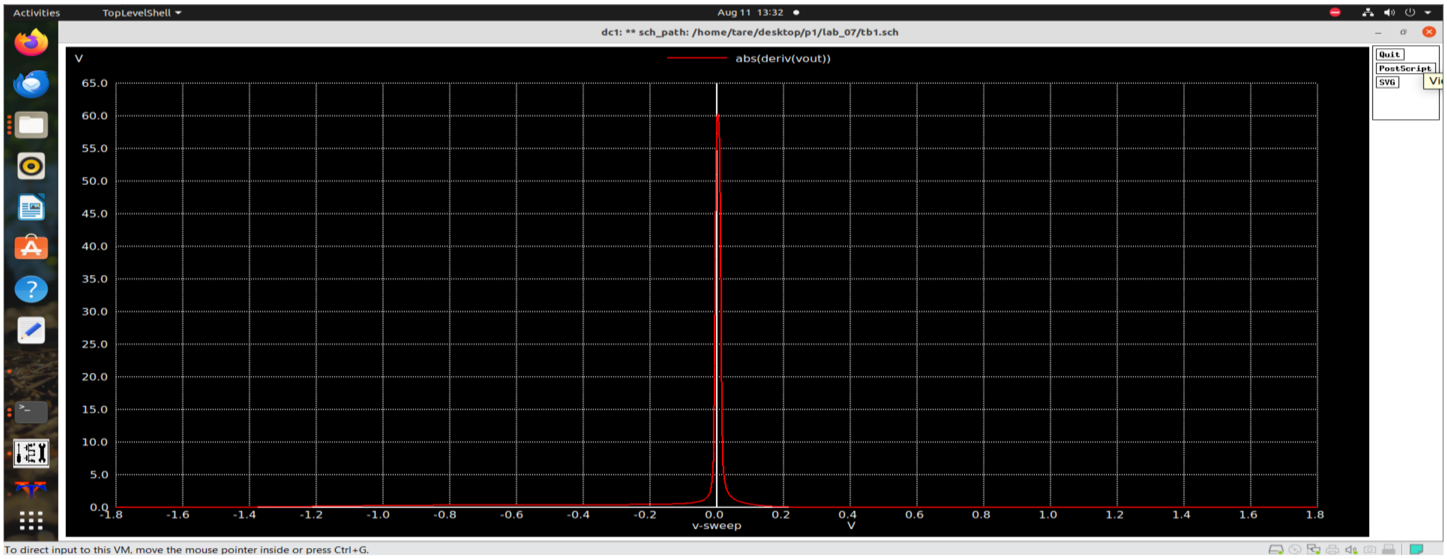
5) Diff large signal ccs:

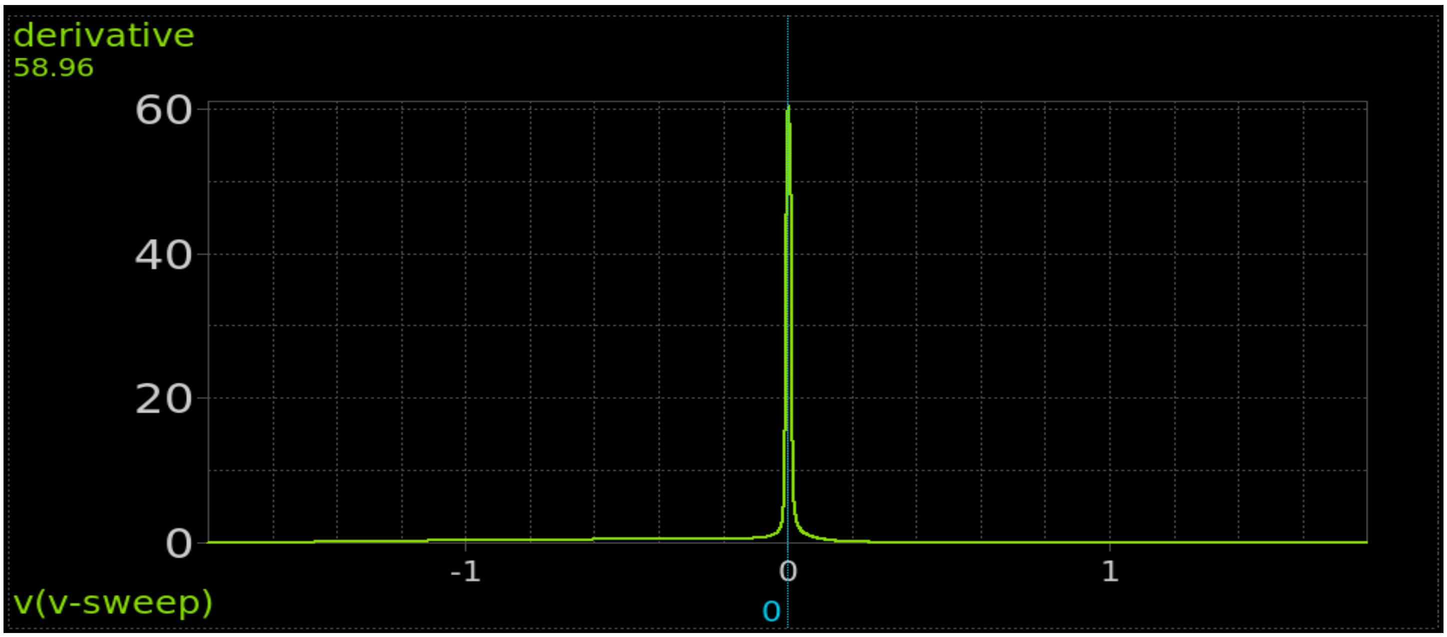
- Use VICM at the middle of the CMIR.
- Use DC sweep (not parametric sweep) VID = -VDD:1m: VDD. You must use a small step (1mV) because the gain region is very small (steep slope).
- Plot VOUT vs VID.

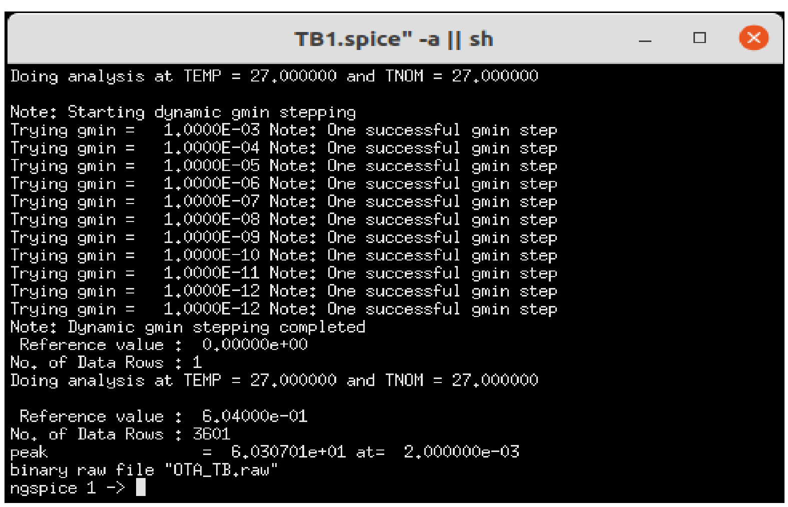




- From the plot, what is the value of Vout at VID = 0? Why?
  - ✓ Vout=.8853V , at VID=0 no differential signal only CM ,so that Vout follow mirror node in the CM so that Vout=885.3mV which is equal to VF.
- Plot the derivative of VOUT vs VID. Compare the peak with Avd.





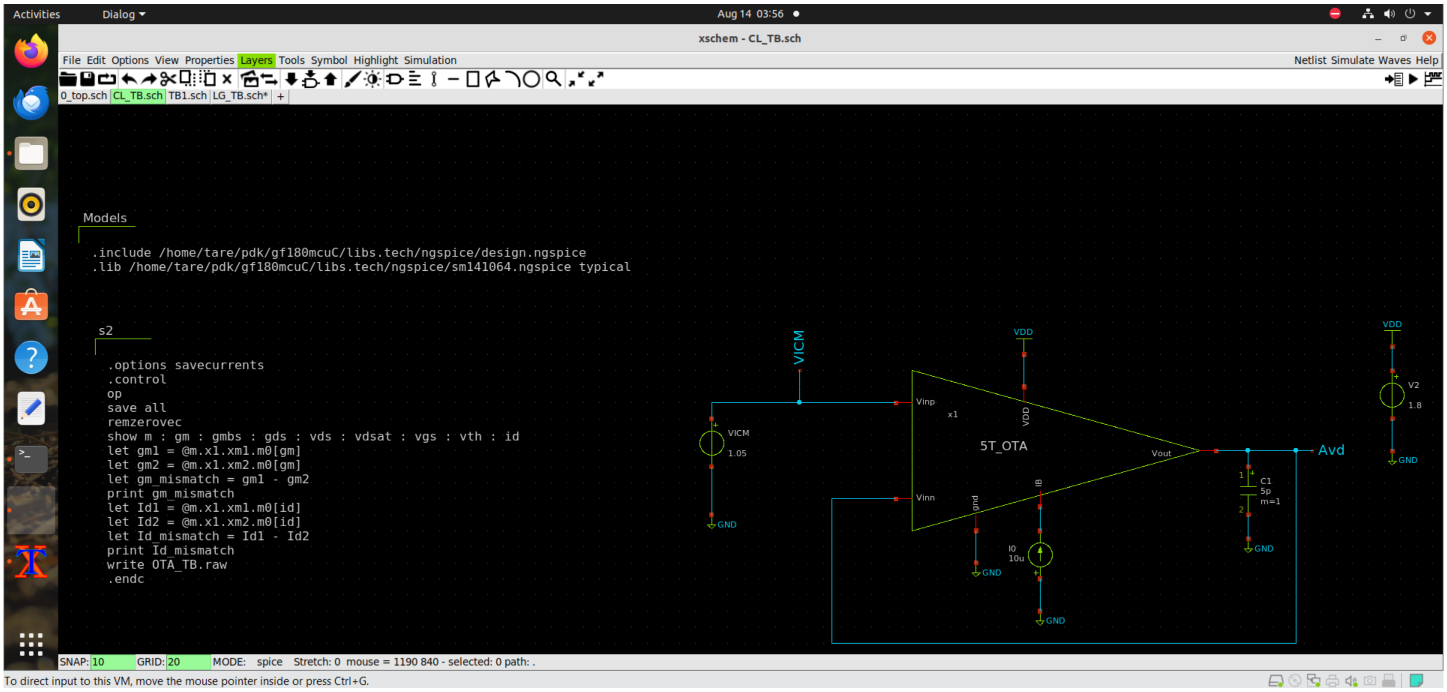


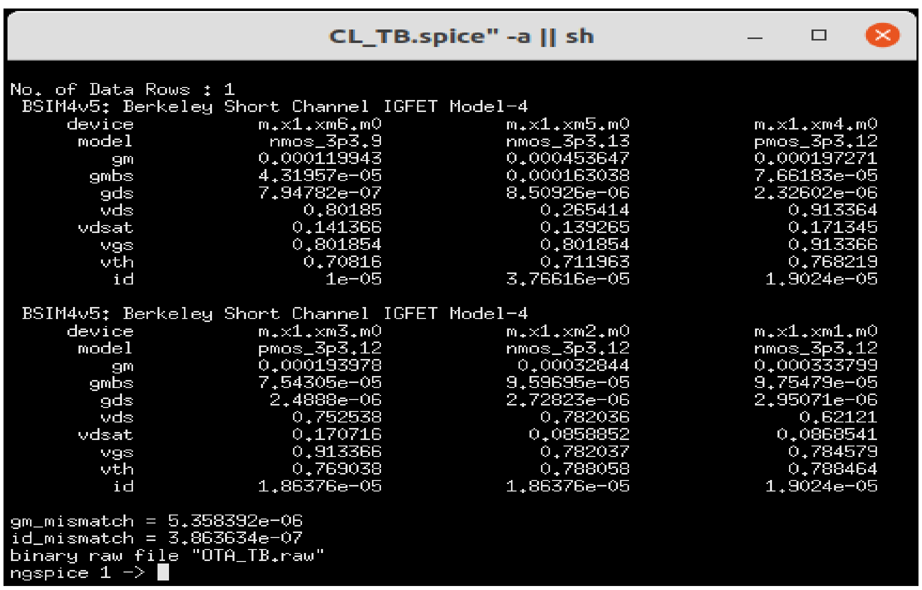
```
TB1.spice" -a || sh
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Note: Starting dynamic gmin stepping
Trying gmin =   1.0000E-03 Note: One successful gmin step
Trying gmin =   1.0000E-04 Note: One successful gmin step
Trying gmin =   1.0000E-05 Note: One successful gmin step
Trying gmin =   1.0000E-06 Note: One successful gmin step
Trying gmin =   1.0000E-07 Note: One successful gmin step
Trying gmin =   1.0000E-08 Note: One successful gmin step
Trying gmin =   1.0000E-09 Note: One successful gmin step
Trying gmin =   1.0000E-10 Note: One successful gmin step
Trying gmin =   1.0000E-11 Note: One successful gmin step
Trying gmin =   1.0000E-12 Note: One successful gmin step
Trying gmin =   1.0000E-12 Note: One successful gmin step
Note: Dynamic gmin stepping completed
 Reference value :  0.00000e+00
No. of Data Rows : 1
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

 Reference value :  6.04000e-01
No. of Data Rows : 3601
peak               =  6.030701e+01 at=  2.000000e-03
binary raw file "OTA_TB.raw"
ngspice 1 ->
```

Deriv(Vout)max=60.307 , which is almost equal to Avd.

PART 4: Closed-Loop OTA Simulation

1) Create schematic of the OTA showing current and gm operating point. Use VINCM = $CMIRlow + 50\ mv$.





```
No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm6.m0          m.x1.xm5.m0          m.x1.xm4.m0
      model          nmos_3p3.9          nmos_3p3.13          pmos_3p3.12
         gm         0.000119943          0.000453647          0.000197271
       gmbs         4.31957e-05          0.000163038          7.66183e-05
        gds         7.94782e-07          8.50926e-06          2.32602e-06
        vds             0.80185             0.265414             0.913364
      vdsat            0.141366             0.139265             0.171345
        vgs            0.801854             0.801854             0.913366
        vth             0.70816             0.711963             0.768219
         id               1e-05          3.76616e-05           1.9024e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm3.m0          m.x1.xm2.m0          m.x1.xm1.m0
      model          pmos_3p3.12          nmos_3p3.12          nmos_3p3.12
         gm         0.000193978           0.00032844          0.000333799
       gmbs         7.54305e-05          9.59695e-05          9.75479e-05
        gds          2.4888e-06          2.72823e-06          2.95071e-06
        vds            0.752538             0.782036              0.62121
      vdsat            0.170716            0.0858852            0.0868541
        vgs            0.913366             0.782037             0.784579
        vth            0.769038             0.788058             0.788464
         id         1.86376e-05          1.86376e-05           1.9024e-05

gm_mismatch = 5.358392e-06
id_mismatch = 3.863634e-07
binary raw file "OTA_TB.raw"
ngspice 1 ->
```

- **Is the current (and gm) in the input pair exactly equal? Why?**
  - ✓ **no gm and ID not exactly equal,as the amplifier has a finite Loop gain then there is some error between the to input this small error generate a small differential signal between the two inputs which cause the errer in gm and id .**
- **Calculate the mismatch in Id and gm.**

As LG≈59.44 , then Verr=$\frac{Vin}{1+LG}$=$\frac{1.25-1.05}{1+59.44}$=3.33mV.

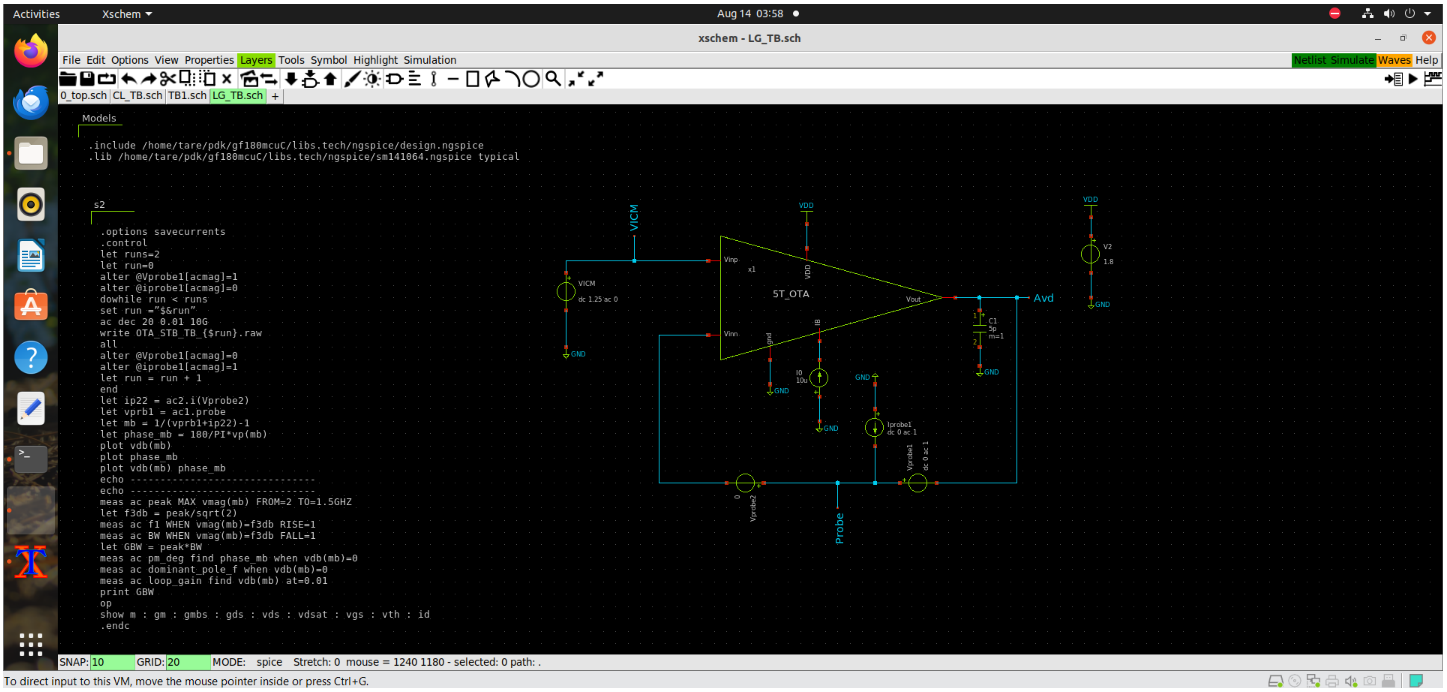
ΔID≈386.4nA.

Δgm≈5.36uS.

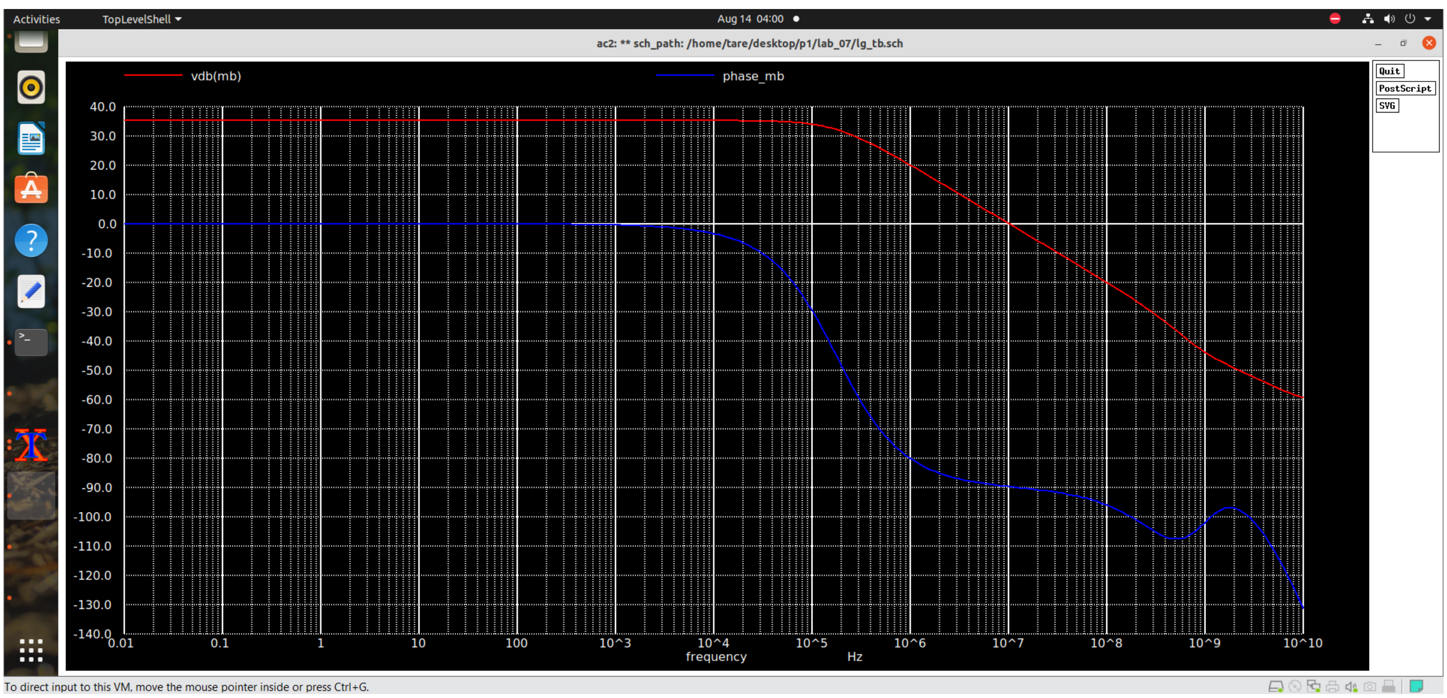
2) Loop Gain:

- **Put the OTA in a unity gain buffer configuration as shown in the schematic below.**

- **Use VICM at the middle of the CMIR.**



- **Plot loop gain in dB and phase vs frequency. Show the results in the console.**



LG_TB.spice" -a || sh

```
meas ac f1 when vmag(mb)=4.118452e+01 rise=1 failed!

bw                  =  1.764202e+05
pm_deg              =  -8.965048e+01
dominant_pole_f     =  1.028223e+07
loop_gain           =  3.530498e+01
gbw = 1.027537e+07
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Note: Starting dynamic gmin stepping
Trying gmin =   1.0000E-03 Note: One successful gmin step
Trying gmin =   1.0000E-04 Note: One successful gmin step
Trying gmin =   1.0000E-05 Note: One successful gmin step
Trying gmin =   1.0000E-06 Note: One successful gmin step
Trying gmin =   1.0000E-07 Note: One successful gmin step
Trying gmin =   1.0000E-08 Note: One successful gmin step
Trying gmin =   1.0000E-09 Note: One successful gmin step
Trying gmin =   1.0000E-10 Note: One successful gmin step
Trying gmin =   1.0000E-11 Note: One successful gmin step
Trying gmin =   1.0000E-12 Note: One successful gmin step
Trying gmin =   1.0000E-12 Note: One successful gmin step
Note: Dynamic gmin stepping completed

No. of Data Rows : 1
```

- **Compare DC gain and GBW with those obtained from open-loop simulation.**

	Open-Loop	Closed-Loop
DC gain	35.43db	35.5db
GBW	10.53MHz	10.3MHz

Comment.

✓ As $\boldsymbol{\beta}$=1 , then Loop gain=open loop gain , as we see LG roughly equal the open loop gain .

✓ As $\boldsymbol{\beta}$=1 , then the GBWoL=GBWcL .

- **Show the operating point at VICM in the middle of the CMIR.**

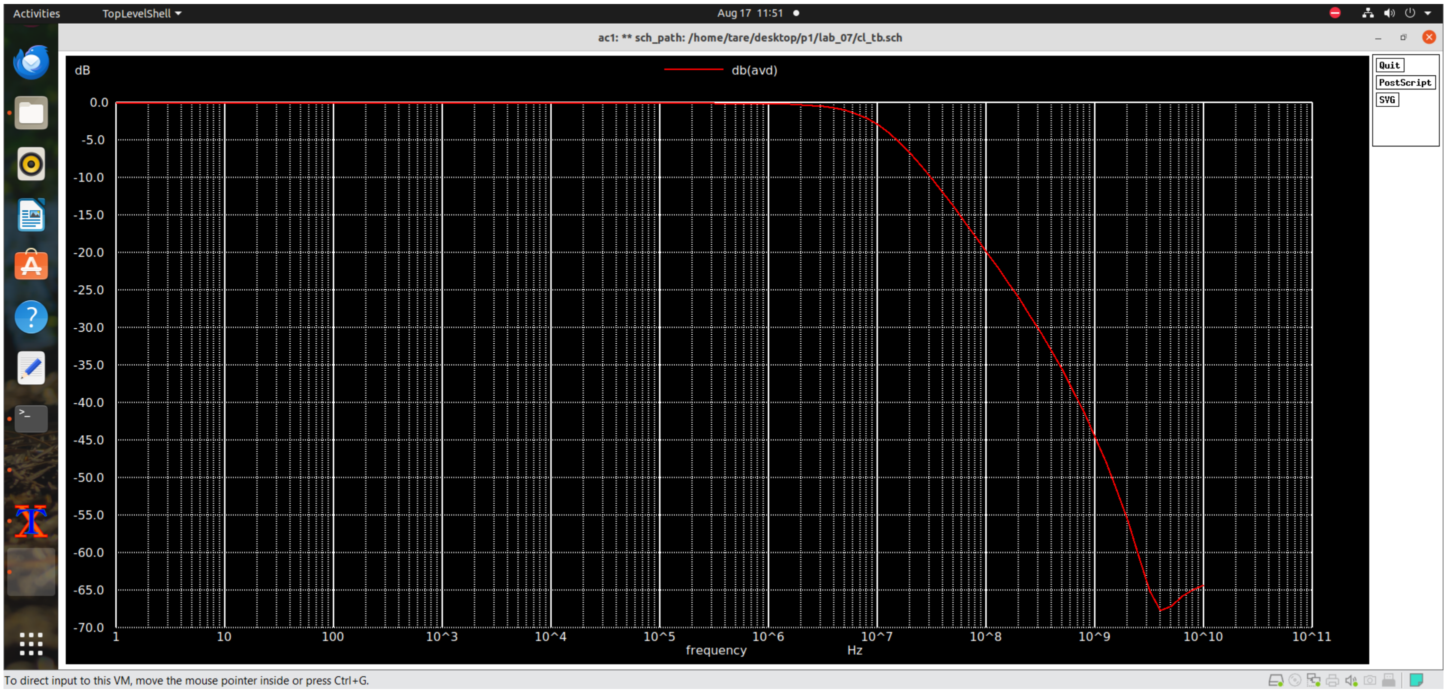
LG_TB.spice" -a || sh

```
      device          m.x1.xm6.m0          m.x1.xm5.m0          m.x1.xm4.m0
       model          nmos_3p3.9           nmos_3p3.13          pmos_3p3.12
          gm          0.000119943          0.000465766          0.000201631
        gmbs          4.31957e-05          0.000167373          7.83268e-05
         gds          7.94782e-07          4.53773e-06          2.39394e-06
         vds              0.80185             0.418614             0.916987
       vdsat             0.141366             0.139359             0.174148
         vgs             0.801854             0.801854             0.916989
         vth              0.70816             0.711823               0.7682
          id                1e-05          3.85683e-05          1.97552e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
      device          m.x1.xm3.m0          m.x1.xm2.m0          m.x1.xm1.m0
       model          pmos_3p3.12          nmos_3p3.12          nmos_3p3.12
          gm          0.000193492          0.000330798          0.000343476
        gmbs          7.53668e-05          8.99482e-05          9.34253e-05
         gds          2.91135e-06          2.72452e-06          3.39269e-06
         vds              0.55599             0.825383             0.464386
       vdsat             0.172733             0.086853            0.0891797
         vgs             0.916989             0.825384             0.831378
         vth             0.770039             0.830396              0.83136
          id          1.88131e-05          1.88131e-05          1.97552e-05

ngspice 1 ->
```

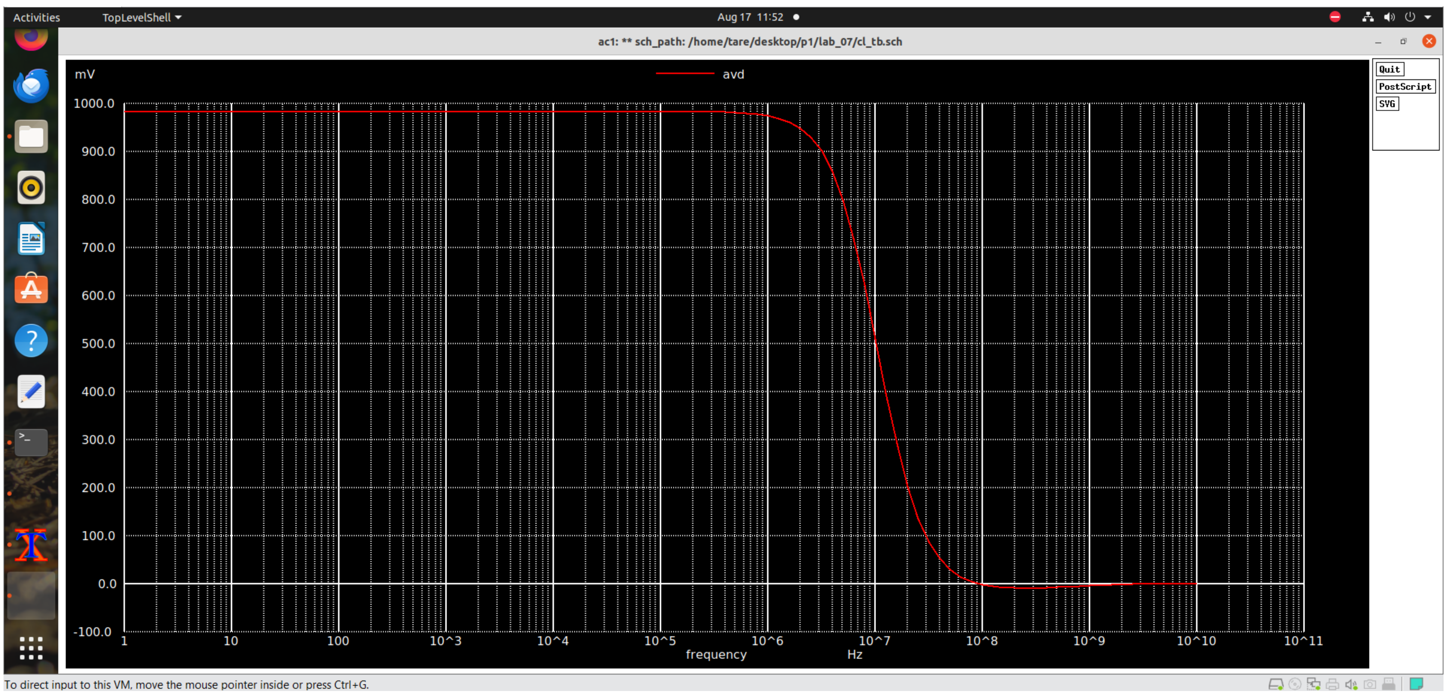
- **Compare simulation results (DC gain and GBW) with hand calculations in a table.**

✓ DC gain=$\frac{Acl}{1+LG}$=$\frac{59.566}{1+59.566}$=.9834v/v.

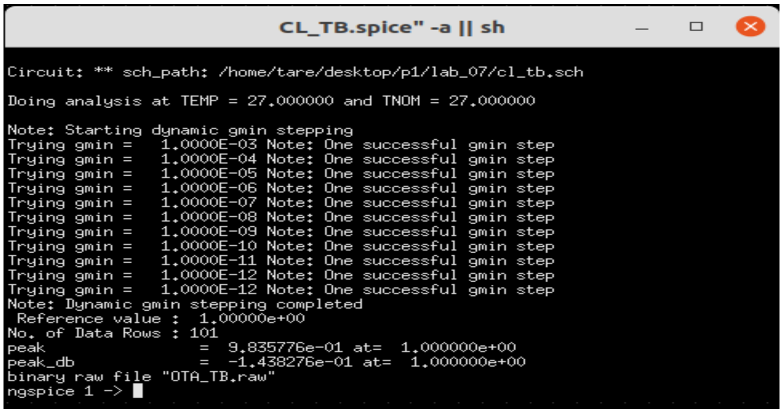
✓ GBW=$\frac{gm1{,}2}{2\pi CL}$=10.73MHz.



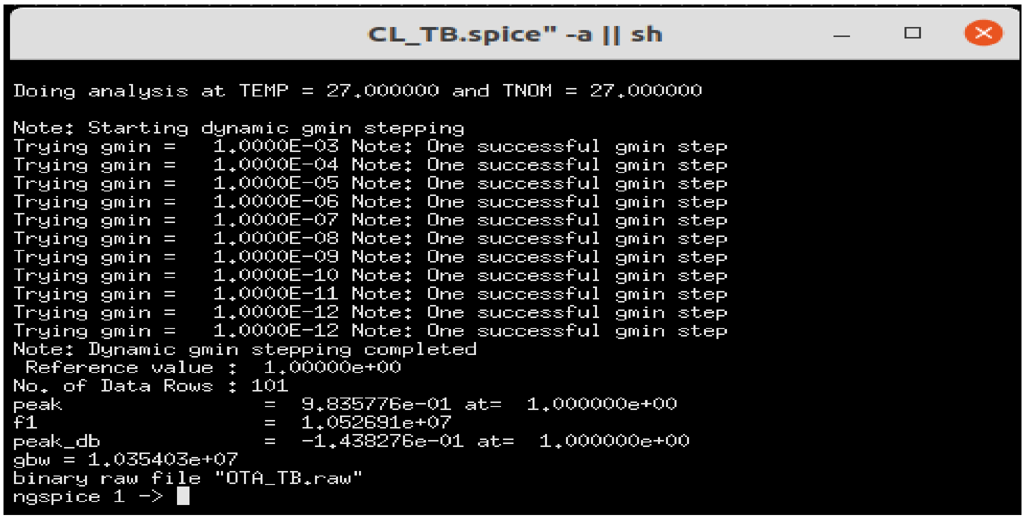
Activities
TopLevelShell
Aug 17 11:51
ac1: ** sch_path: /home/tare/desktop/p1/lab_07/cl_tb.sch
Quit
PostScript
SVG
dB
db(avd)
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
-35.0
-40.0
-45.0
-50.0
-55.0
-60.0
-65.0
-70.0
1
10
100
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^10
10^11
frequency
Hz
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.



Activities
TopLevelShell
Aug 17 11:52
ac1: ** sch_path: /home/tare/desktop/p1/lab_07/cl_tb.sch
Quit
PostScript
SVG
mV
avd
1000.0
900.0
800.0
700.0
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
1
10
100
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^10
10^11
frequency
Hz
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.



```
CL_TB.spice" -a || sh

Circuit: ** sch_path: /home/tare/desktop/p1/lab_07/cl_tb.sch

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Note: Starting dynamic gmin stepping
Trying gmin =   1.0000E-03 Note: One successful gmin step
Trying gmin =   1.0000E-04 Note: One successful gmin step
Trying gmin =   1.0000E-05 Note: One successful gmin step
Trying gmin =   1.0000E-06 Note: One successful gmin step
Trying gmin =   1.0000E-07 Note: One successful gmin step
Trying gmin =   1.0000E-08 Note: One successful gmin step
Trying gmin =   1.0000E-09 Note: One successful gmin step
Trying gmin =   1.0000E-10 Note: One successful gmin step
Trying gmin =   1.0000E-11 Note: One successful gmin step
Trying gmin =   1.0000E-12 Note: One successful gmin step
Trying gmin =   1.0000E-12 Note: One successful gmin step
Note: Dynamic gmin stepping completed
 Reference value :  1.00000e+00
No. of Data Rows : 101
peak                =  9.835776e-01 at=  1.000000e+00
peak_db             =  -1.438276e-01 at=  1.000000e+00
binary raw file "OTA_TB.raw"
ngspice 1 ->
```



```
CL_TB.spice" -a || sh

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Note: Starting dynamic gmin stepping
Trying gmin =   1.0000E-03 Note: One successful gmin step
Trying gmin =   1.0000E-04 Note: One successful gmin step
Trying gmin =   1.0000E-05 Note: One successful gmin step
Trying gmin =   1.0000E-06 Note: One successful gmin step
Trying gmin =   1.0000E-07 Note: One successful gmin step
Trying gmin =   1.0000E-08 Note: One successful gmin step
Trying gmin =   1.0000E-09 Note: One successful gmin step
Trying gmin =   1.0000E-10 Note: One successful gmin step
Trying gmin =   1.0000E-11 Note: One successful gmin step
Trying gmin =   1.0000E-12 Note: One successful gmin step
Trying gmin =   1.0000E-12 Note: One successful gmin step
Note: Dynamic gmin stepping completed
 Reference value :  1.00000e+00
No. of Data Rows : 101
peak                =  9.835776e-01 at=  1.000000e+00
f1                  =  1.052691e+07
peak_db             =  -1.438276e-01 at=  1.000000e+00
gbw = 1.035403e+07
binary raw file "OTA_TB.raw"
ngspice 1 ->
```

	Hand Analysis	Simulation
DC gain	.9834v/v	.984v/v
GBW	10.73MHz	10.35MHz