وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design – Cadence and Master Micro Tools
Lab 06
Differential Amplifier

Part 1: Differential Amplifier Design

1) We want to design a resistive loaded differential amplifier with the specifications below.
NOTE: that the bias current is split between two transistors; each transistor gets $ID = 20\mu A$.

Parameter	
Supply (V_{DD})	$1.8V$
Bias current (I_{SS})	$40\mu A$
Differential gain	8
CM output level[1]	$V_{DD}/3$
Load capacitance	$1pF$

2) **Since the required output level is closer to the ground rail, we will use a PMOS input stage. Assume the PMOS will not be placed in a dedicated well to save the area -Body cannot be connected to floating source-. Assume we will use a simple current mirror for biasing. The design schematic is shown below.**

3) **Choose R_D to meet the CM output level spec.**
   - ✓ RD=$\frac{2*VoCM}{ISS}$=$\frac{2*.6}{40uA}$=30KΩ.

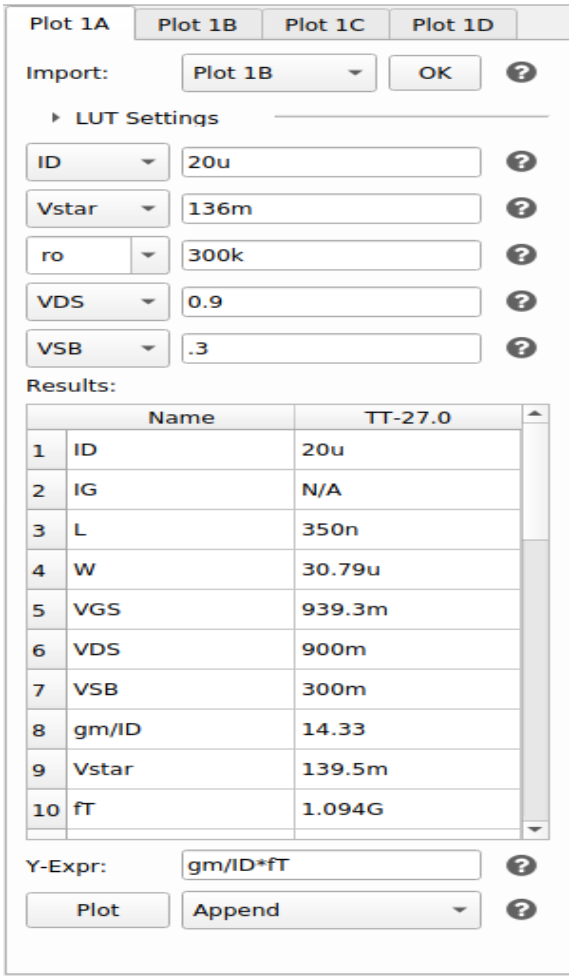
4) **The differential amplifier gain is given by $|Av| \approx g_m(R_D||r_o)$**

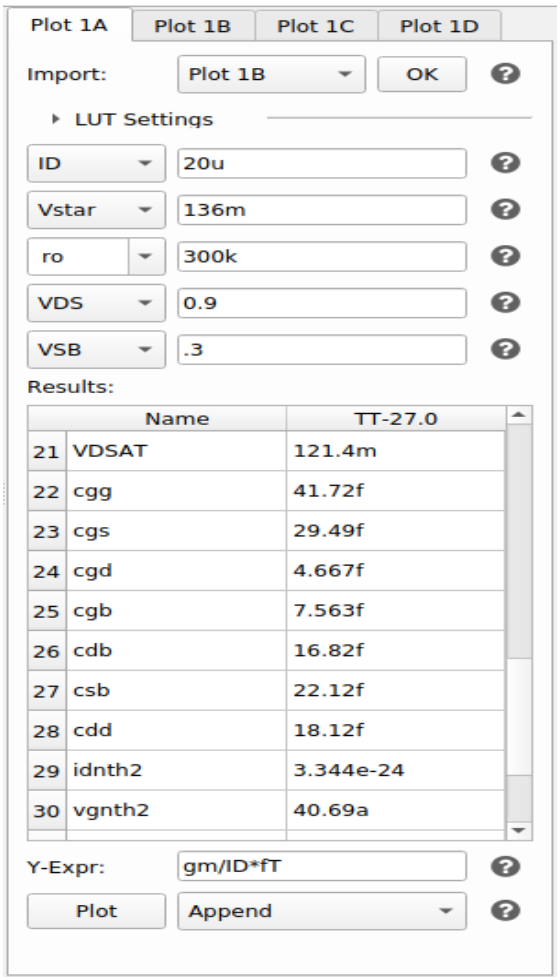
5) **We will choose L to set $ro \gg RD$, ro = 10 × RD=300KΩ.**

$$|A_v| \approx 0.91 \times g_m R_D = 0.91 \times \frac{2I_D}{V^*} \times R_D = \frac{1.82V_{R_D}}{V^*}$$

Av=$\frac{2*ID*RD}{V*}$*.91=$\frac{1.82VRD}{V*}$=8 , **V*=136.5mV.**

6) Assume we will set VDS of the tail current source to $300mV$ to allow more output swing. **Report the input pair sizing using SA.**



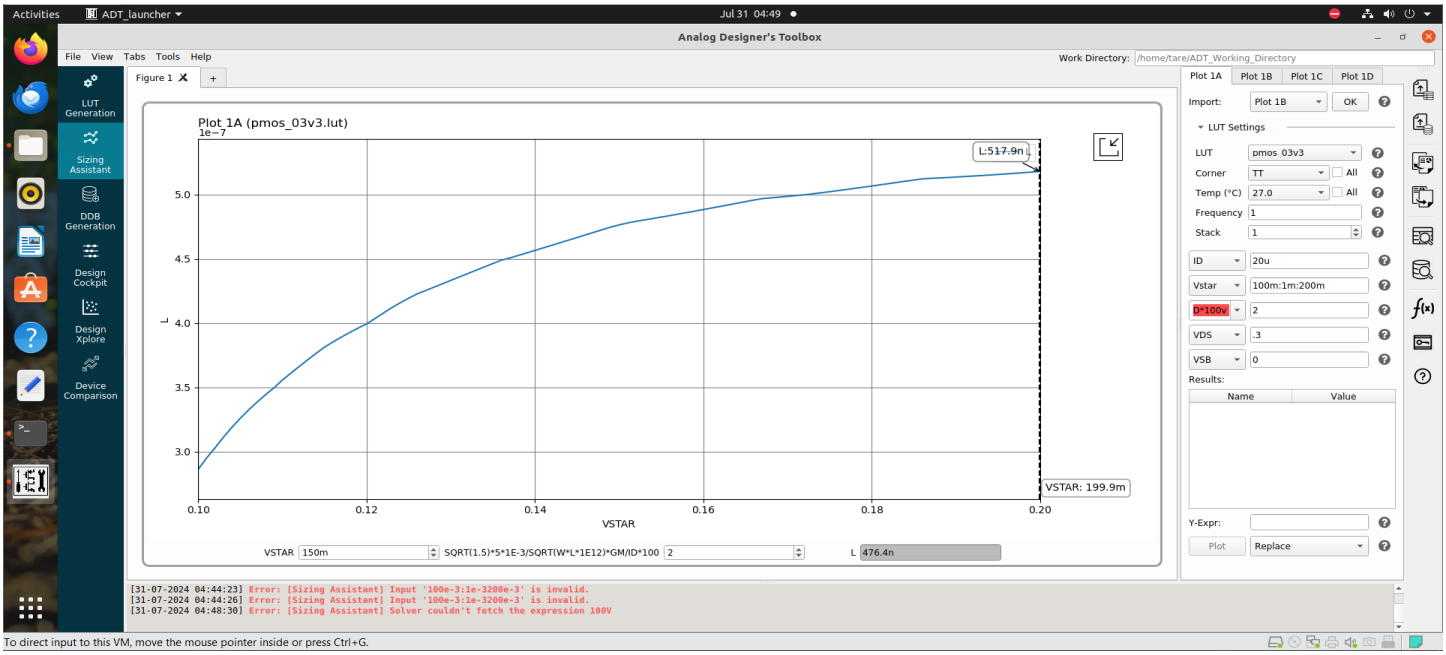


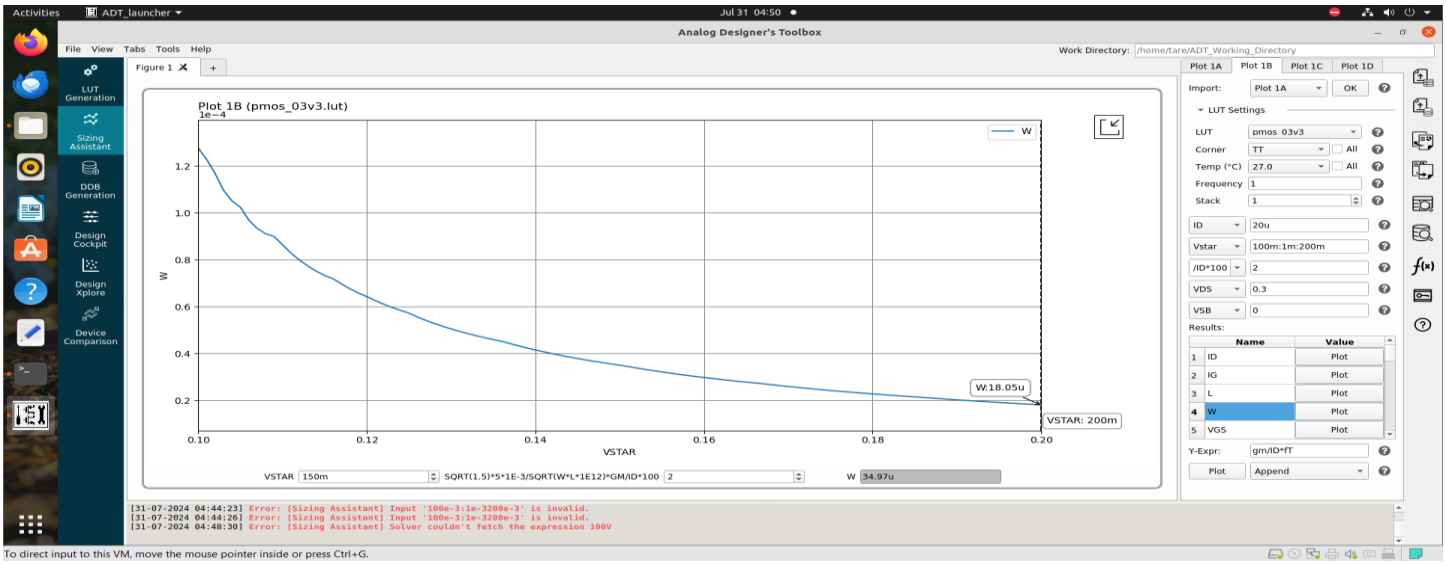
7) Given the above assumption for V_{DS} of the tail current source, calculate the required CM input level.

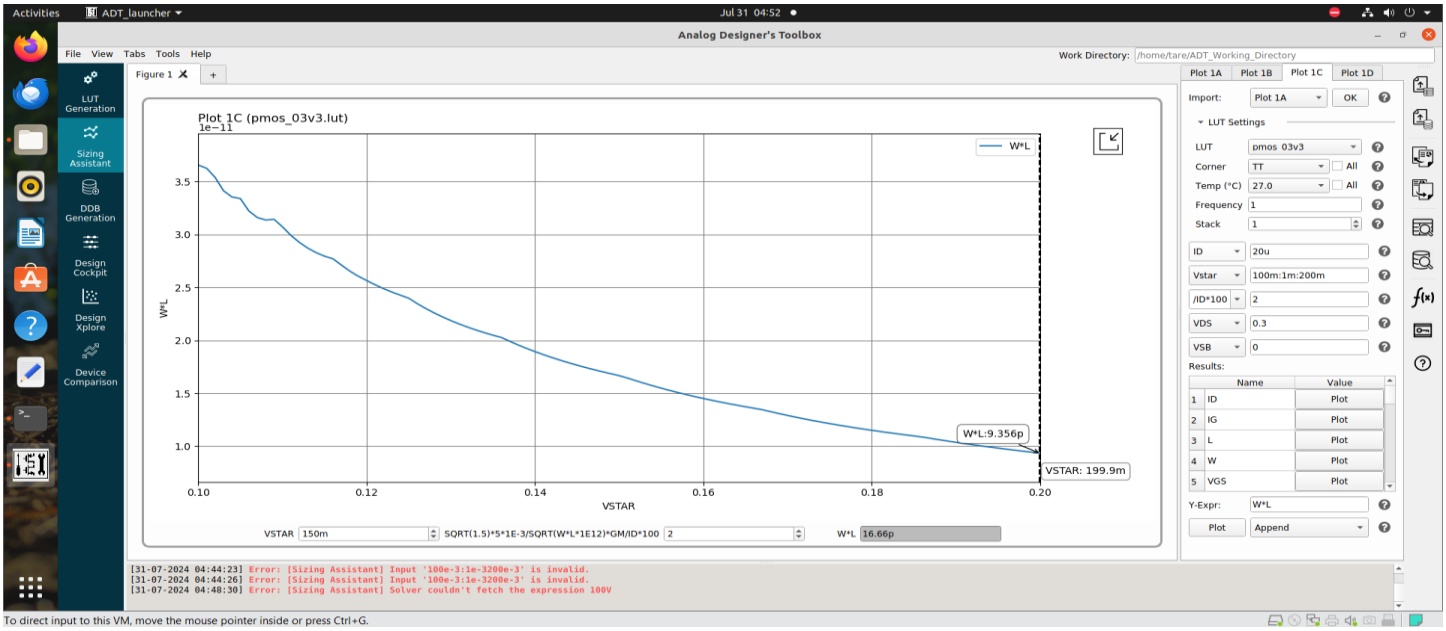
- ✓ **V_{iCM}=VDD-|VDS1|-|VGS3|=1.8-.3-.9393=.5607V.**

8) The tail current source has the following specifications:

Parameter	
Input current	$20\mu A$
Percent mismatch: $\sigma(I_{out})/I_{out}$	$\leq 2\%$
Compliance voltage	$\leq 200mV$
Area	Minimize


Activities
ADT_launcher
Jul 31 04:49
Analog Designer's Toolbox
File View Tabs Tools Help
Work Directory: /home/tare/ADT_Working_Directory
LUT Generation
Sizing Assistant
DDB Generation
Design Cockpit
Design Xplore
Device Comparison
Figure 1
Plot 1A (pmos_03v3.lut)
1e−7
L:517.9n
VSTAR: 199.9m
L
VSTAR
VSTAR 150m
SQRT(1.5)*5*1E-3/SQRT(W*L*1E12)*GM/ID*100 2
L 476.4n
Plot 1A Plot 1B Plot 1C Plot 1D
Import: Plot 1B OK
LUT Settings
LUT pmos_03v3
Corner TT All
Temp (°C) 27.0 All
Frequency 1
Stack 1
ID 20u
Vstar 100m:1m:200m
D*100V 2
VDS .3
VSB 0
Results:
Name Value
Y-Expr:
Plot Replace
[31-07-2024 04:44:23] Error: [Sizing Assistant] Input '100e-3:1e-3200e-3' is invalid.
[31-07-2024 04:44:26] Error: [Sizing Assistant] Input '100e-3:1e-3200e-3' is invalid.
[31-07-2024 04:48:30] Error: [Sizing Assistant] Solver couldn't fetch the expression 100V
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.


Activities
ADT_launcher
Jul 31 04:50
Analog Designer's Toolbox
File View Tabs Tools Help
Work Directory: /home/tare/ADT_Working_Directory
LUT Generation
Sizing Assistant
DDB Generation
Design Cockpit
Design Xplore
Device Comparison
Figure 1
Plot 1B (pmos_03v3.lut)
1e−4
W
W:18.05u
VSTAR: 200m
W
VSTAR
VSTAR 150m
SQRT(1.5)*5*1E-3/SQRT(W*L*1E12)*GM/ID*100 2
W 34.97u
Plot 1A Plot 1B Plot 1C Plot 1D
Import: Plot 1A OK
LUT Settings
LUT pmos_03v3
Corner TT All
Temp (°C) 27.0 All
Frequency 1
Stack 1
ID 20u
Vstar 100m:1m:200m
/ID*100 2
VDS 0.3
VSB 0
Results:
Name Value
1 ID Plot
2 IG Plot
3 L Plot
4 W Plot
5 VGS Plot
Y-Expr: gm/ID*fT
Plot Append
[31-07-2024 04:44:23] Error: [Sizing Assistant] Input '100e-3:1e-3200e-3' is invalid.
[31-07-2024 04:44:26] Error: [Sizing Assistant] Input '100e-3:1e-3200e-3' is invalid.
[31-07-2024 04:48:30] Error: [Sizing Assistant] Solver couldn't fetch the expression 100V
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

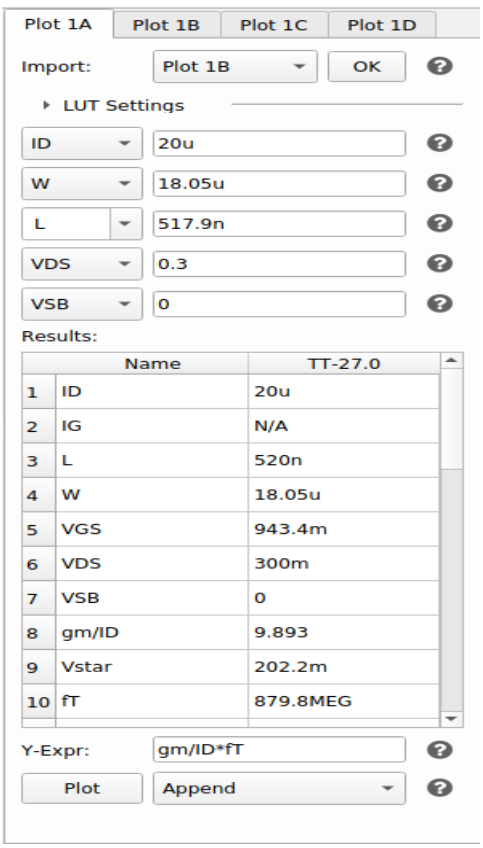

Activities
ADT_launcher
Jul 31 04:52
Analog Designer's Toolbox
File View Tabs Tools Help
Work Directory: /home/tare/ADT_Working_Directory
LUT Generation
Sizing Assistant
DDB Generation
Design Cockpit
Design Xplore
Device Comparison
Figure 1
Plot 1C (pmos_03v3.lut)
1e−11
W*L
W*L:9.356p
VSTAR: 199.9m
W*L
VSTAR
VSTAR 150m
SQRT(1.5)*5*1E-3/SQRT(W*L*1E12)*GM/ID*100 2
W*L 16.66p
Plot 1A Plot 1B Plot 1C Plot 1D
Import: Plot 1A OK
LUT Settings
LUT pmos_03v3
Corner TT All
Temp (°C) 27.0 All
Frequency 1
Stack 1
ID 20u
Vstar 100m:1m:200m
/ID*100 2
VDS 0.3
VSB 0
Results:
Name Value
1 ID Plot
2 IG Plot
3 L Plot
4 W Plot
5 VGS Plot
Y-Expr: W*L
Plot Append
[31-07-2024 04:44:23] Error: [Sizing Assistant] Input '100e-3:1e-3200e-3' is invalid.
[31-07-2024 04:44:26] Error: [Sizing Assistant] Input '100e-3:1e-3200e-3' is invalid.
[31-07-2024 04:48:30] Error: [Sizing Assistant] Solver couldn't fetch the expression 100V
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

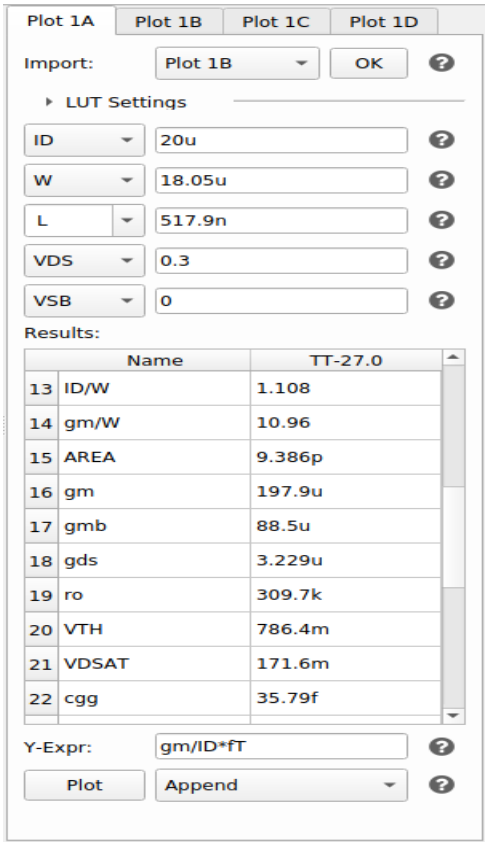
9) As seen in the plot above, for a given mismatch requirement, the minimum area is achieved at the max V_*. Similarly, for a given area requirement, the minimum mismatch is achieved at the max V_*. That's why current mirrors are commonly biased in strong inversion.

10) The plot also shows that at a given V_* (compliance voltage), going for lower mismatch necessitates longer L, which also gives lower λ (higher r_o, although the effect of L on λ is limited at low V_{DS}). However, this comes at the expense of area.

11) Given the compliance voltage spec, **report** the above figure with a cursor added to the selected design point.

12) **Calculate** the min and max CM input levels.





V_{iCMmax}= VDD-V*1-|VGS4|=1.8-.2022-.9393=.6587V

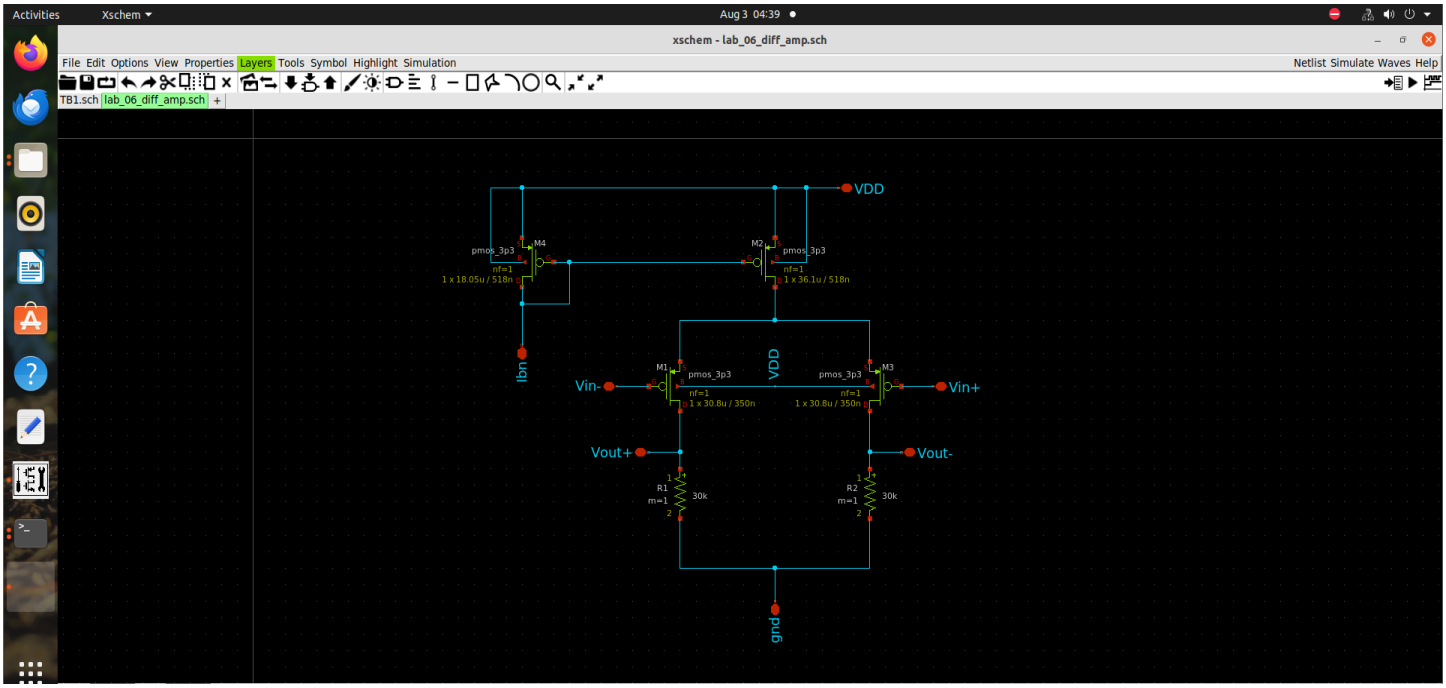
V_{iCMmin}= VRD+|VGS4|-V*=.6-.9393+.1395=-.1998V

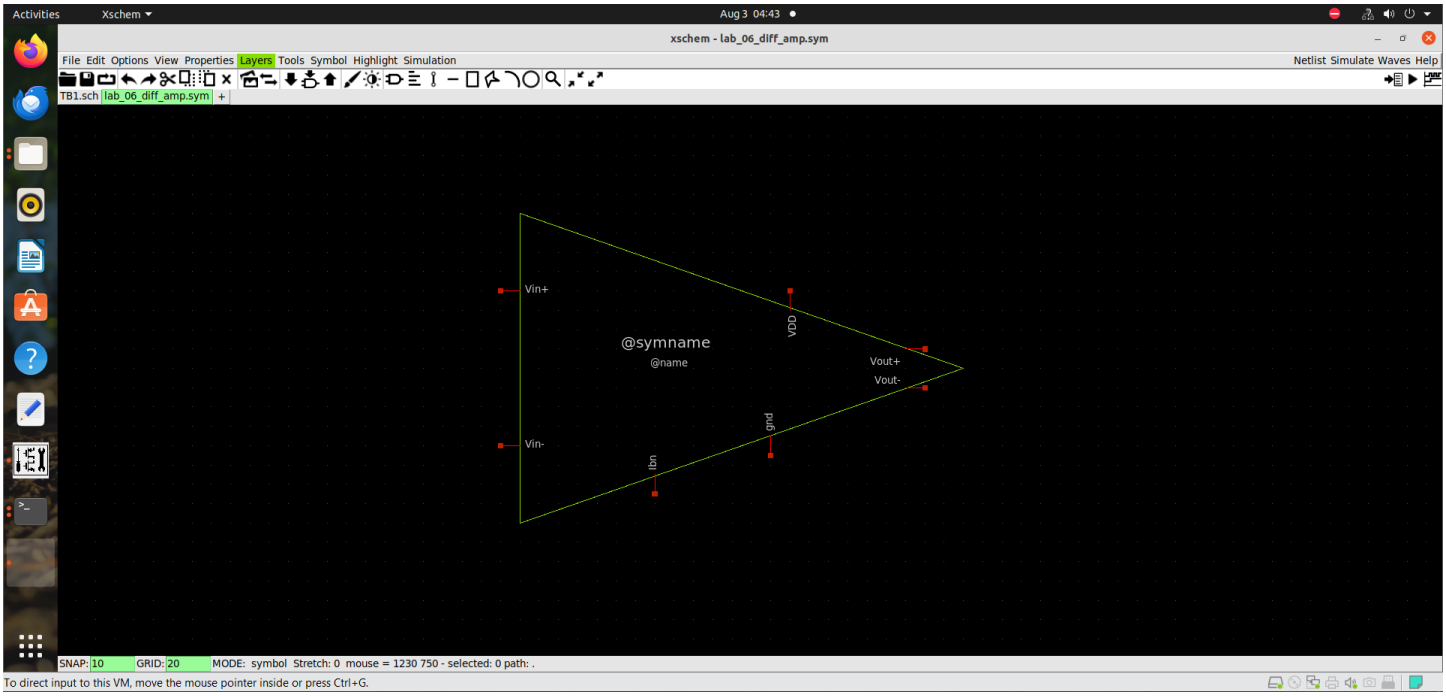
Is the previously selected CM input level in the valid range?

As V_{iCM}=.5607V , so that it is in the valid range.

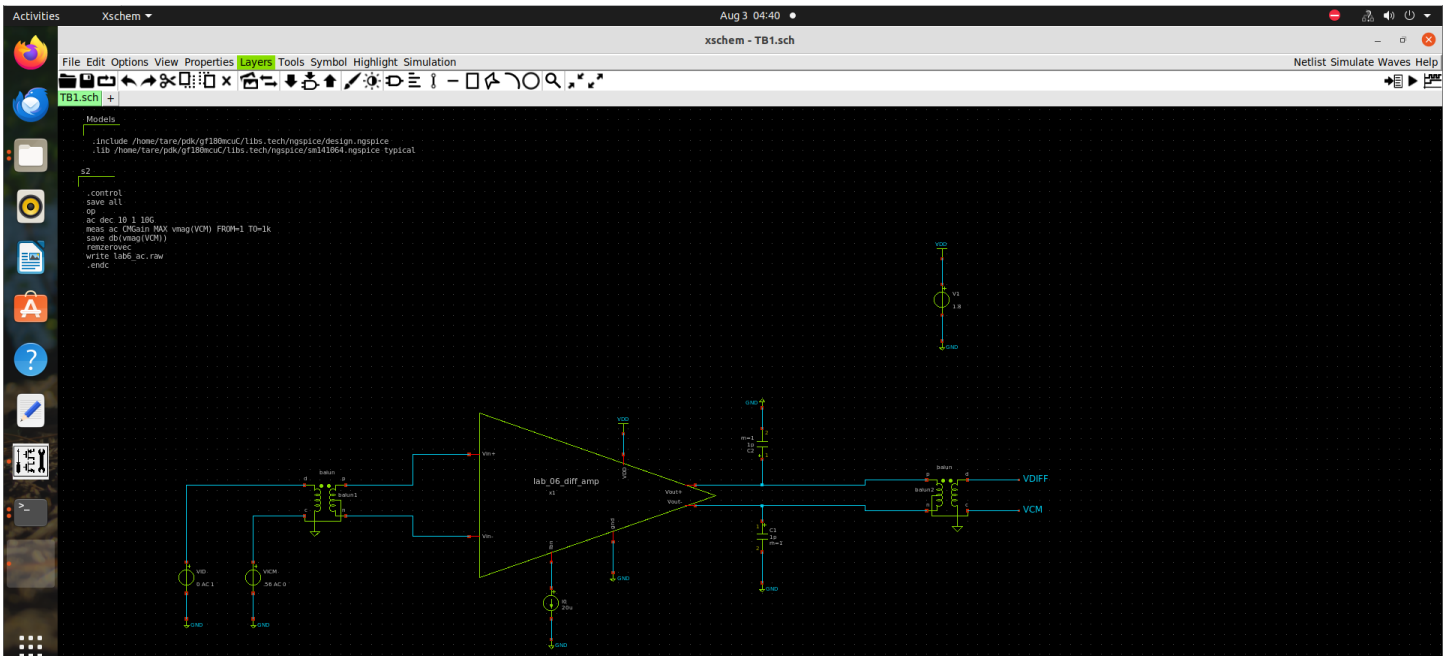
Part 2: Differential Amplifier Simulation

1) **Create the schematic of a differential amplifier “lab_06_diff_amp”.**
2) **Create a symbol for the diff pair. Edit the symbol to look as shown below in the testbench schematic.**





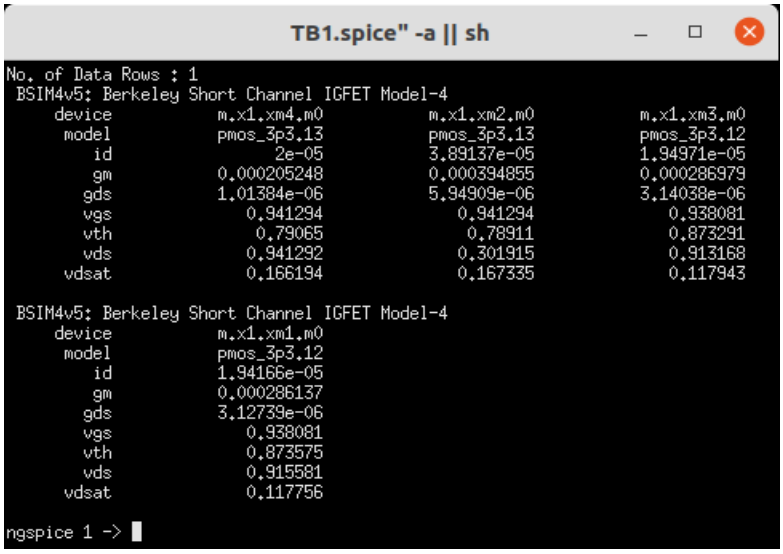
3) Create a new cell for the testbench "lab_06_diff_amp_tb". Create the testbench schematic as shown below.



4) Set the transistor sizing and Vicm as designed in Part 1. Unless otherwise stated, set Vid = 0 (this is the large signal differential input voltage).

1. OP simulation:

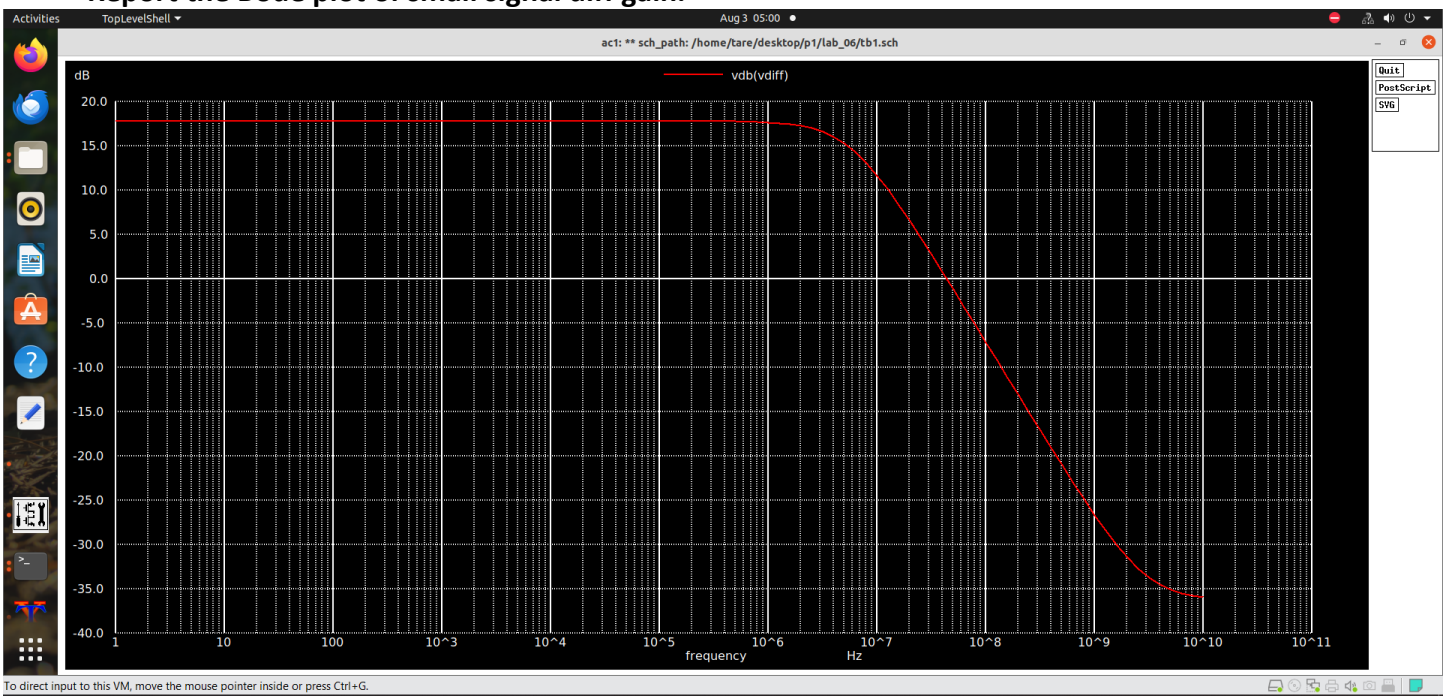
- **Report a snapshot clearly showing the following parameters.**

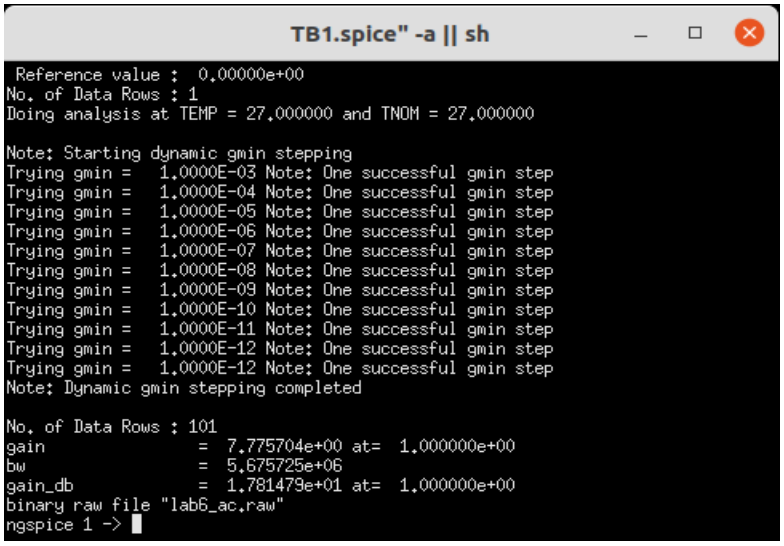


- **Check that all transistors operate in saturation.**
  - ✓ **As VDS>VDSat for all transistors then all transistors in saturation.**

2. Diff small signal ccs:

- **Use AC magnitude = 1 for the diff source (and AC magnitude = 0 for the CM source).**
- **Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).**
- **Report the Bode plot of small signal diff gain.**





- **Compare the DC diff gain and BW with hand analysis in a table.**

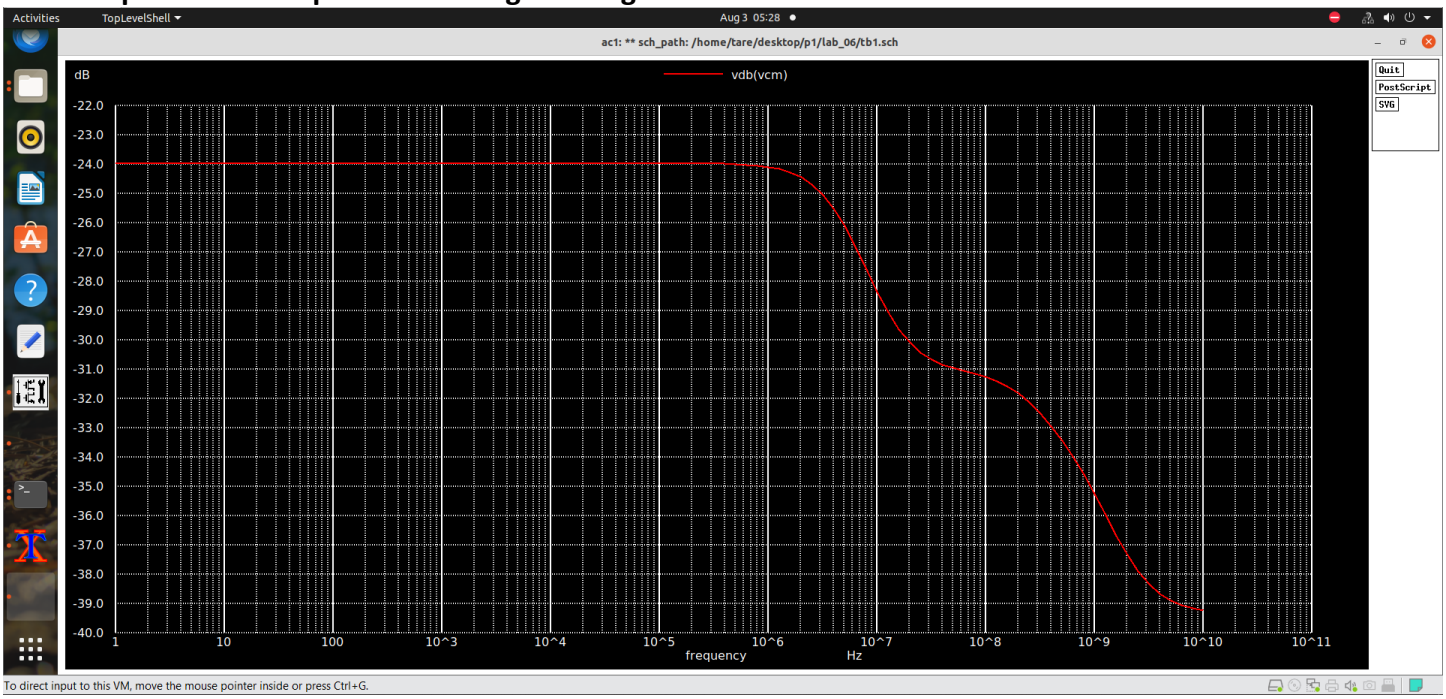
Av=.91*gm*RD=7.32V/V =17.3db

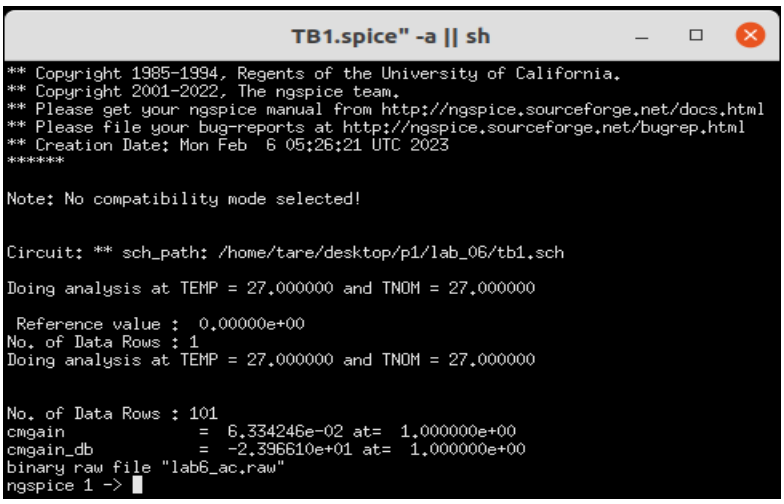
BW= $\frac{1}{2\pi * .91 * RD * (CL + Cgd + Cdb)}$ **=5.707MHZ**

	Hand Analysis	Simulation
Gain	**7.32v/v=17.3db**	**7.78v/v=17.81db**
BW	**5.707MHz**	**5.676MHz**

3. CM small signal ccs:

- **Use AC magnitude = 1 for the CM source (and AC magnitude = 0 for the diff source).**
- **Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).**
- **Report the Bode plot of small signal CM gain.**





- **Compare the DC CM gain with hand analysis in a table.**

Avcm=$\frac{gm*RD}{1+2gm*ro2}$=88.33mV/V=-21db.

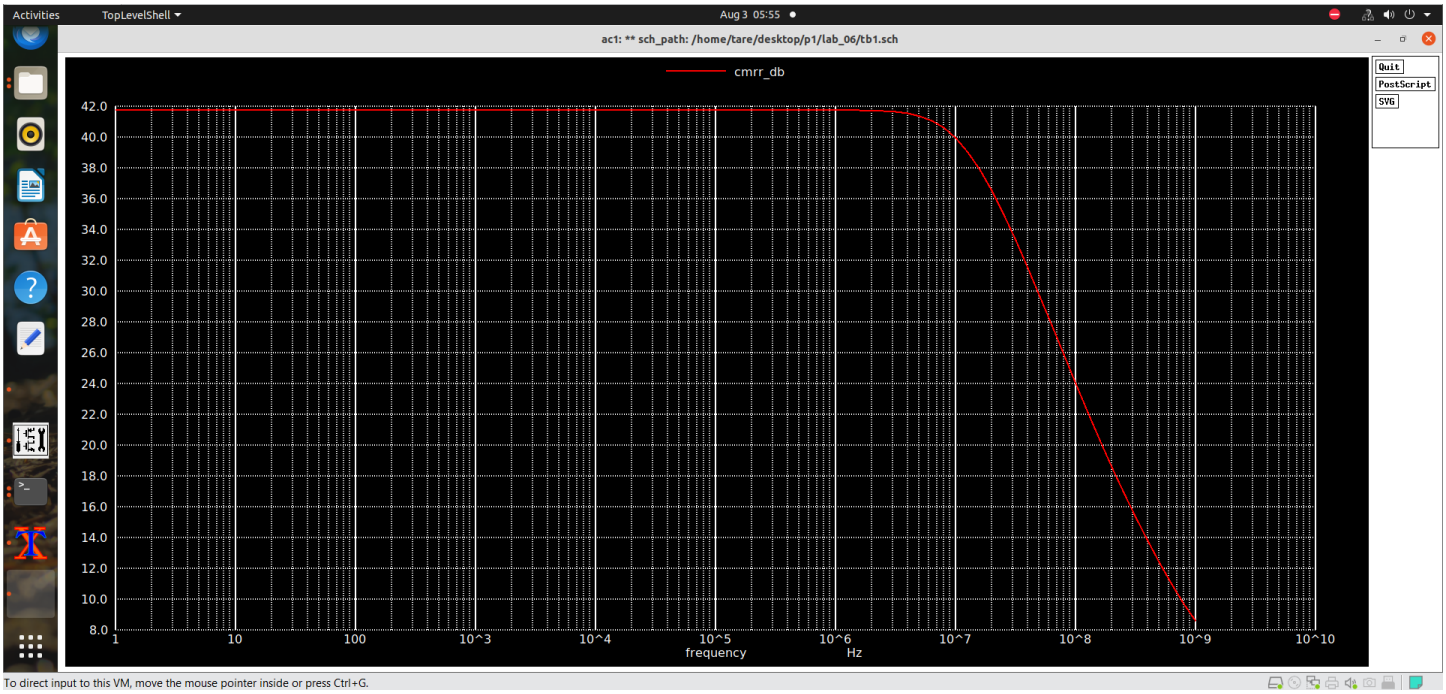
	Hand Analysis	Simulation
CMgain	88.33mV/V=-21db	63.34mV/V=-23.97db

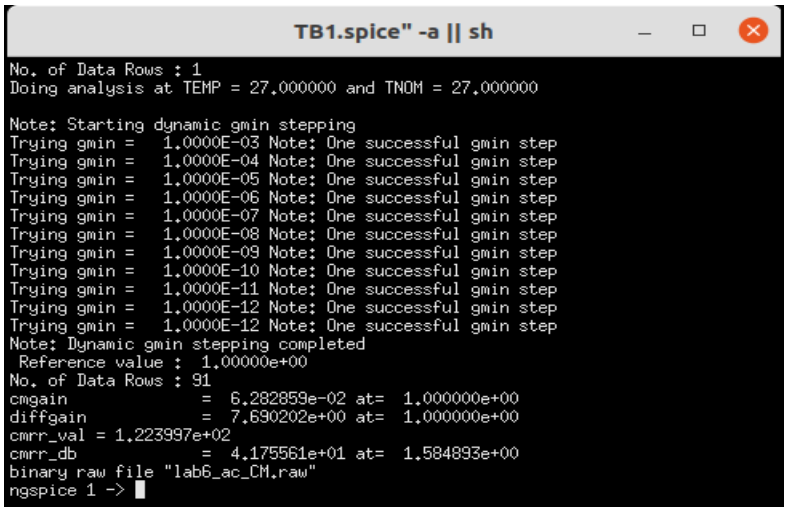
- **Is it smaller than "1"? Why?**
  - ✓ **Yes it is smaller than 1 , as the half circuit in CM ac analysis is Common Source degenerated by large resistance 2*ro2 , so that it attenuate the CM signal.**

- **Justify the variation of Avcm vs frequency.**

✓ **As we see the CM gain start drop at the frequency of the output pole but as frequency increases more the capacitances at the coupling node shunting ro2 so that the degeneration decreases so that the CM gain saturate and continue to drop .**

- **Plot Avd/Avcm in dB. Compare Avd/Avcm @ DC with hand analysis in a table.**





✓ **CMRR≈1+2*gm*ro2=97.15v/v=39.75db.**

	Hand Analysis	Simulation
CMRR	97.15=39.75db	122.4=41.76db

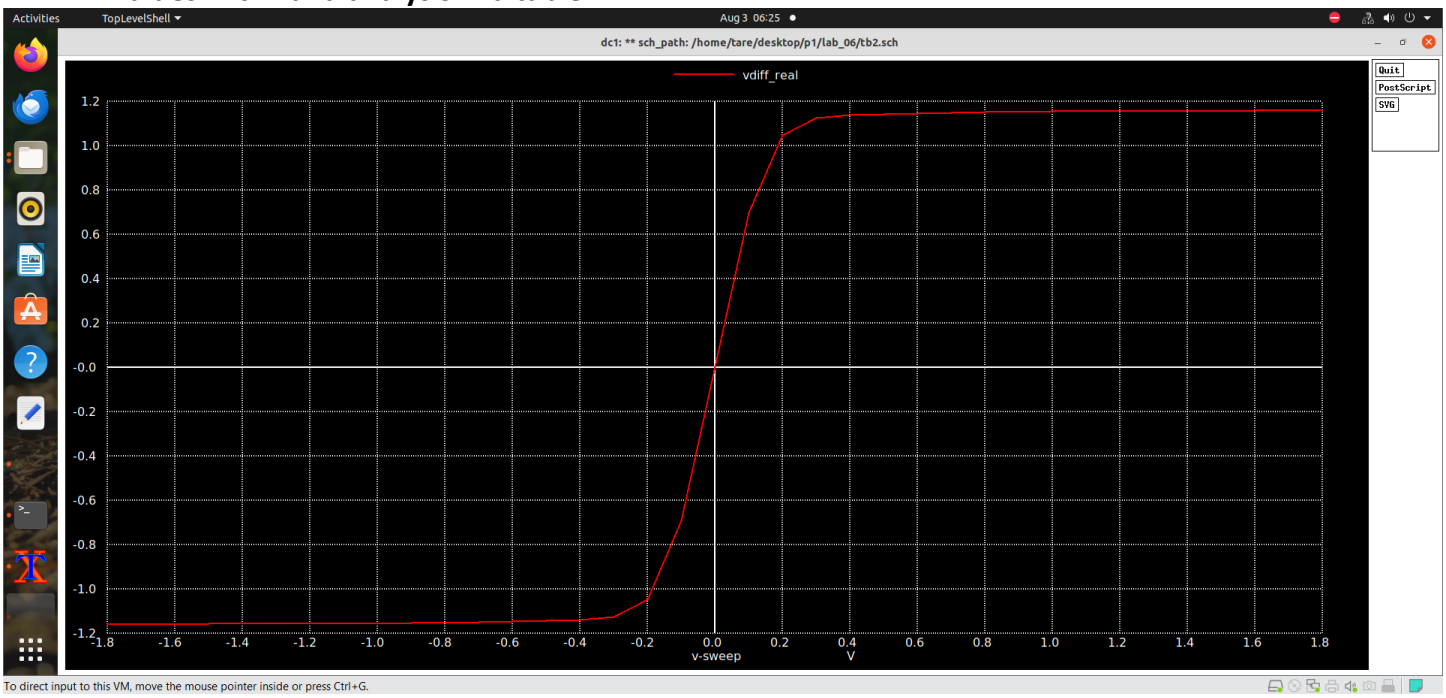
- **Justify the variation of Avd/Avcm with frequency.**

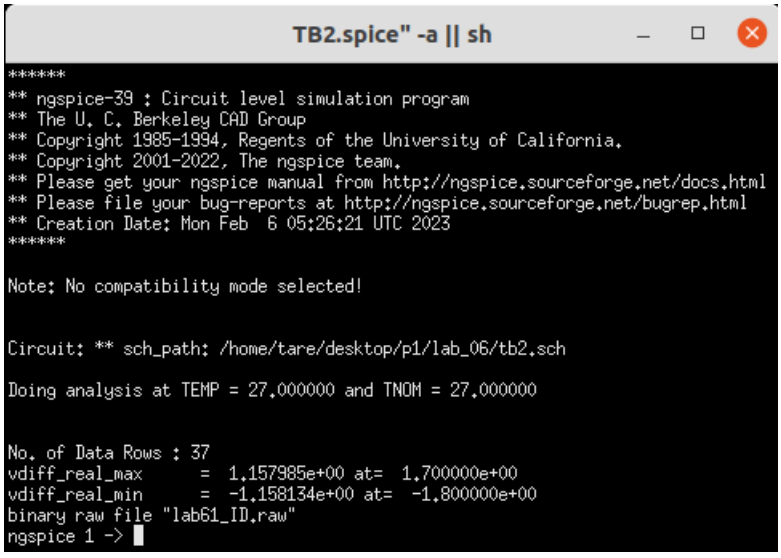
✓ **Due to the output pole the Differential gain and CM gain drop by 20db/decade so that CMRR is constant , as frequency increases above output pole frequency CMRR starts to drop due to the zero in the CM**

gain as the CP shunting RSS at high frequency so that the degeneration Resistance decreases and CM gain increases.

4. Diff large signal ccs:

- **Use dc sweep (not parametric sweep) for Vid = -VDD:10m:VDD.**
- **Report diff large signal ccs (VODIFF vs VIDIFF). Compare the extreme values with hand analysis in a table.**

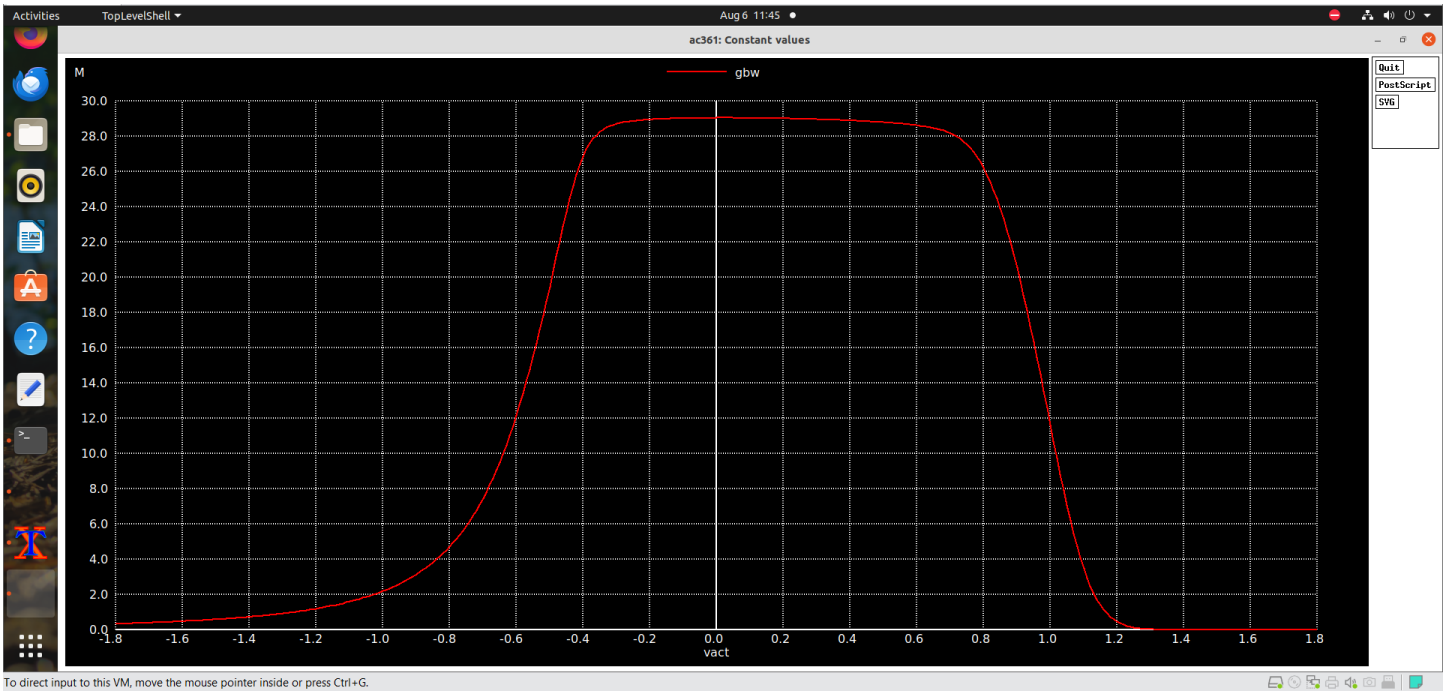




	Hand Analysis	Simulation
VODIFF_high	Iss*RD=1.2V	1.58
VODIFF_low	-Iss*RD=-1.2V	-1.58

5. CM large signal ccs (GBW vs Vicm):

- **We will use parametric sweep on AC analysis to get GBW.**
- **Report CM large signal ccs (GBW vs VICM). Assume the valid range for Vicm (CMIR) is defined by the condition that Avd is within 90% of the max gain, i.e., 10% drop in gain.**
- **Find the CM input range (CMIR). Compare with hand analysis in a table.**




```
TB2.spice" -a || sh
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 111
diffgain            =  3.416536e-08 at=  1.000000e+00
f3db                =  8.093062e+03
binary raw file "Lab6_param.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 111
diffgain            =  2.607076e-08 at=  1.000000e+00
f3db                =  7.040622e+03
binary raw file "Lab6_param.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

 Reference value :  1.00000e+00
No. of Data Rows : 111
diffgain            =  1.989301e-08 at=  1.000000e+00
f3db                =  6.180621e+03
binary raw file "Lab6_param.raw"
vicmmax = 7.700000e-01
vicmmin = -4.00000e-01
ngspice 1 ->
```

	Hand Analysis	Simulation
VICMMAX	.6587V	.77V
VICMMIN	-.1998V	-.4V