

وَمَا أُوتِينَتْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Ain Shams University – Faculty of Engineering – ECE Dept. – Integrated Circuits Lab.
Dr. Hesham Omran

Analog IC Design

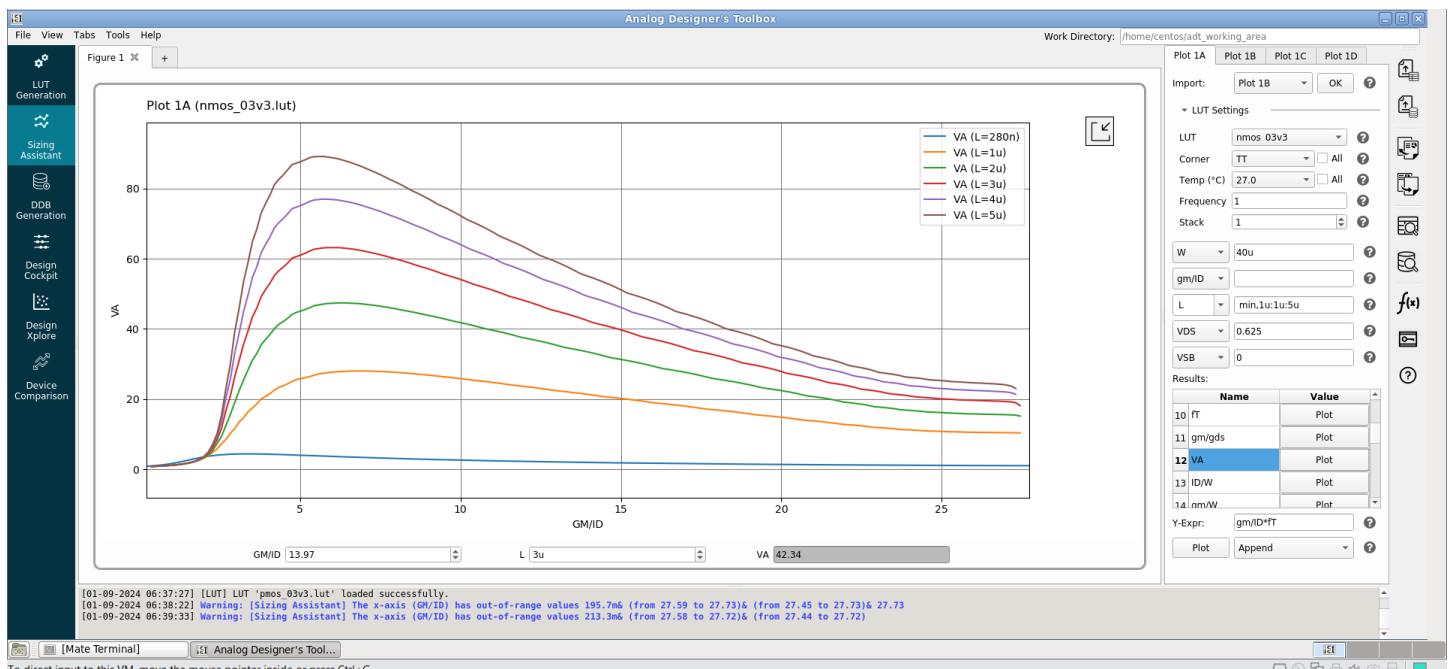
Lab 11 (Mini Project 02)

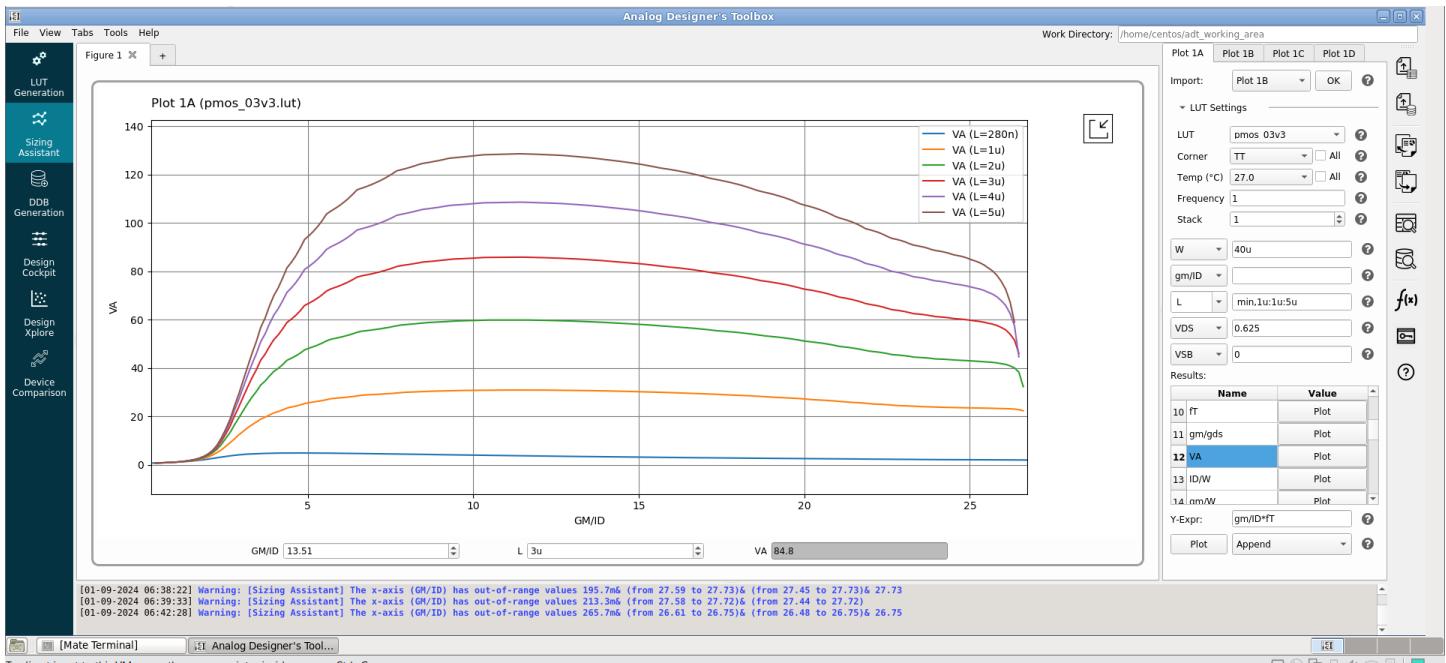
Fully-Differential Folded Cascode OTA

PART 1: gm/ID Design Charts

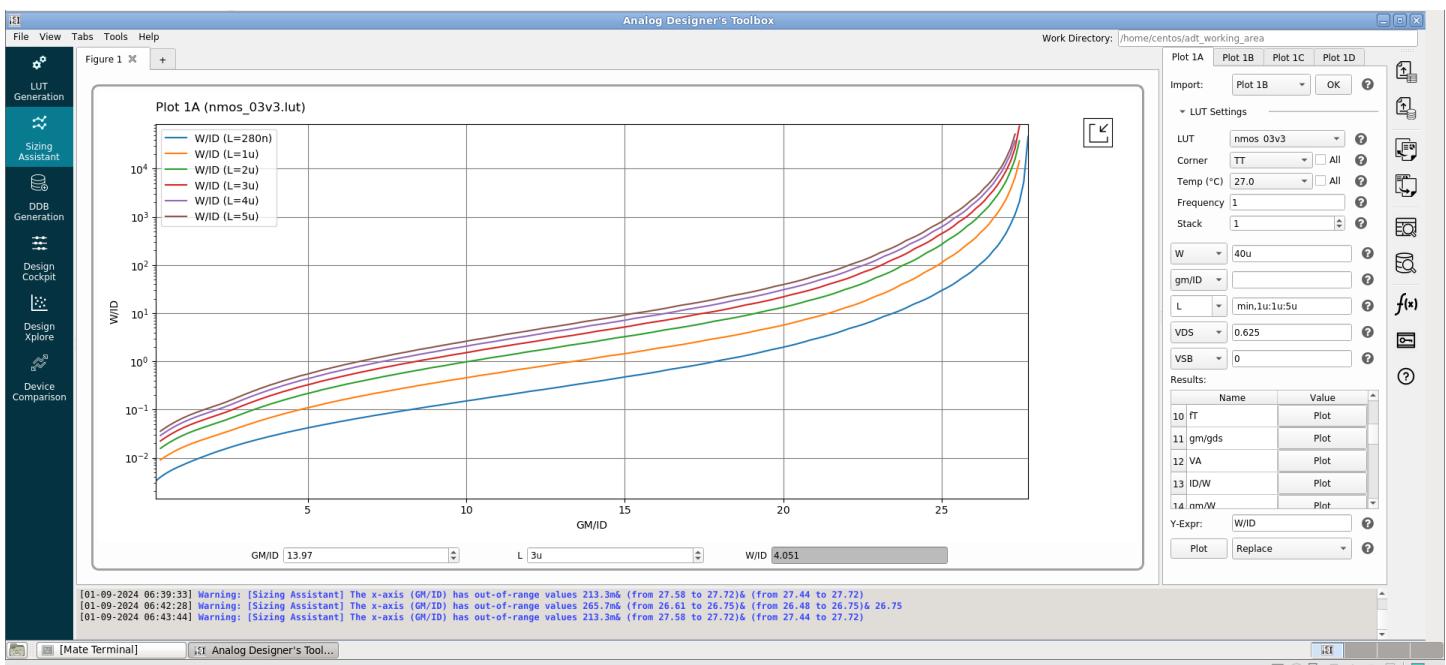
Using ADT Sizing Assistant, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS to a reasonable value and L = min,1u:1u:5u.

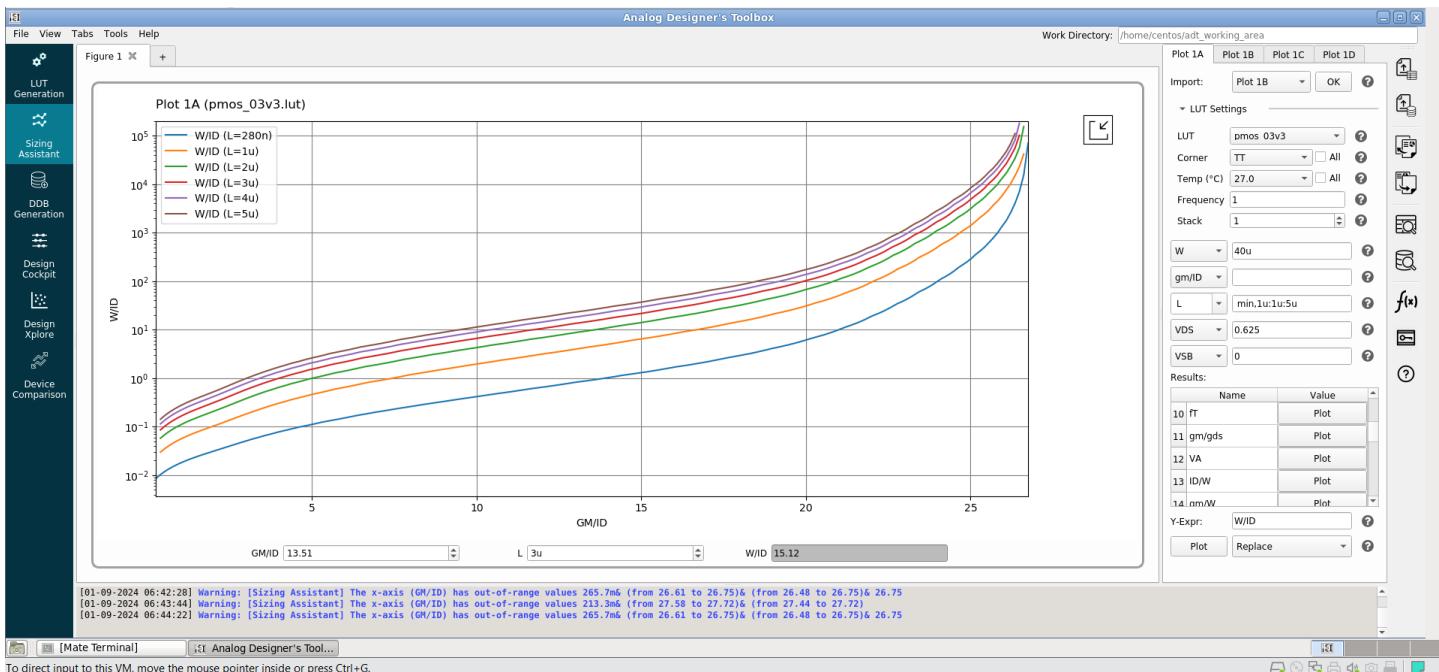
1. VA



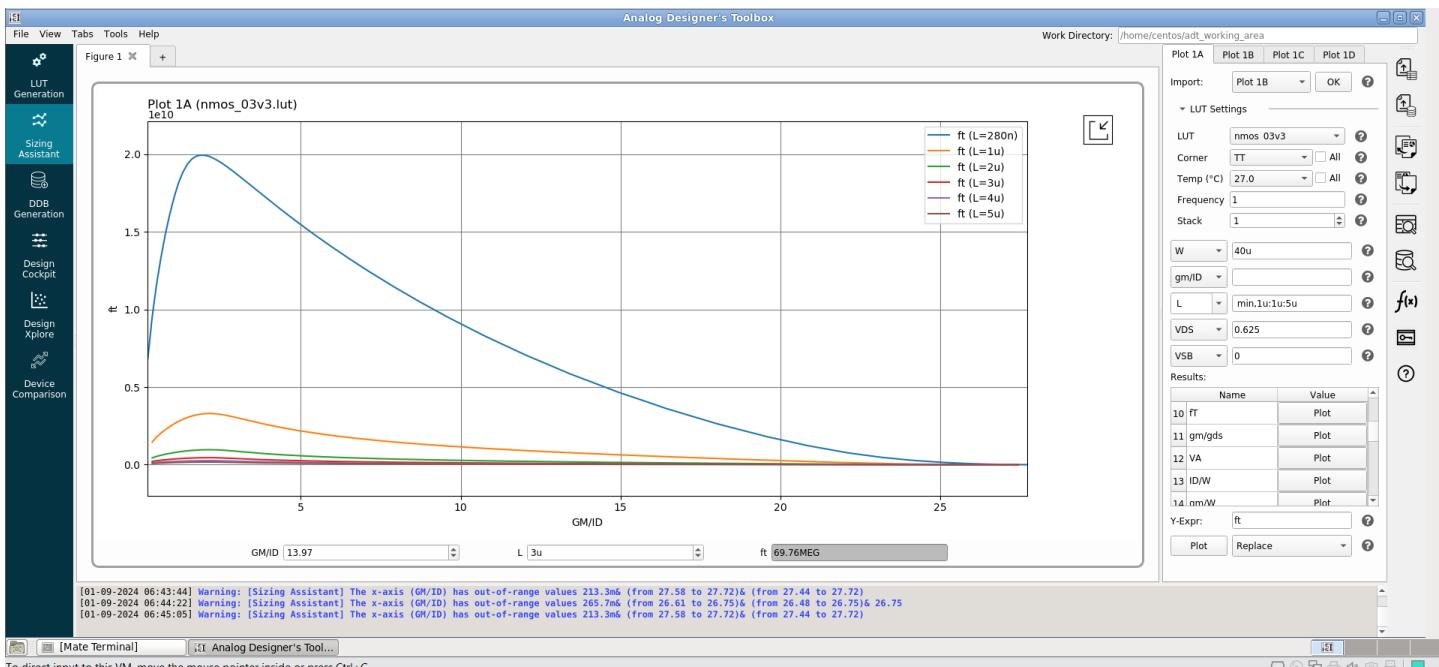


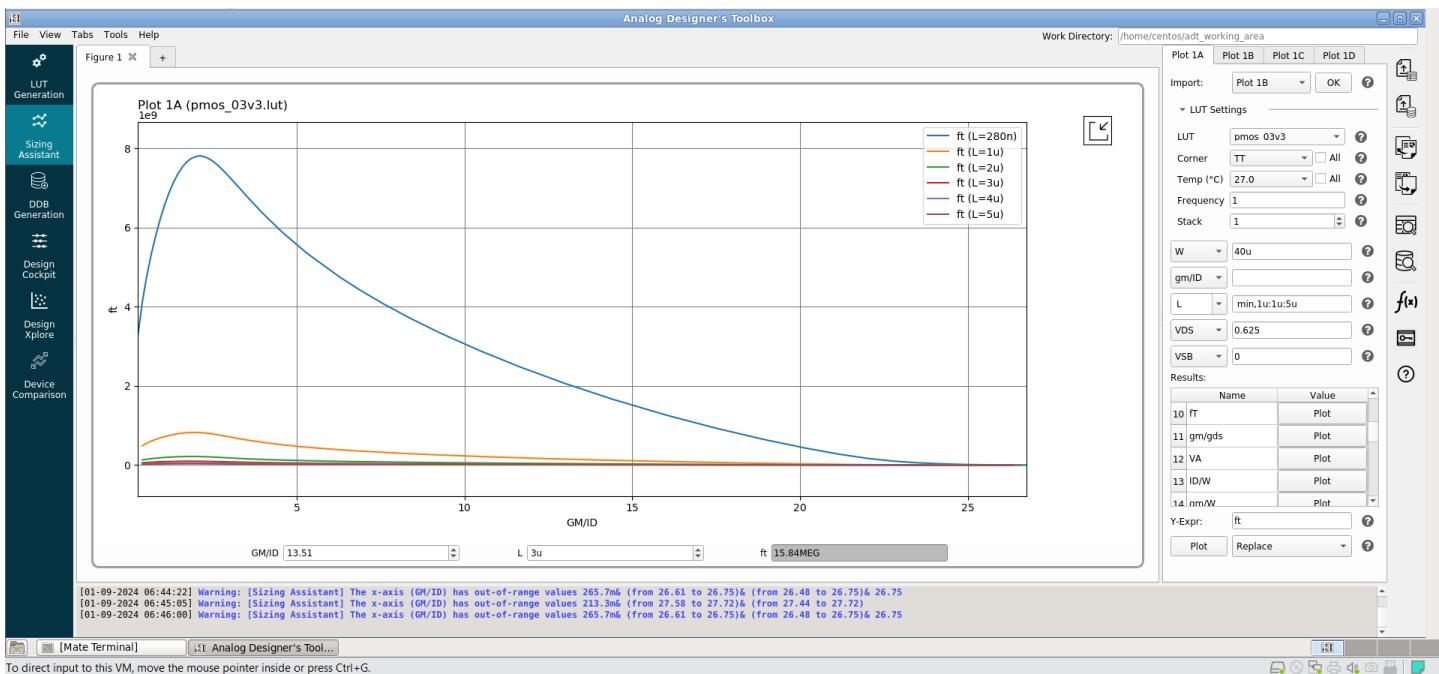
2. W/ID



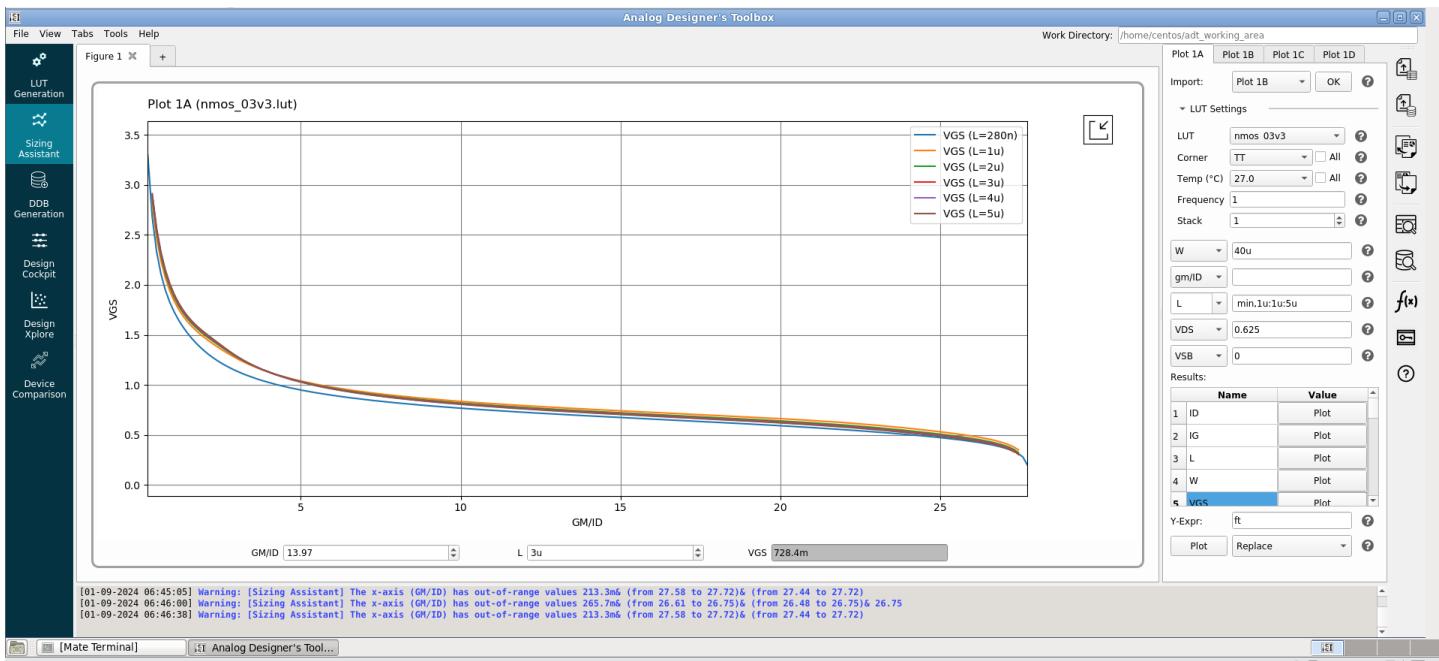


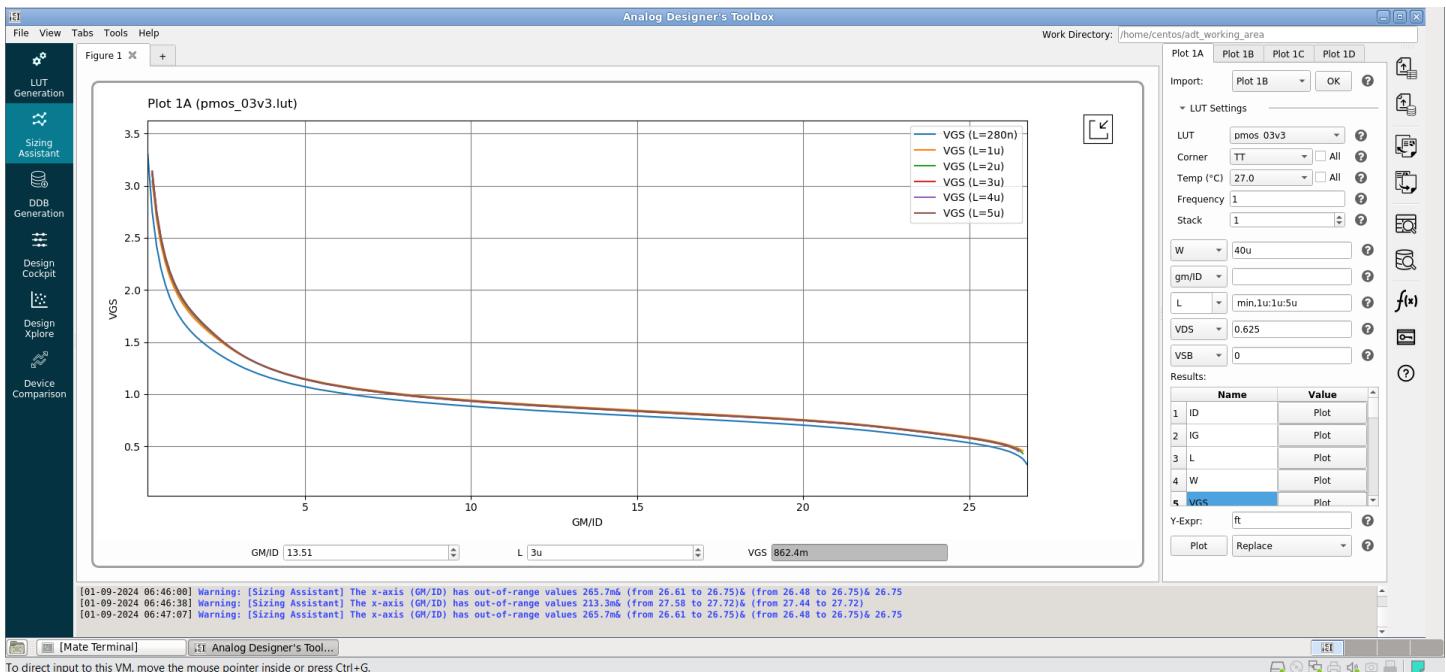
3. Ft





4. VGS





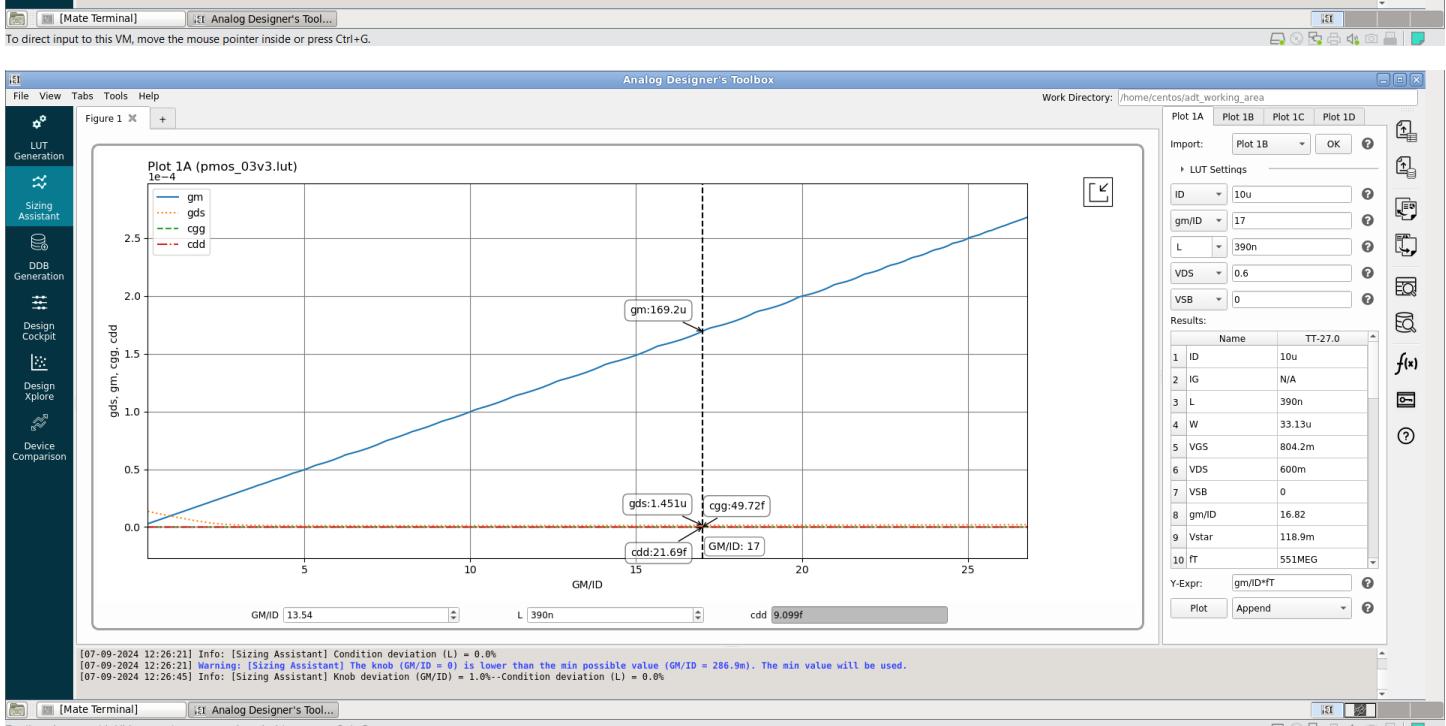
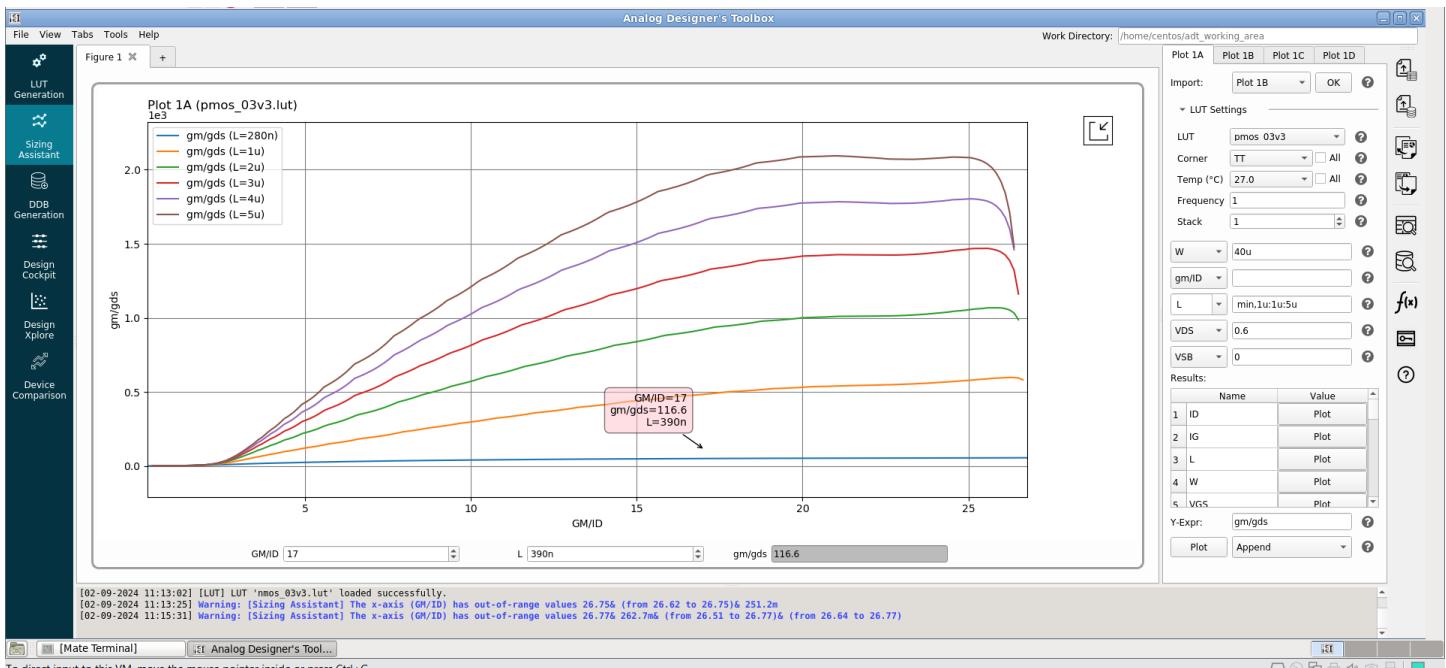
PART 2: OTA Design

Design a fully-differential folded cascode OTA with capacitive feedback that meets the specifications below. The current consumed in the biasing branches (current mirrors) is not included in the specifications.

Technology	GF180MCU
Supply	2.5V
Closed loop gain	2
Phase margin at the required ACL	>=70deg
CM input range – low	<=0
CM input range – high	>=1V
Differential output swing	1.2Vpk-to-pk
Load	500fF
DC Loop gain	60db
CL settling time for 1% error	100nS

DESIGN PROCEDURE

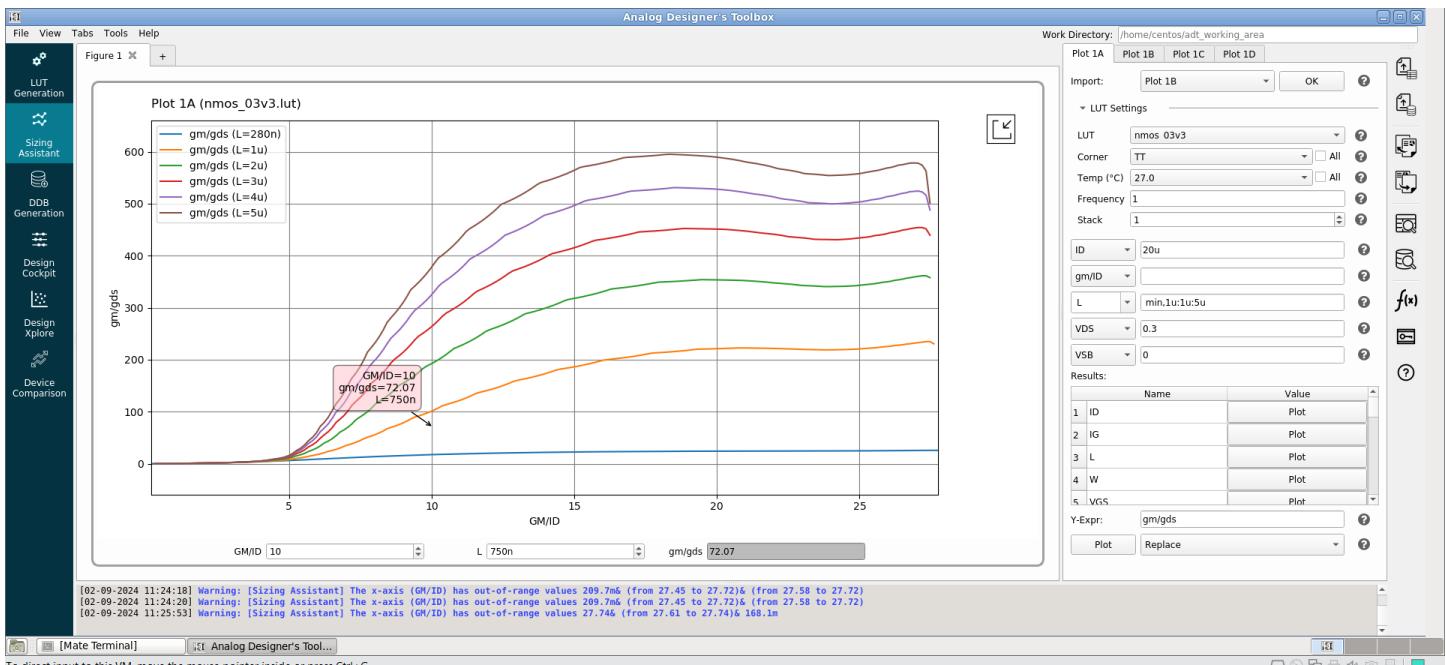
- 1) As $\beta \approx \frac{C_f}{C_f + C_s} = \frac{1}{3}$, $LG = 60\text{db}$, then $A_{vol} = \frac{LG}{\beta} = 70\text{db}$.
- 2) As $T_s = -\ln(0.01)^*\tau_{cl} = 4.605^*\tau_{cl}$, then $\tau_{cl} = 21.715\text{ns}$ or, $w_u = \frac{\tau_{cl}}{t}$, $A_{cl} = \frac{1}{\beta} = 3$, $\tau_{cl} = 21.715\text{nS}$, then $W_u = 138.15\text{Mrad/s} = 22\text{MHz}$.
- 3) As $W_u = \frac{gm1}{CL + Cout}$, $Cout = (C_f || (C_s + C_{in}))$, assume $C_{in} = 0$ and I will revisit it, then $Cout = C_f || C_s = \frac{2}{3}\text{pF}$, then $gm1 = 161.175\mu\text{S}$, assume $(gm/ID)_1 = 15$, then $ID1 = 10\mu\text{A}$ and $gm/ID = 17$.
- 4) Assume all $\frac{gm1}{gds1} = \frac{gm3}{gds3} = \frac{gm4}{gds4}$, $gds2 = 2gds1 = 2gds5$, $Rout = \frac{gm3}{gds3} * \frac{1}{gds1 + gds2} || \frac{gm4}{gds4 * gds5} = \frac{gm1}{4 * gds1^2}$
Then $A_{vol} = \frac{1}{4} * (\frac{gm1}{gds1})^2$, then $\frac{gm1}{gds1} = 2\sqrt{A_{vol}} = 109.55\text{V/V}$.



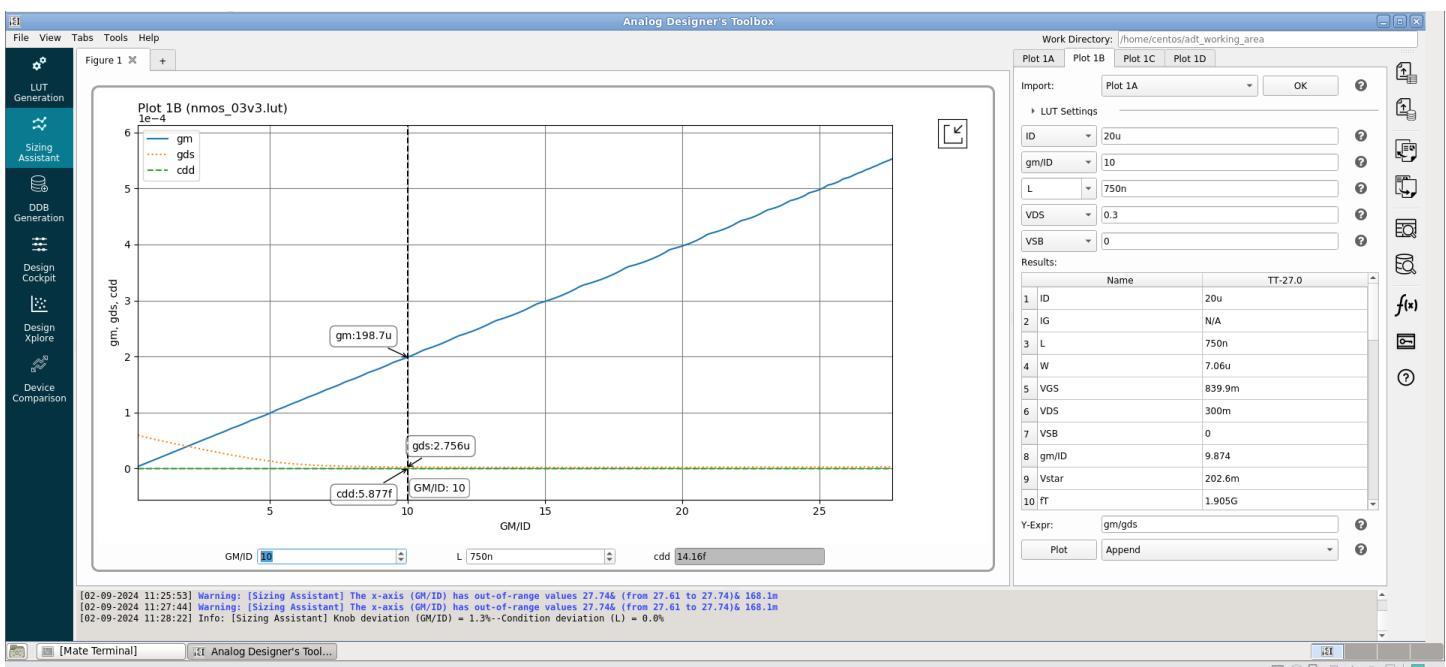
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

L1=390nm ,W1=33.1um ,Cgg=47.18fF as we see Cgg1 is very small compare to Cs and Cf so that neglecting Cgg1 is justified.

5) As ID2=2ID1=20uA , gds2=2gds1=2*.5u=2.9uS , assume (gm/ID)2=10 , gm=200uS , (gm/gds)5=69V/V.



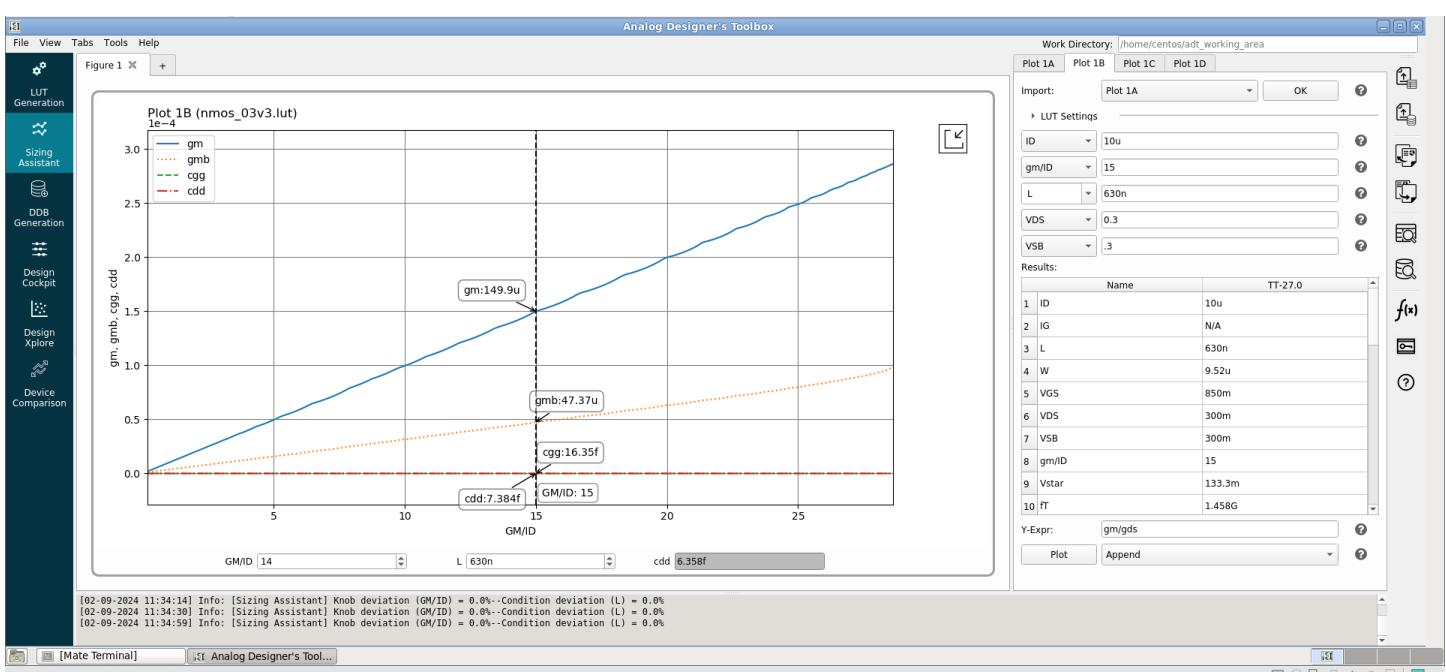
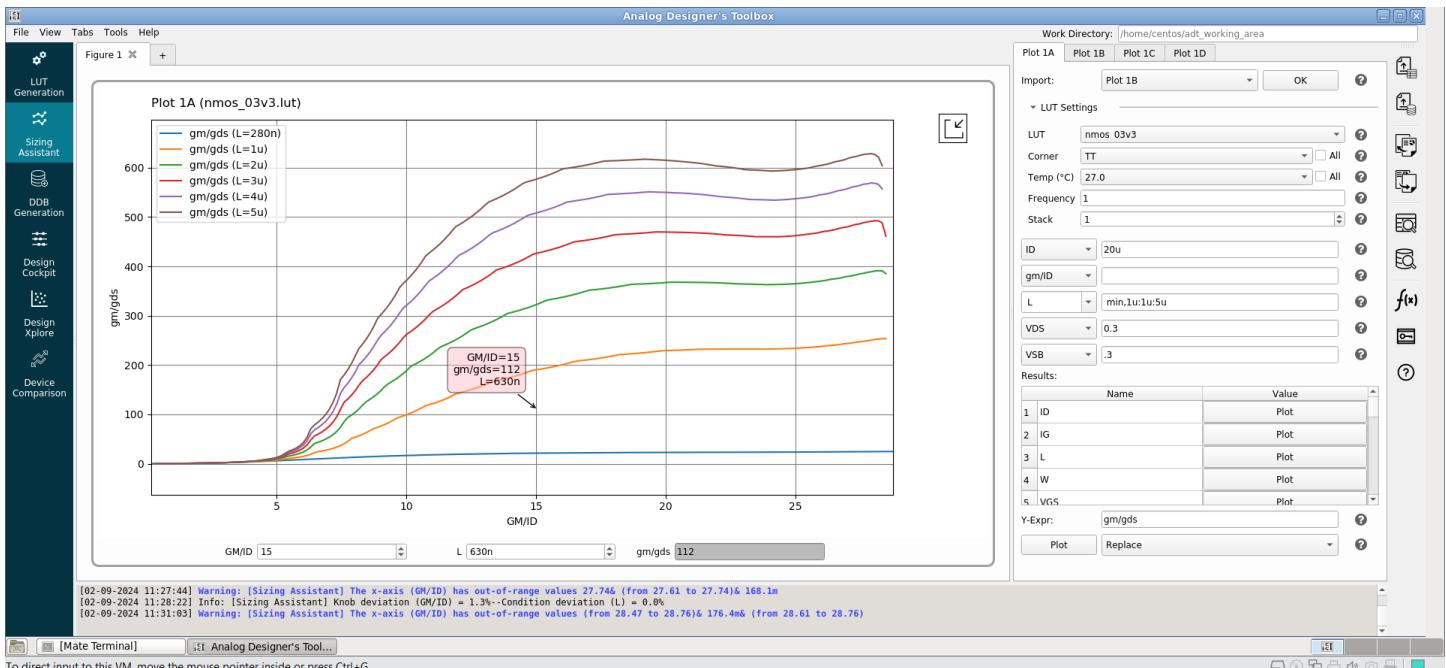
To direct input to this VM, move the mouse pointer inside or press Ctrl+G.



To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

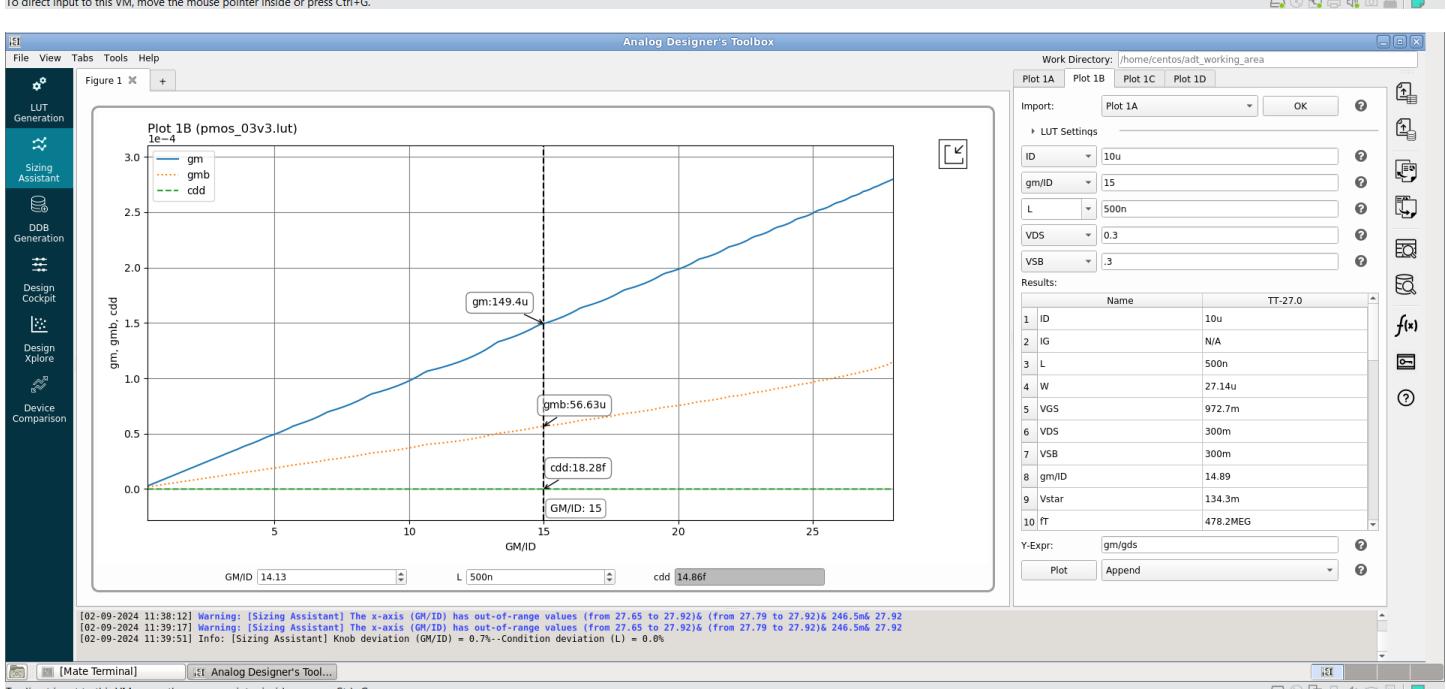
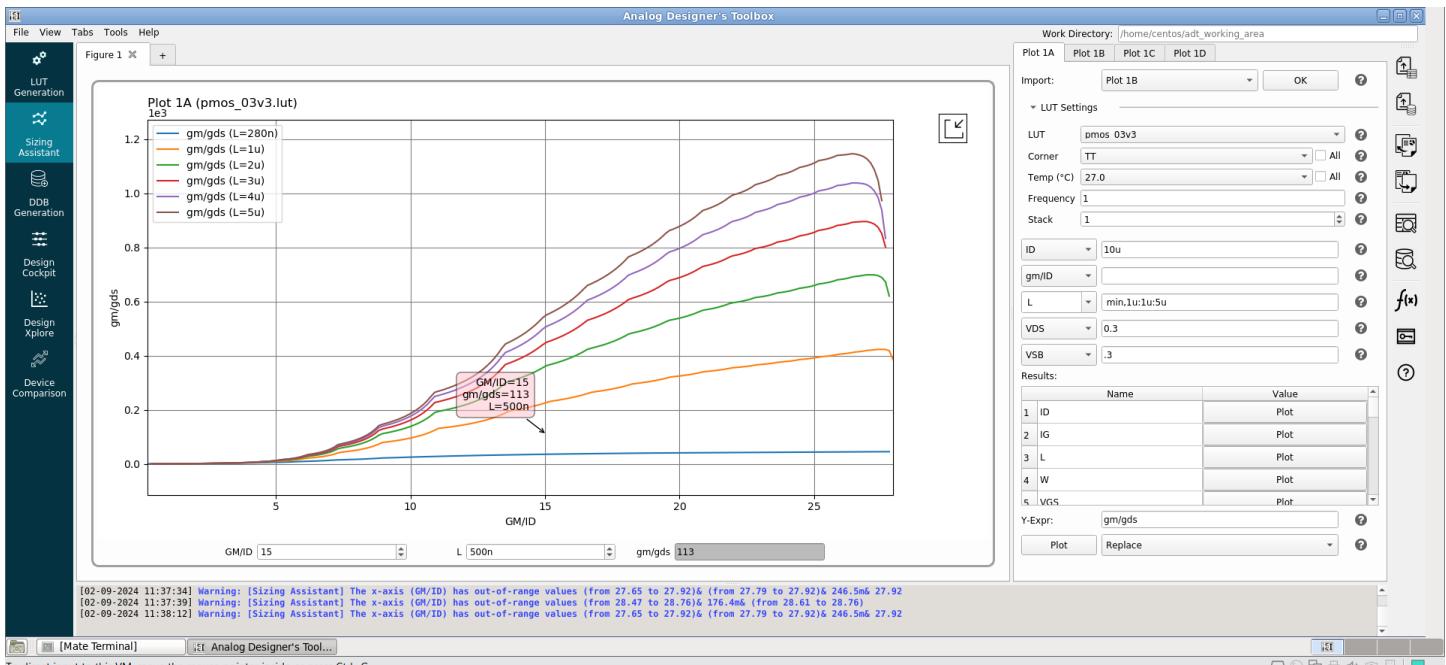
L2=750nm ,W2=7.06um , gds5=2.76uS.

6) As we assumed that $\frac{gm_1}{gds_1} = \frac{gm_3}{gds_3} = 109.6$ V/V , assume (gm/ID)=15 , to include body effect Vsb=VDS2=.3V.



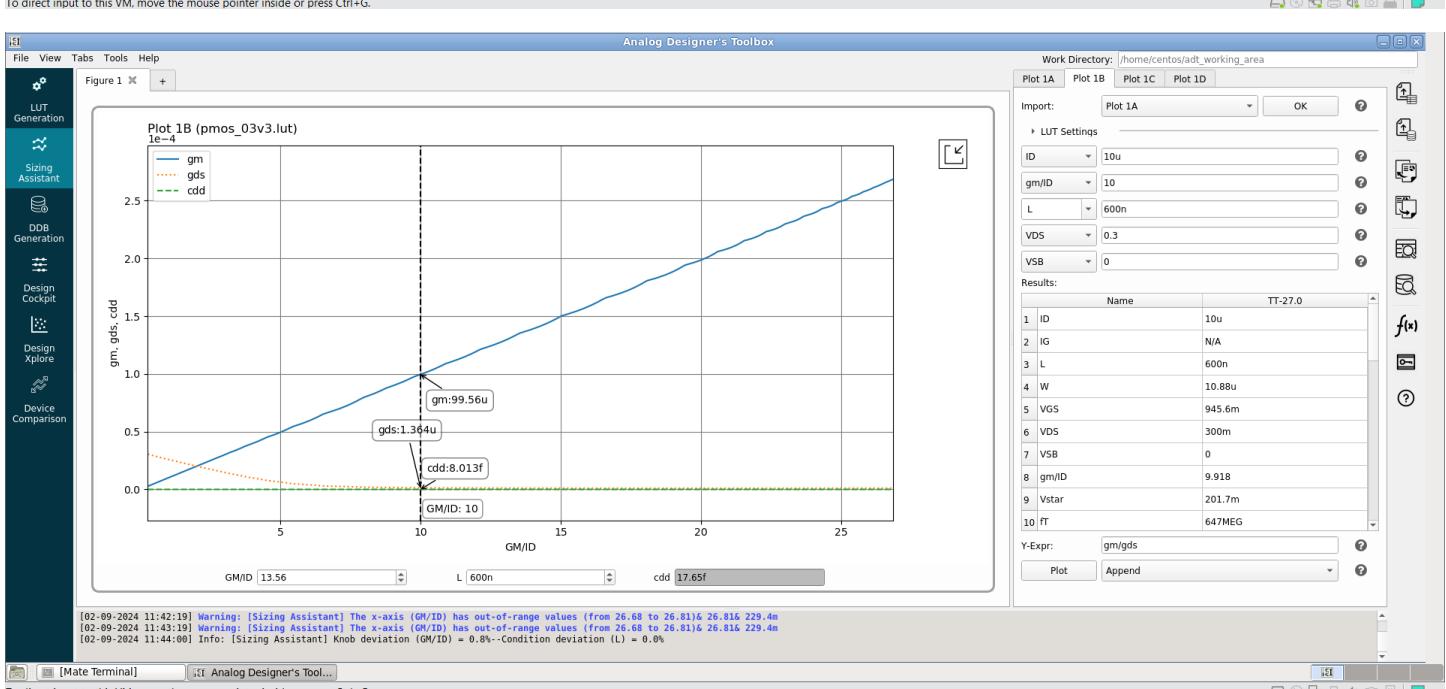
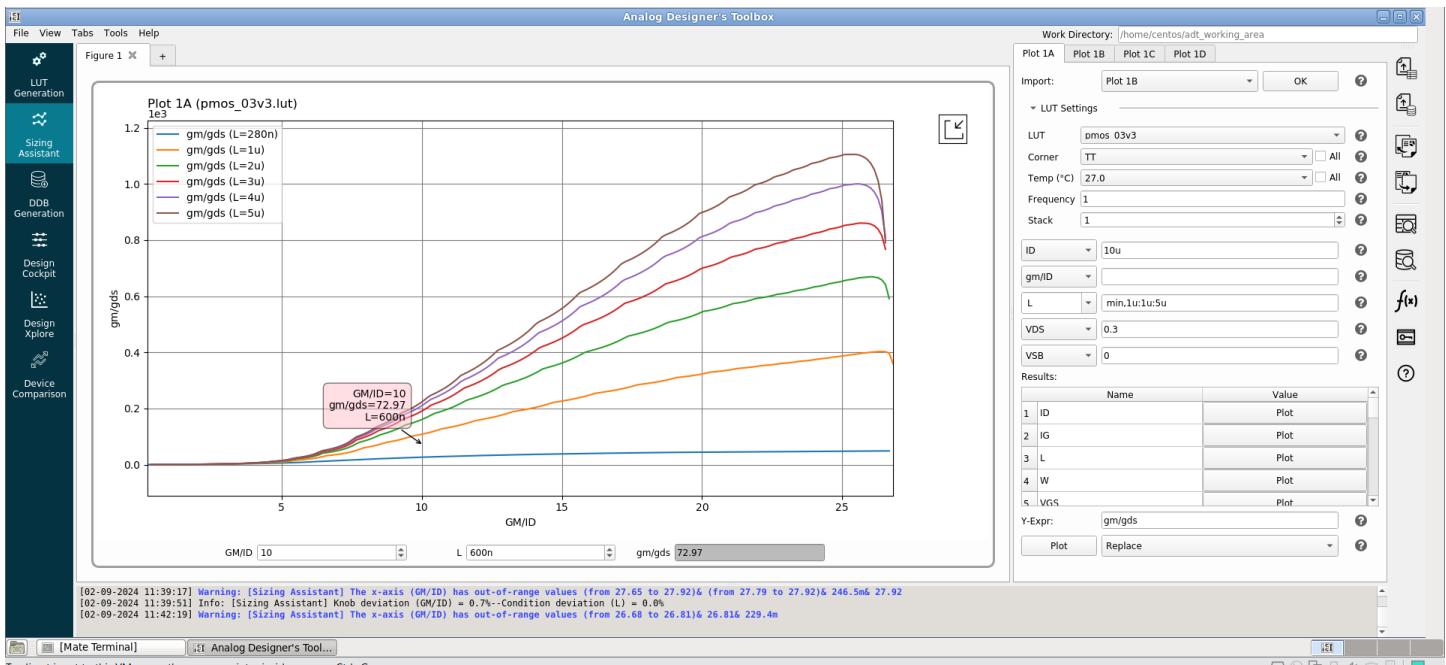
L3=630nm , W3=9.52um , Cdd=7.4ff as we see Cgg3 is negligible compared to CL.

7) As we assumed that $\frac{gm1}{gds1} = \frac{gm4}{gds4} = 109.6$ V/V , assume (gm/ID)=15 , to include body effect $|Vsb| = VDD - (VDD - VDS5)$, assume $VDS5=.3V$, then $|Vsb|=.3V$.



L4=500nm , W4=27.14um , Cdd4=18.28fF.

8) As gds5=gds1=1.4uS , ID=10uA ,assume (gm/ID)5=10 , then gm=100uS , gm/gds=72V/V



L5=600nm , W5=10.9um.

9) as $(gm/ID)_6$ must equal to $(gm/ID)_5$, and $L_6=L_5=600nm$, $(gm/ID)_6=10$, $ID_6=20\mu A$, $W_6=2W_5=22\mu m$.

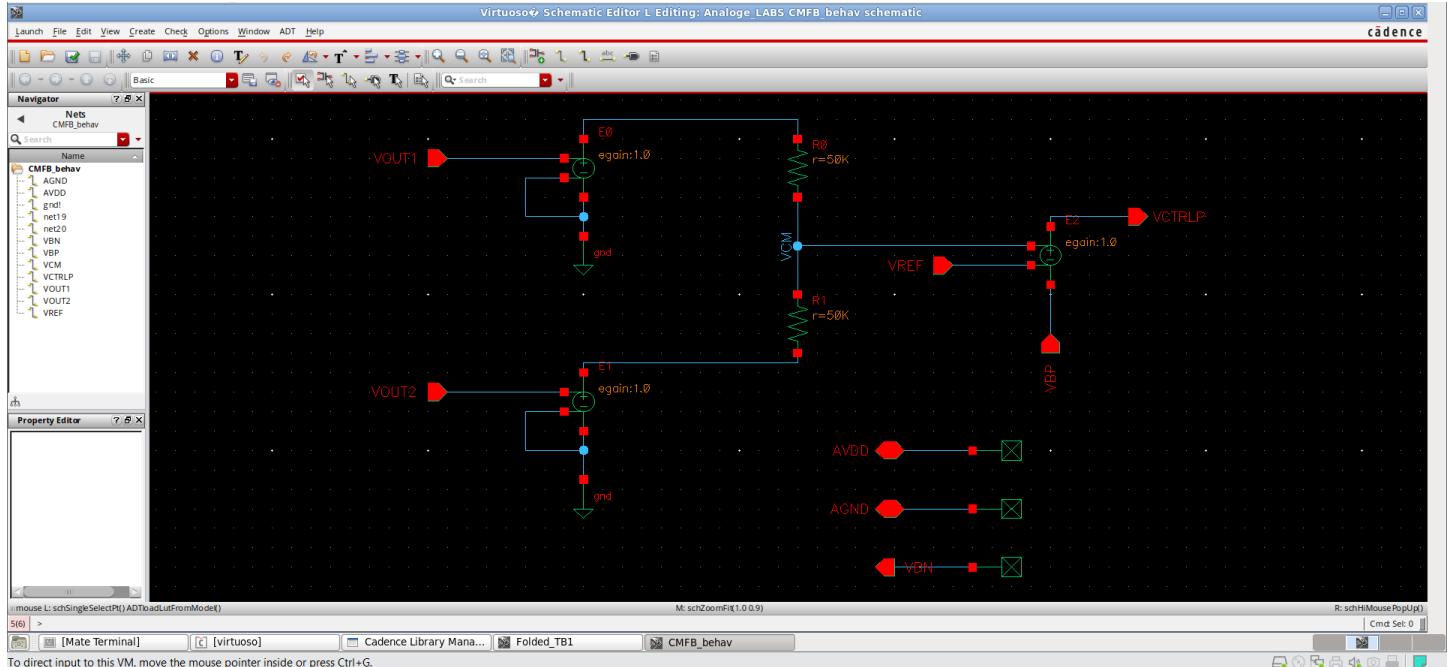
Then:

$$VCASN=VGS3+VDS2=850m+300m=1.15V.$$

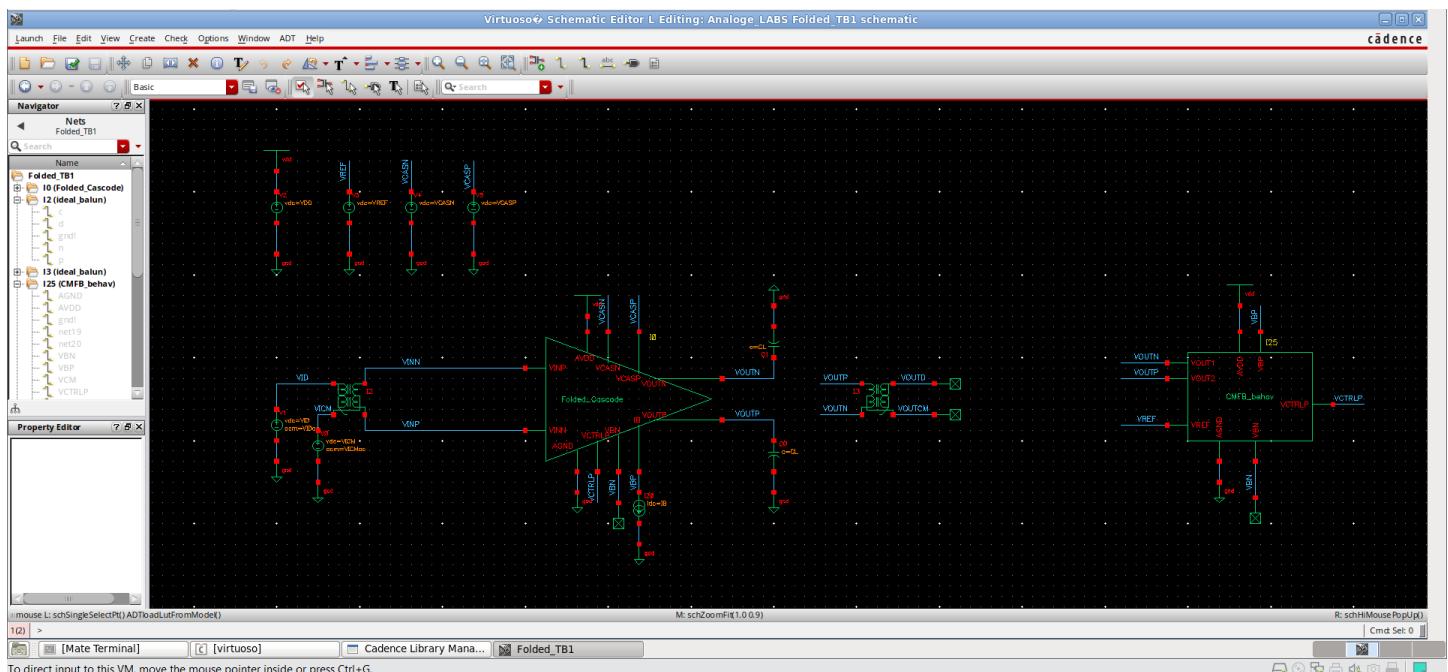
$$VCASP=VDD-VDS5-VGS4=2.5-.3-.973=1.23V.$$

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

We will start with a behavioral CMFB network similar to the one shown below. We use ideal buffers to avoid loading the OTA output with the CM sensing resistors. Note that we don't need high gain in the CMFB loop (why?); thus, we use a gain = 1 in the error amplifier. We use dummy pins in the behavioral CMFB circuit to be "pin-accurate" with the actual CMFB circuit we will use later.

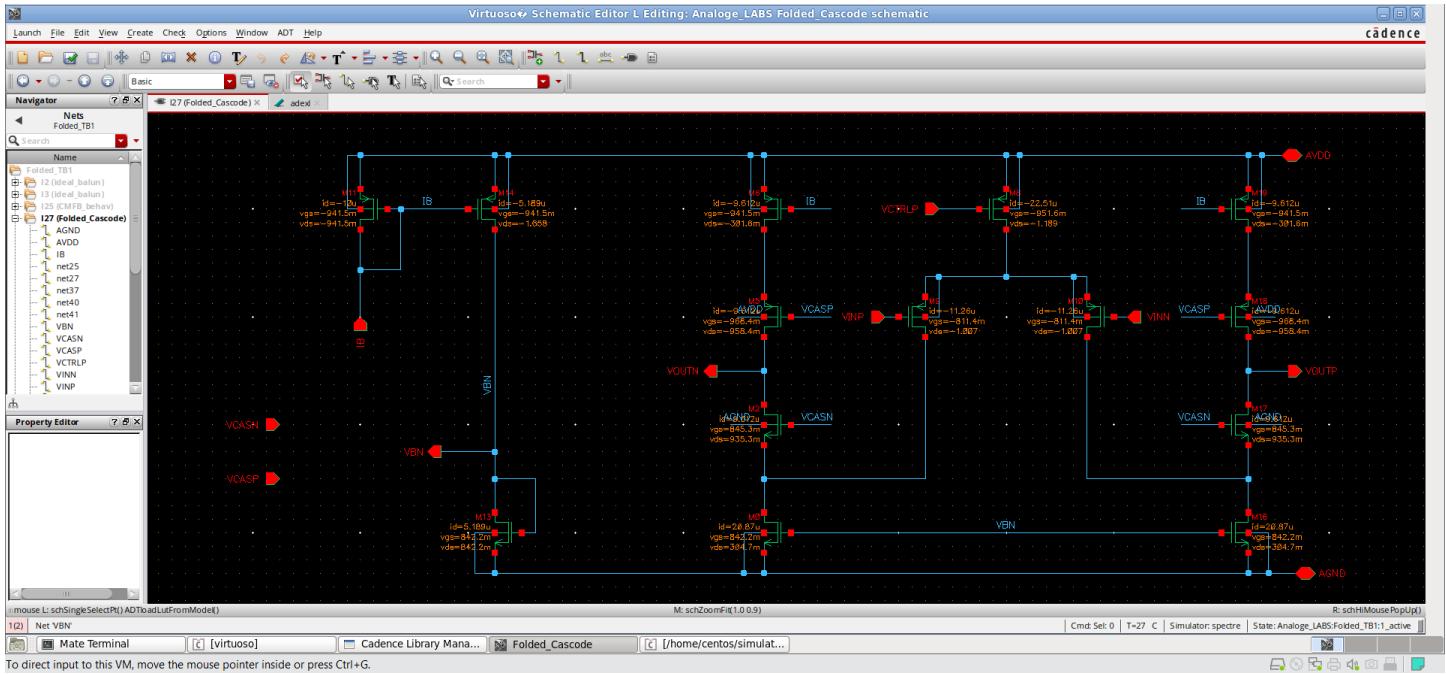


Create a testbench similar to the one shown below.

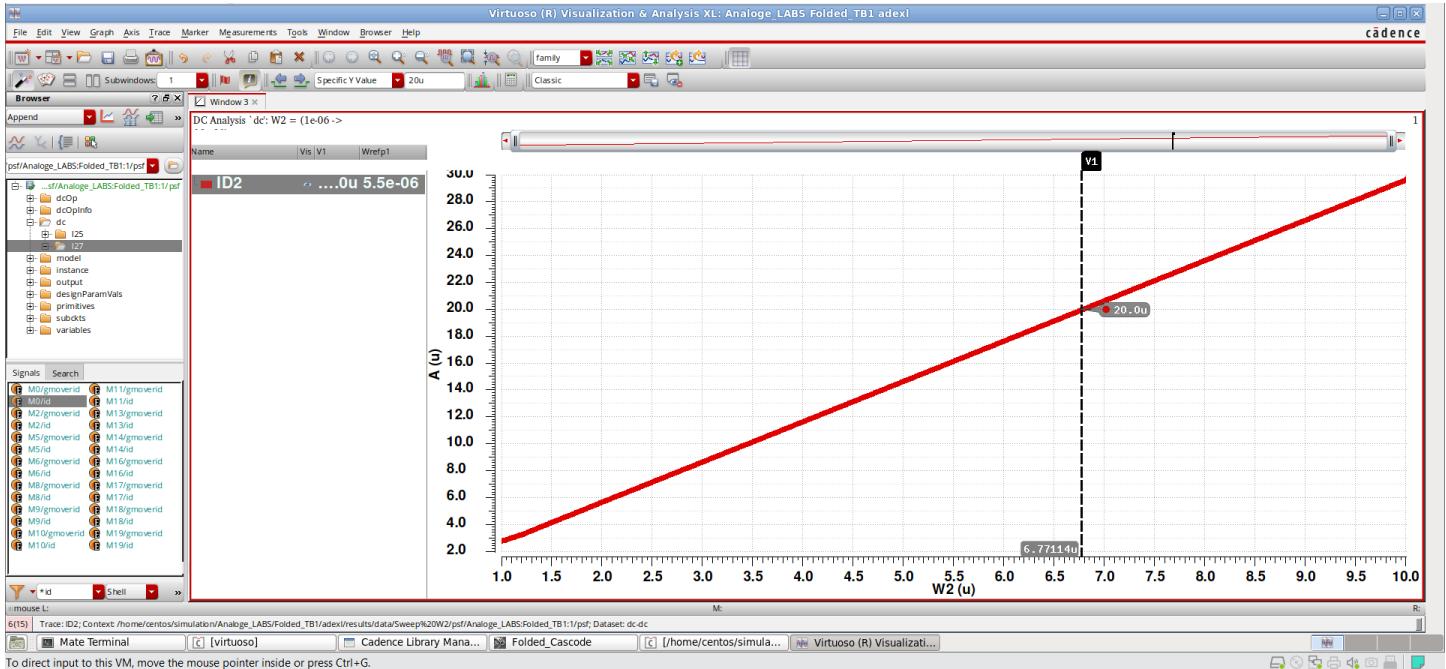


Report the following:

- 1) Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.

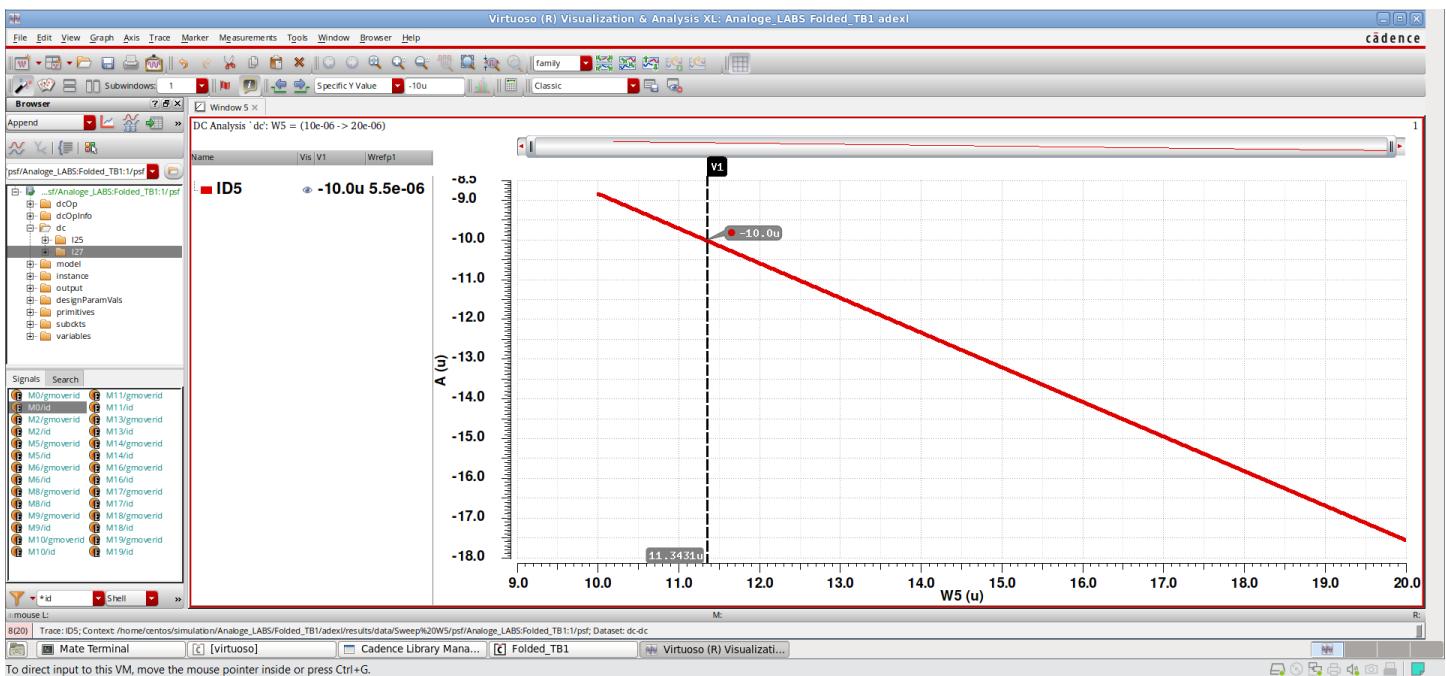


As we see ID1 and ID2 is slightly higher than the designed value , so I will sweep W2 to decrease ID2.



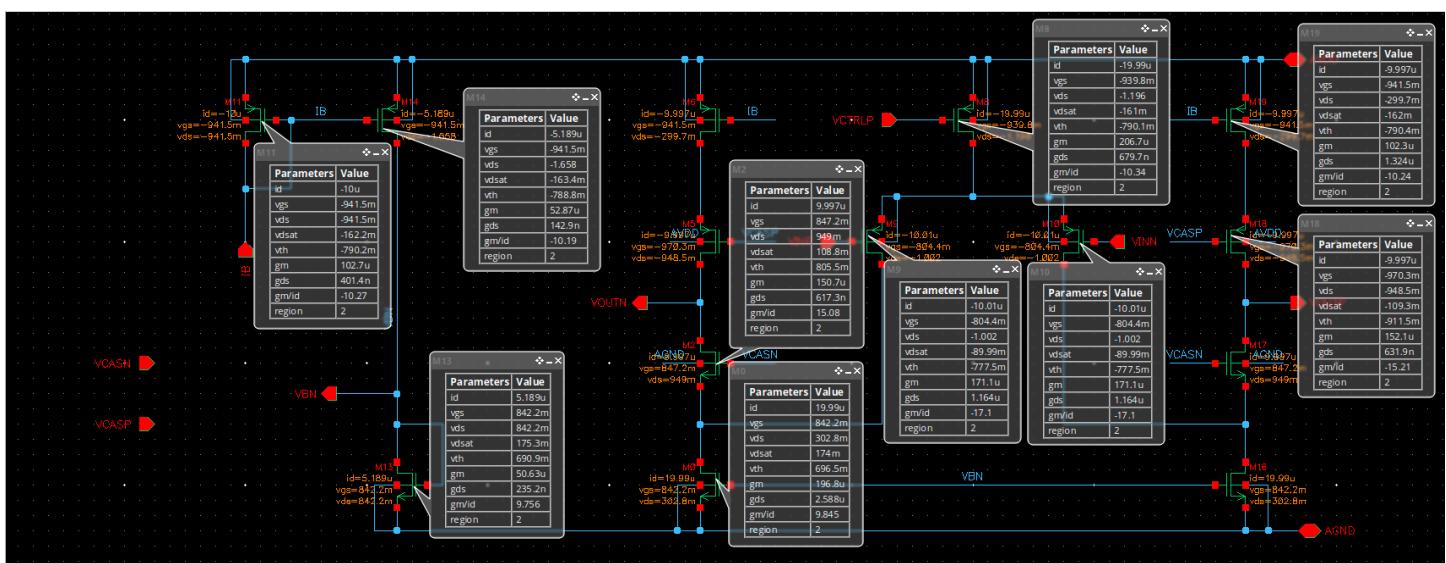
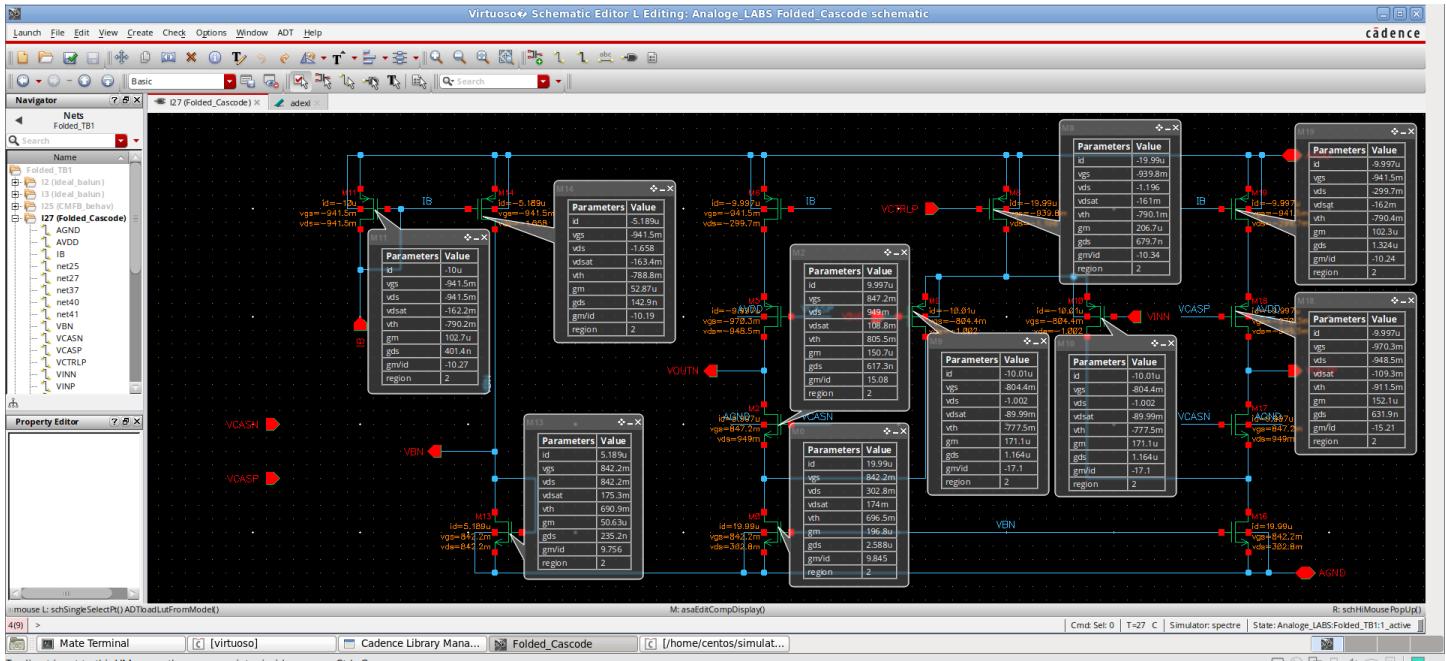
$W2=6.77\mu m$.

Now I will sweep W5 to increase ID5 and that result in increase in ID1.



W5=11.34um.

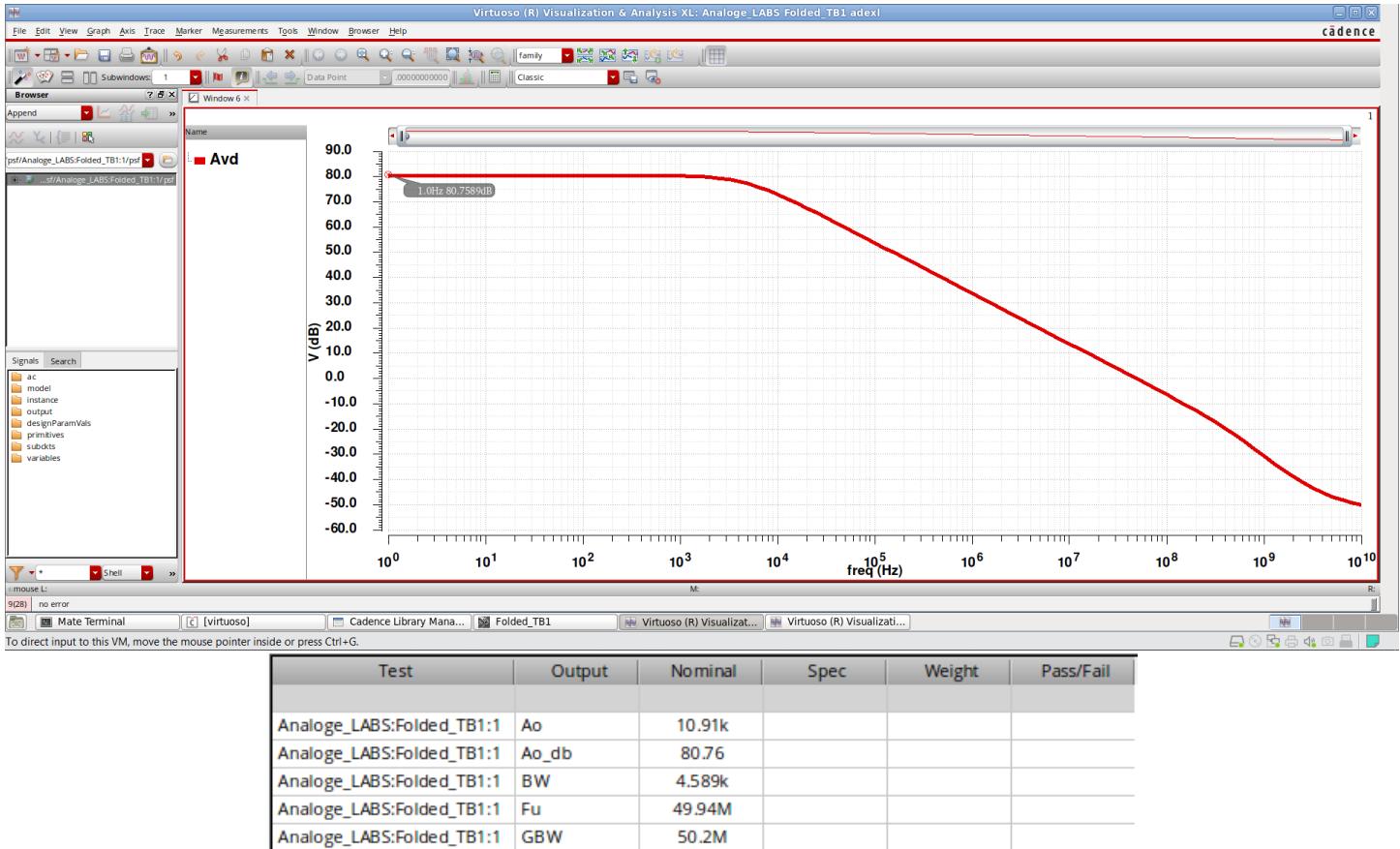
- Set VICM at the middle of the CMIR.
- Select VREF to maximize the symmetrical output swing.



- What is the CM level at the OTA output?
- ✓ $V_{out} = V_{DS2} + V_{DS3} = 302.8m + 949m = 1.2518V$.
- What are the differential input and output voltages of the error amplifier? What is the relation between them?
- ✓ $V_{ID} = V_{out} - V_{ref} = 1.2518 - 1.25 = 1.8mV$.
- ✓ $V_{outD} = V_{CTRLP} - V_{BP} = 1.5602 - 1.5585 = 1.7mV$.
- ✓ $V_{outD}/V_{ID} \approx 1$, equal to the gain of the error amplifier.

2) Diff small signal ccs:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VIDAC = 1 and VICMAC = 0.
- Set VICM at the middle of the CMIR.
- Plot diff gain (magnitude in dB and phase) vs frequency.



- Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

$$A_{vd} = GM * R_{out}$$

$$GM \approx gm_1 = 171.1 \mu S.$$

$$R_{out} \approx [gm_3 * ro_3 * (ro_1 || ro_2)] || [gm_4 * ro_4 * ro_5] = \frac{gm_3}{gds_3 * (gds_1 + gds_2)} || \frac{gm_4}{gds_4 * gds_5} = 44 M\Omega$$

$$A_{vd} = 171.1 \mu * 44M = 7.53Kv/v$$

$$BW \approx \frac{1}{2\pi * R_{out} * C_{out}}, Cout = CL + Cdd3 + Cdd4 = .5p + 7.4f + 18.28f.$$

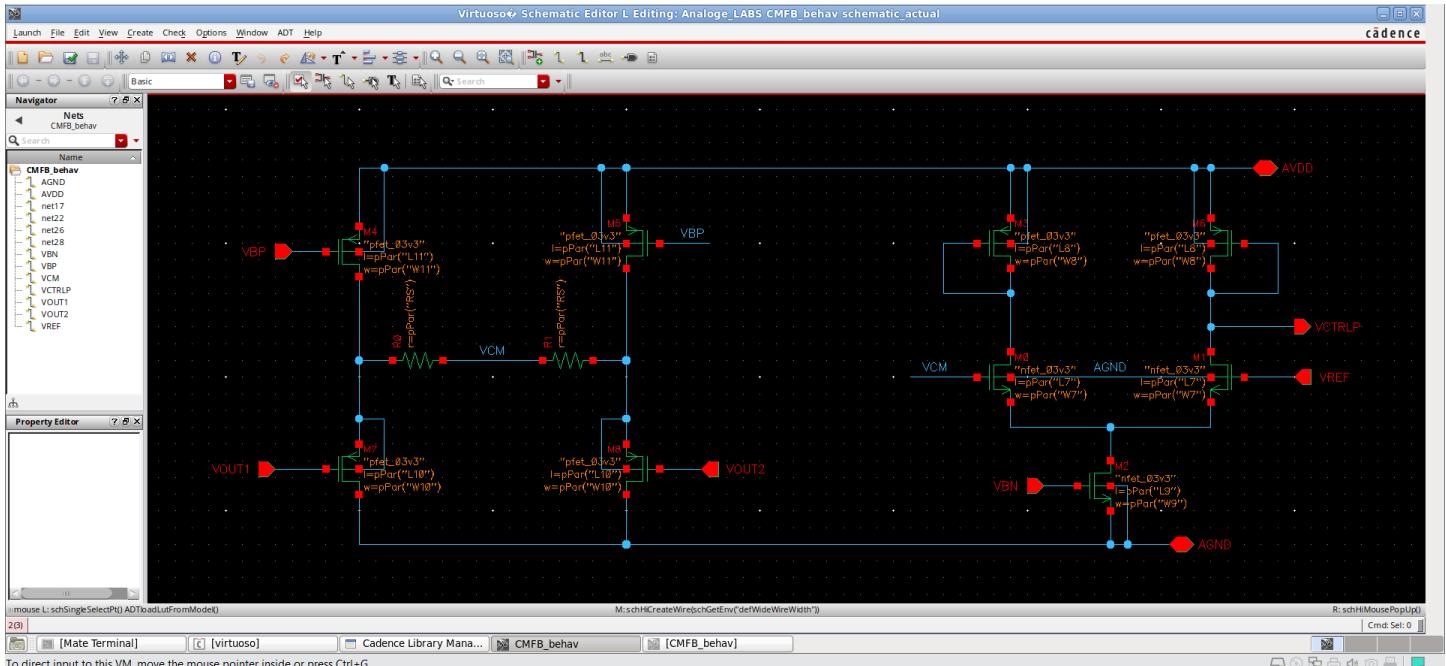
$$BW \approx \frac{1}{2\pi * 44M * .53p} = 6.9 KHz.$$

$$GBW \approx A_{vd} * BW = 51.96 MHz.$$

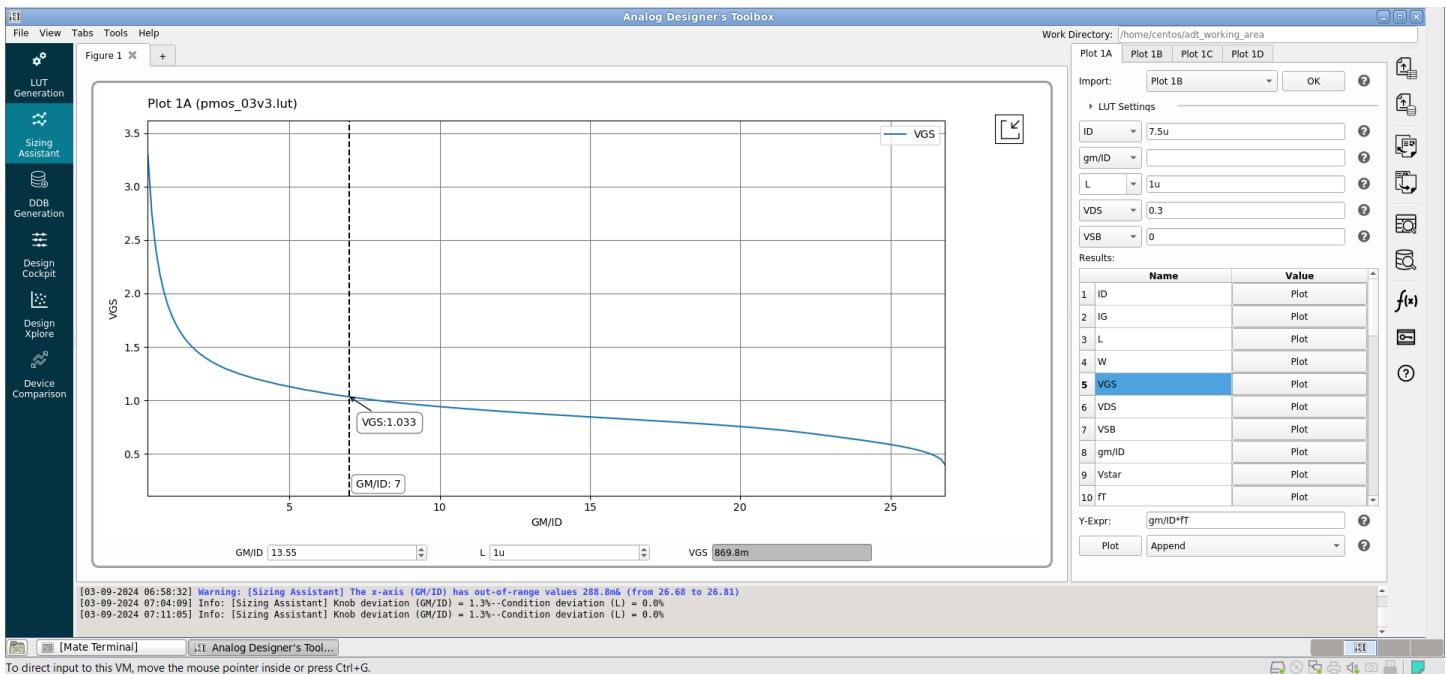
- Compare simulation results with hand calculations in a table

	Hand Analysis	Simulation
A_{vd}	$7.53K = 77db$	$10.91K=80db$
BW	$6.9KHz$	$4.6KHz$
GBW	$51.96MHz$	$50.2MHz$
F_u	$51.96MHz$	$49.49MHz$

PART 4: Open-Loop OTA Simulation (Actual CMFB)



- As the OTA consume about 40uA (without basing circits) , so that 20uA for the CMFB circuit is reasonable.
 - as M8 will bias M6 (M6 is PMOS tail current source of the input pair) , so M8 must have the same L and gm/ID as M6 , then $L8=600\text{nm}$ and $(\text{gm}/\text{id})8=10$, as $\text{ID}8=\frac{\text{ID}6}{8}$, then $W8=.125*W6=2.75\mu\text{m}$.
 - As M9 mirror the current from Mrefn , so that must have the same length and gm/id as Mrefn , then $L9=750\text{nm}$, $(\text{gm}/\text{id})9=10$, $\text{ID}9=5\mu\text{A}$, as $\text{ID}9=\frac{\text{ID}2}{4}$, then $W9 = .25 * W2 = 1.8\mu\text{m}$.
 - As M11 mirror from Mrefp , so that should have the same L and gm/id , then $L11=600\text{nm}$ and $\text{gm}/\text{id}=10$ as $\text{ID}11=.75*\text{ID}refp$, then $W11=.75*Wrefp=8.2\mu\text{m}$.
- Note: I chose the current of the buffer stage greater than the current of the error amplifier as the differential output signal VpK-to-pK=1.2V , so that the maximum differential signal on the sensing resistance =.6V then the Current through the resistors =6uA, so that the current of the buffer stage must be greater than 6uA to sense the correct VCM , so that I chose ID11=7.5uA.
- As $Vdsat11=200\text{mV}$, and the swing at the output .6 peak to peak so , that M11 must have VDS margin at least 300mV ,so that we chose $VDS11=500\text{mV}$, we set $Voutcm=1\text{V}$ to maximize the output swing , then $VGS10<= (2.5-.5)-1=1\text{V}$, if we assume $L11=1\mu$ then the minimum $(\text{gm}/\text{ID})10=7$.
 - I will chose $(\text{gm}/\text{id})10=12$, then $L10=1\mu$, $W10=24.13\mu\text{m}$.
 - As $VCM=VICM+|VGS|11=1+.9=1.9\text{V}$.



Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK

LUT Settings:

ID	7.5u
gm/ID	12
L	1u
VDS	0.3
VSB	0

Results:

	Name	TT-27.0
1	ID	7.5u
2	IG	N/A
3	L	1u
4	W	24.13u
5	VGS	898.7m
6	VDS	300m
7	VSB	0
8	gm/ID	11.96
9	Vstar	167.3m
10	fT	170.7MEG

Y-Expr: gm/ID*fT

h) I will chose (gm/id)=15 , L7=500nm, then W7=1.94um.

Plot 1A Plot 1B Plot 1C Plot 1D

Import:

► LUT Settings

ID	2.5u	<input type="button" value="?"/>
gm/ID	15	<input type="button" value="?"/>
L	500n	<input type="button" value="?"/>
VDS	0.3	<input type="button" value="?"/>
VSB	0.3	<input type="button" value="?"/>

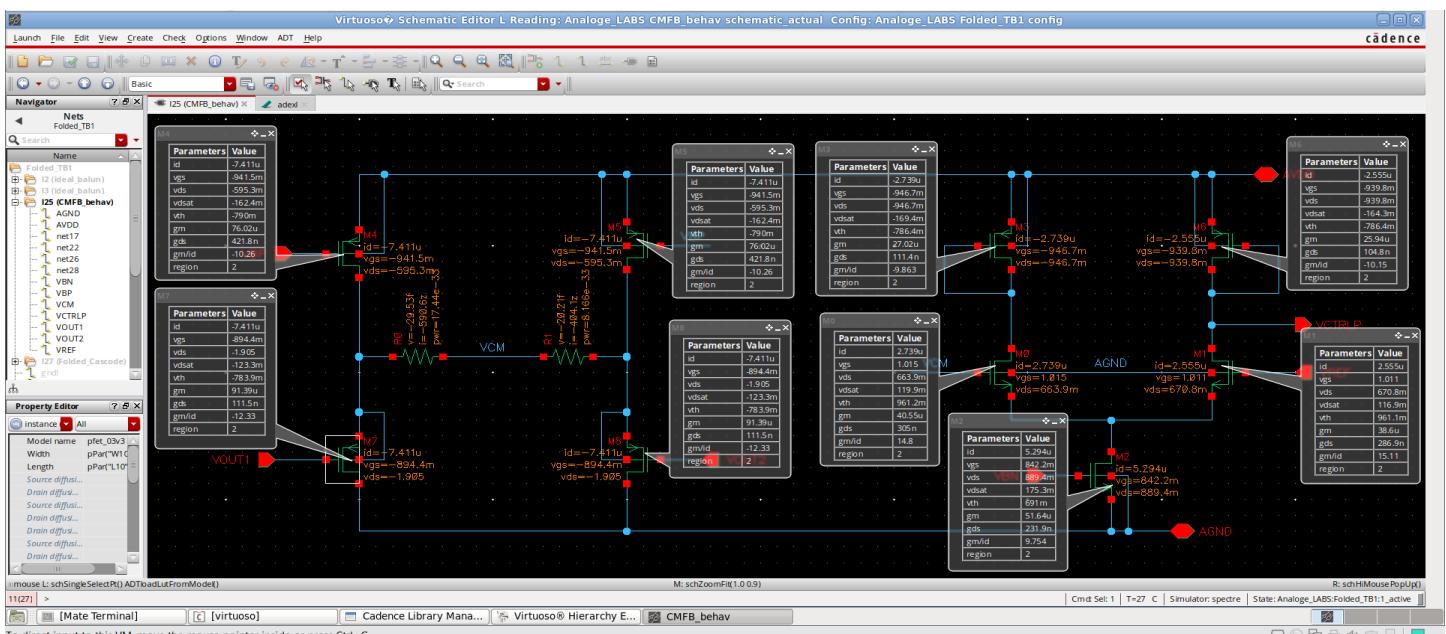
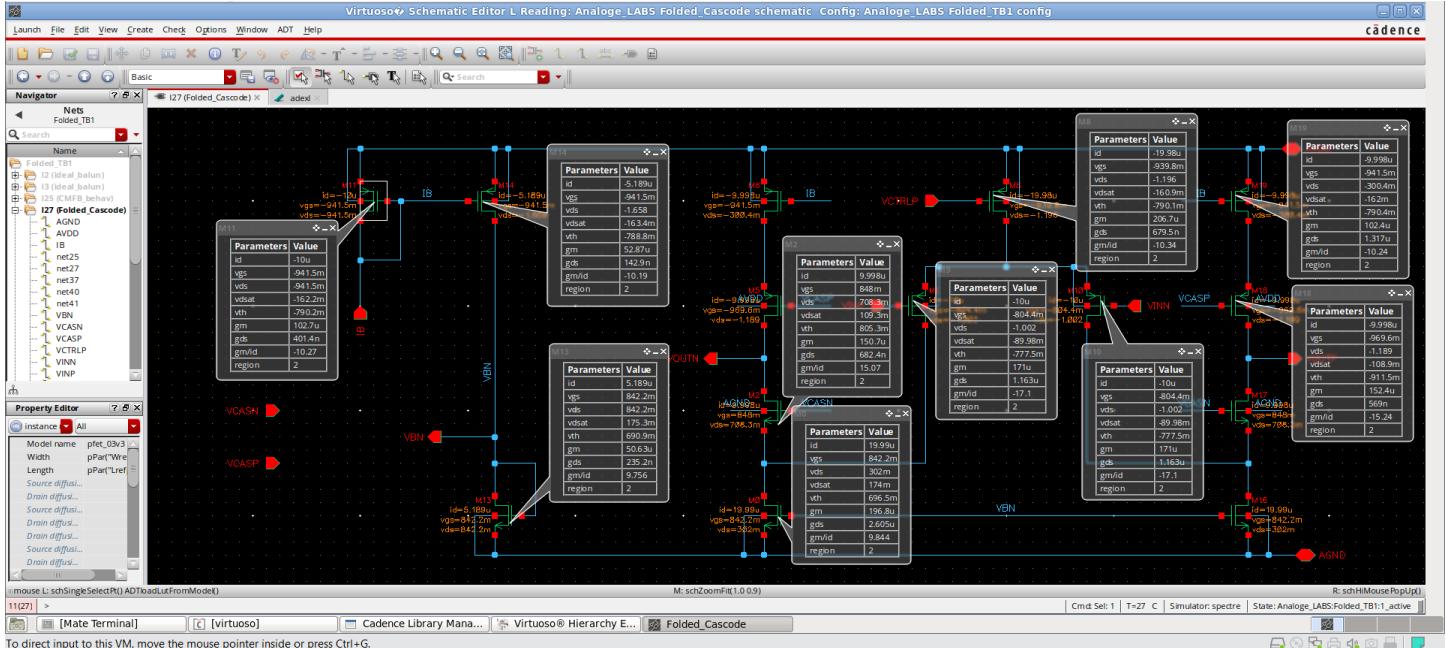
Results:

	Name	TT-27.0
1	ID	2.5u
2	IG	N/A
3	L	500n
4	W	1.94u
5	VGS	851.4m
6	VDS	300m
7	VSB	300m
8	gm/ID	14.94
9	Vstar	133.9m
10	fT	2.151G

Y-Expr:

Report the following:

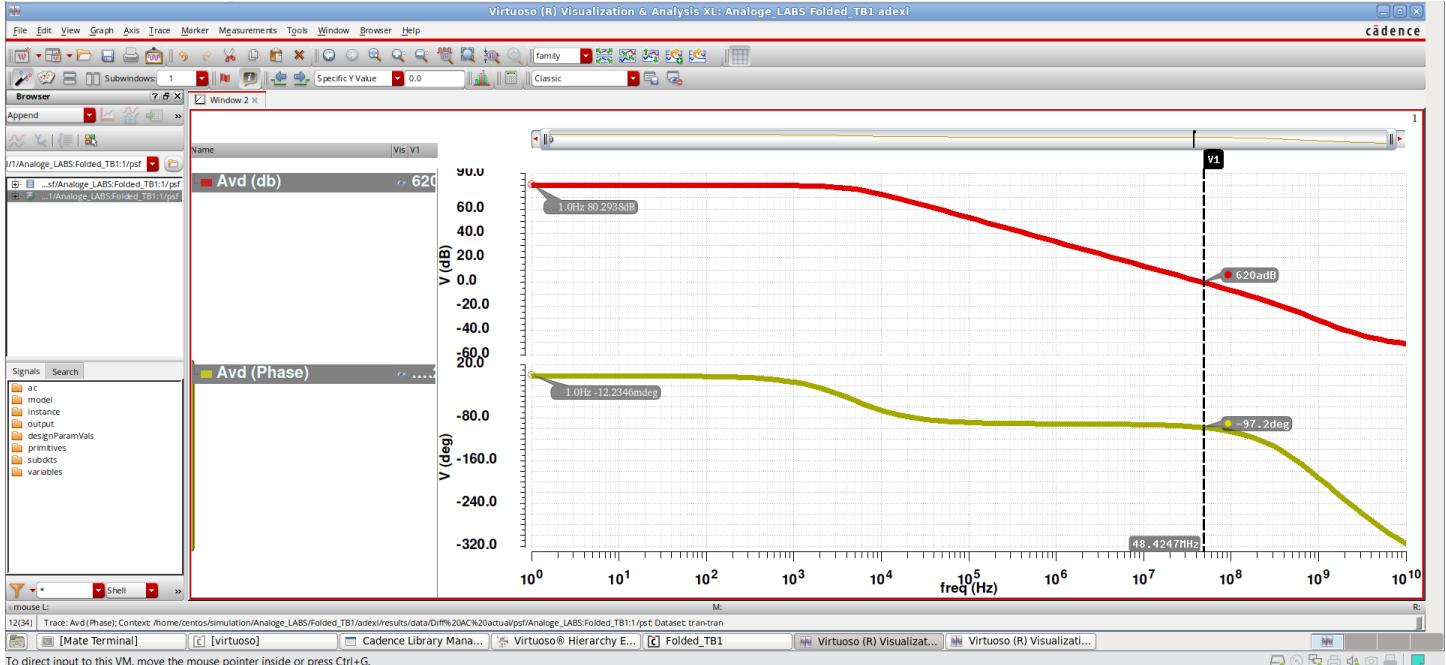
- 1) Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.



- Set VICM at the middle of the CMIR.
- What is the CM level at the OTA output? Why?
 - ✓ $V_{out} = V_{DS2} + V_{DS3} = 302m + 708m = 1.0103V$, we set $V_{ref} = V_{OCM} + V_{GS10} = 1 + 1.9 = 2.9V$, then V_{OCM} must be equal to $1V$, due to finite LG $V_{OCM} = 1.0103V$.
- What are the differential input and output voltages of the error amplifier? What is the relation between them?
 - ✓ $V_{ID} = V_{out} - V_{ref} + |V_{GS10}| = 1.0103 - 1.9 + .8944 = 4.7mV$.
 - ✓ $V_{outD} = V_{CTRLP} - V_{DD} + |V_{GS8}| = 1.5602 - 2.5 + .9467 = 6.9mV$.
 - ✓ $V_{outD}/V_{ID} \approx 1.5$, equal to the gain of the error amplifier.

2) Diff small signal ccs:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VIDAC = 1 and VICMAC = 0.
- Set VICM at the middle of the CMIR.
- Plot diff gain (magnitude in dB and phase) vs frequency.



Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB1:1	Ao	10.34k			
Analoge_LABS:Folded_TB1:1	Ao_db	80.29			
Analoge_LABS:Folded_TB1:1	BW	4.684k			
Analoge_LABS:Folded_TB1:1	Fu	48.58M			
Analoge_LABS:Folded_TB1:1	GBW	48.56M			
Analoge_LABS:Folded_TB1:1	PM	82.87			

Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

$$A_{vd} = GM * R_{out}$$

$$GM \approx gm_1 = 171\mu S.$$

$$R_{out} \approx [gm_3 * ro_3 * (ro_1 || ro_2)] || [gm_4 * ro_4 * ro_5] = \frac{gm_3}{gds_3 * (gds_1 + gds_2)} || \frac{gm_4}{gds_4 * gds_5} = 44M\Omega$$

$$A_{vd} = 171.1\mu * 44M = 7.53Kv/v$$

$$BW \approx \frac{1}{2\pi * R_{out} * C_{out}}, C_{out} = CL + C_{dd3} + C_{dd4} = 5p + 7.4f + 18.28f.$$

$$BW \approx \frac{1}{2\pi * 44M * .53p} = 6.9KHz.$$

$$GBW \approx A_{vd} * BW = 51.96MHz.$$

$$as W_{pnd} = \frac{1}{2\pi * R_{fold} * C_{fold}}, R_{fold} = \frac{1}{gm_3 + gds_3 + gds_2 + gds_1} = 6.5K\Omega, C_{fold} = C_{dd2} + C_{dd1} = 21.7f + 5.9f = 27.7fF, W_{pnd} = 887.5MHz.$$

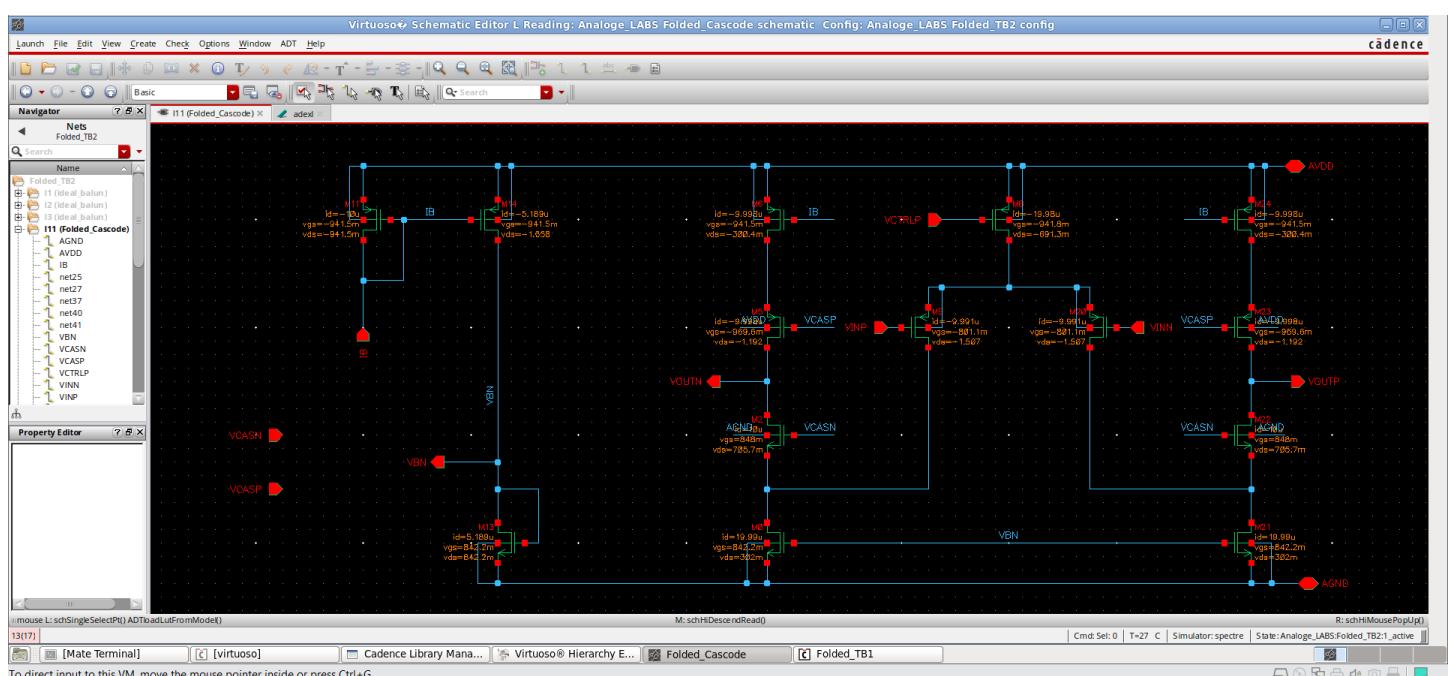
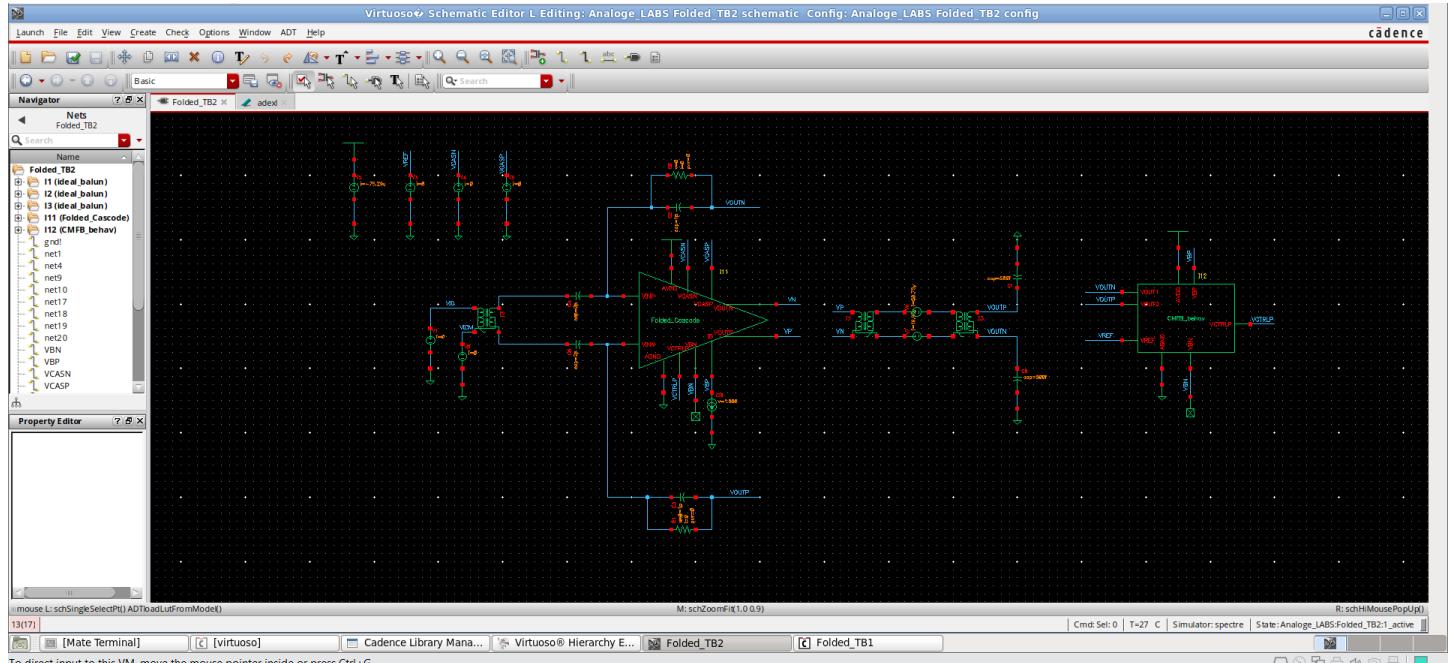
$$PM = 90 - \tan^{-1} \left(\frac{W_{pnd}}{W_{pd}} \right) = 89.99deg$$

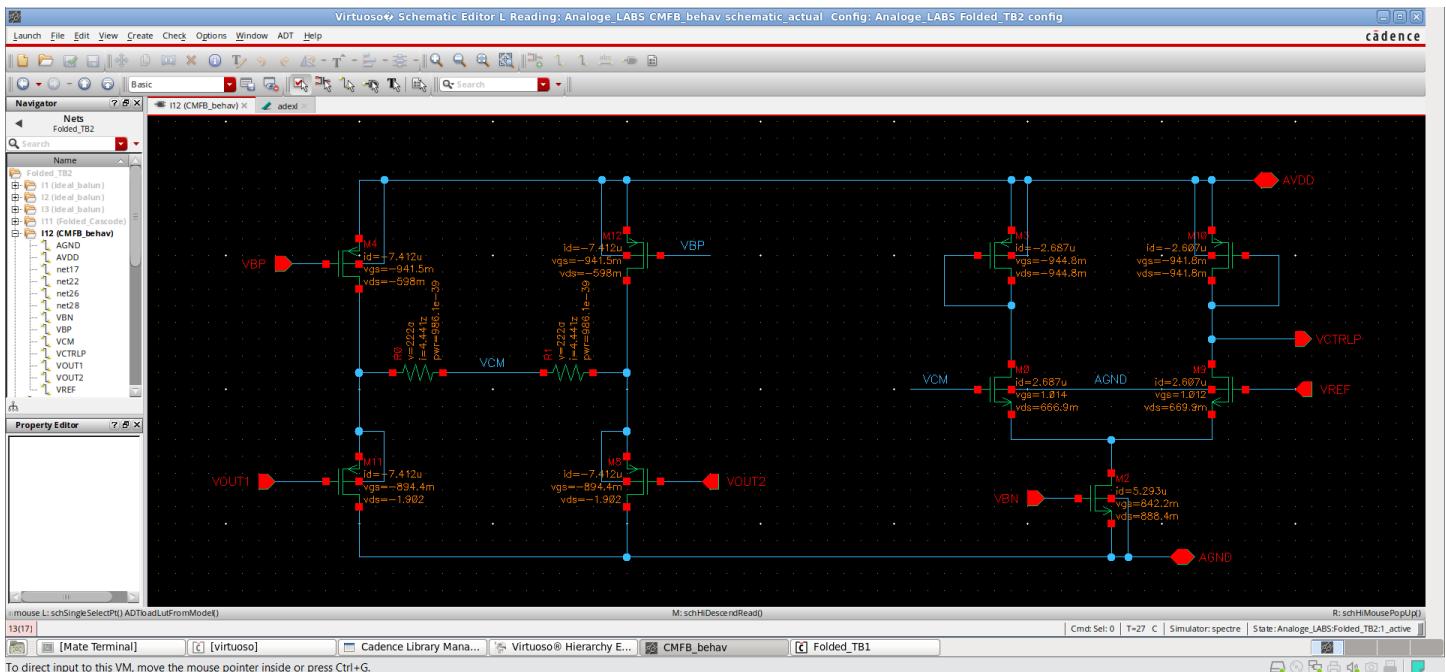
	Hand Analysis	Simulation
A_{vd}	$7.53K = 77db$	$10.34K=80db$
BW	$6.9KHz$	$4.68KHz$
GBW	$51.96MHz$	$48.56MHz$
F_u	$51.96MHz$	$48.58MHz$
PM	$89.99deg$	$82.87deg$

PART 5: Closed Loop Simulation (AC and STB Analysis)

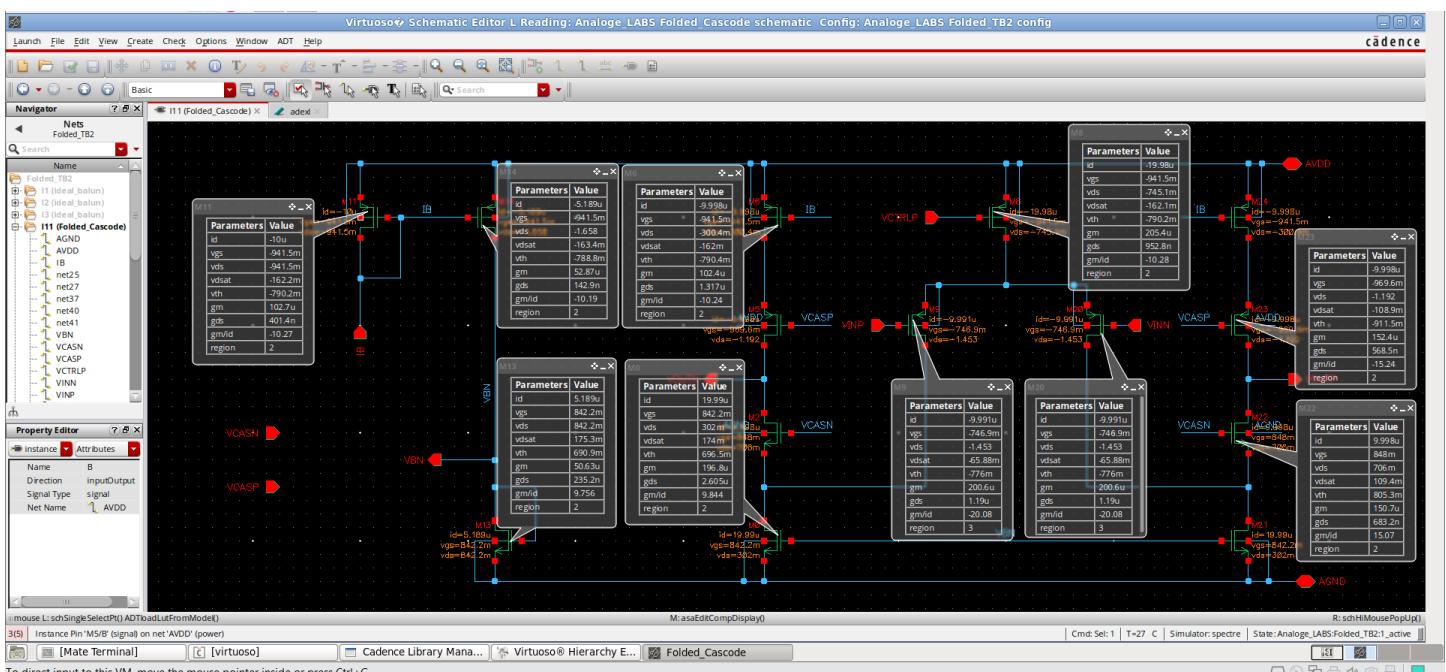
Report the following:

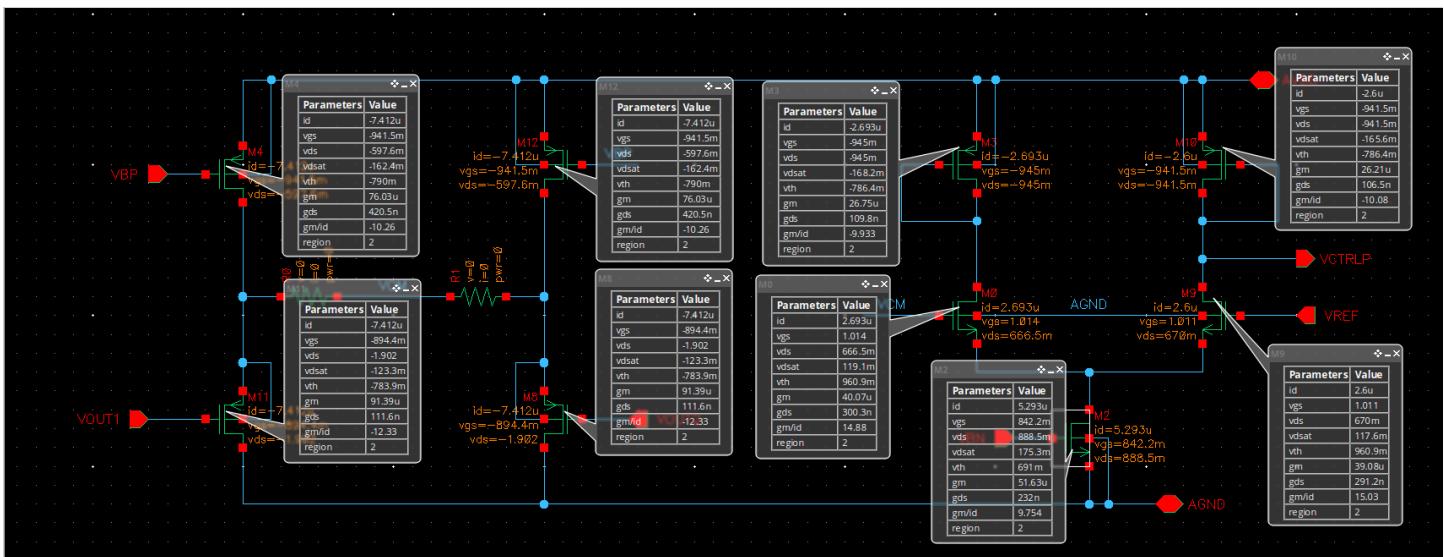
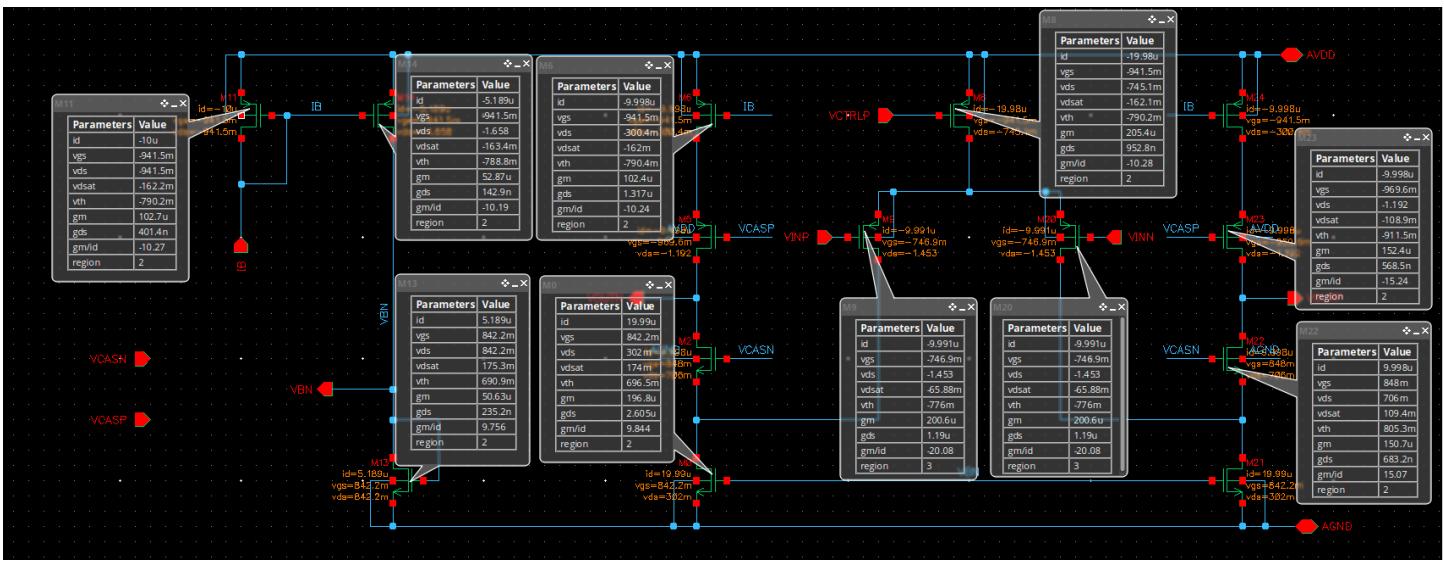
- Schematic of the OTA and the CMFB circuit with DC OP point clearly annotated in closed-loop configuration.





After increasing (gm/id)1:

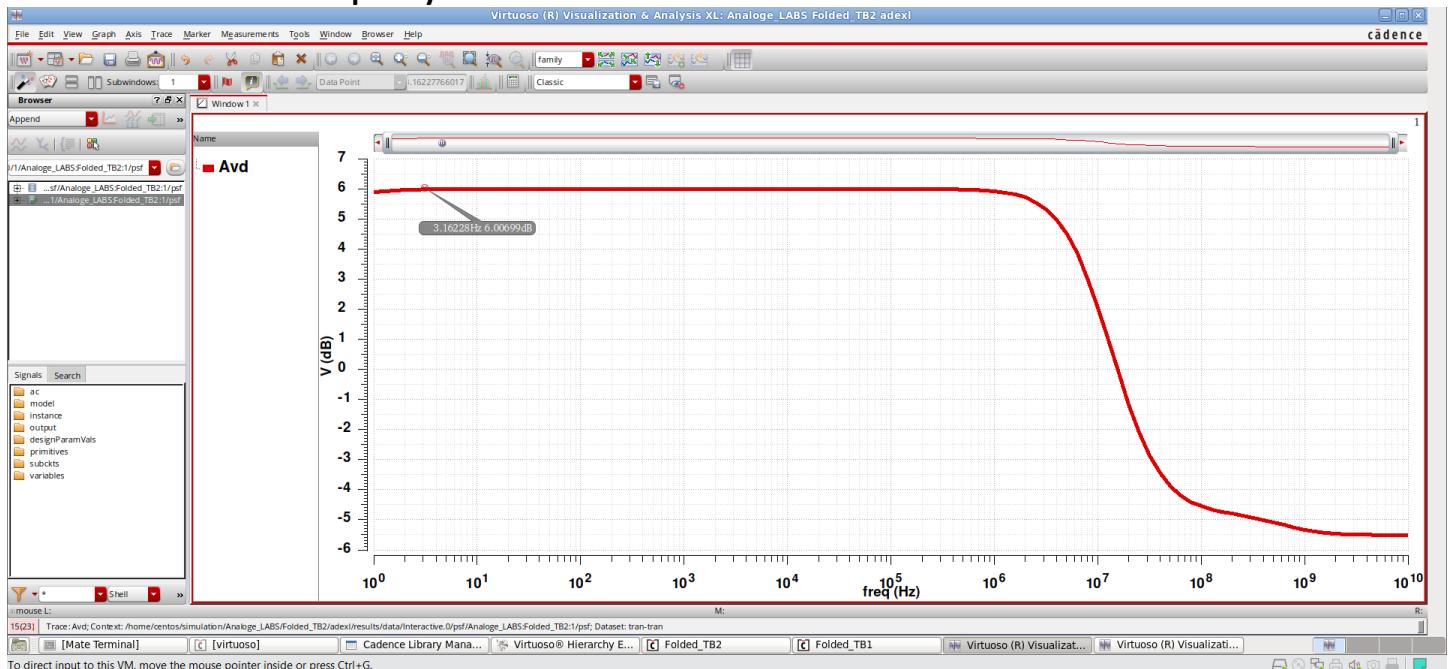




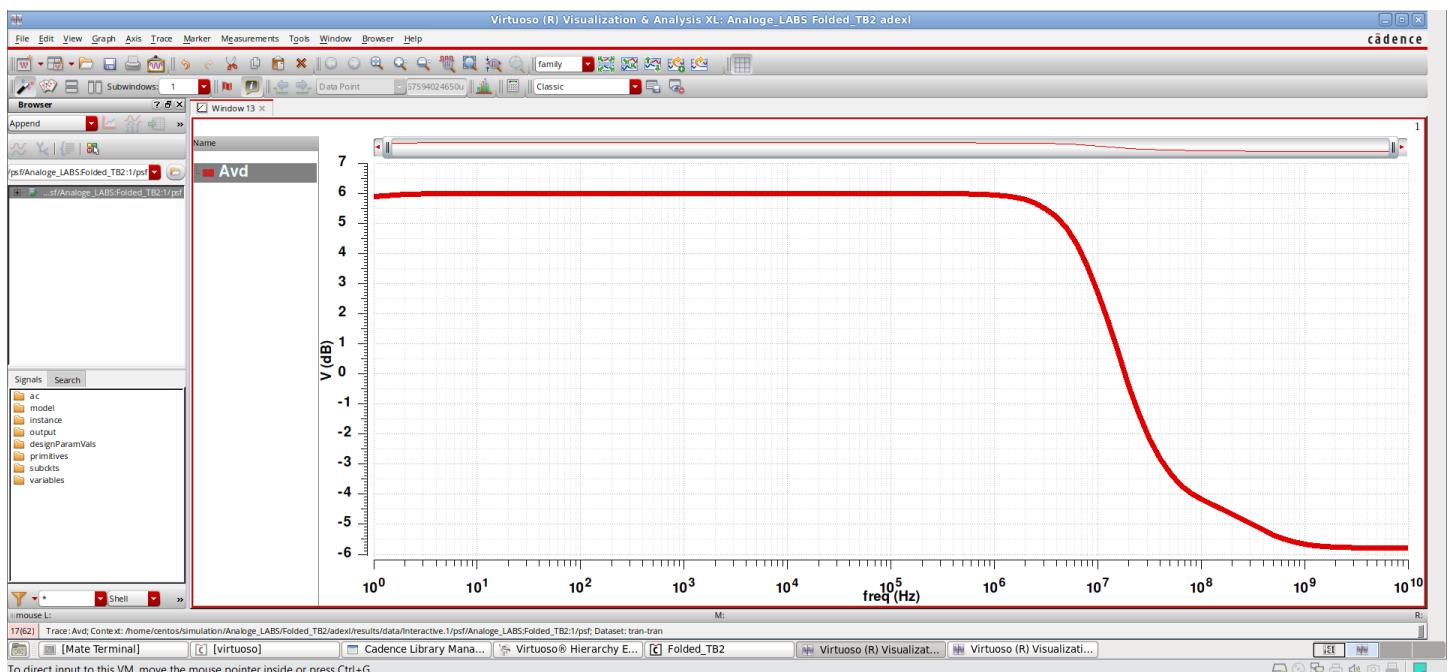
- What is the CM level at the OTA output? Why?
- $V_{out} = V_{DS3} + V_{DS2} = 706m + 302m = 1.008V$, we set $V_{ref} = V_{OCM} + |V_{GS1}| = 1 + .9V$, so that we expect $V_{OCM} = 1V$, but due to finite LG of CM Feedback $V_{OCM} = 1.008V$.
- What is the CM level at the OTA input? Why?
- $V_{IN} = V_{DD} - V_{DS6} - V_{GS1} = 2.5 - 745.1m - 746.9m = 1.008V$, due to the large feedback resistance V_{ICM} is exact equal to V_{OCM} .

2) Differential closed-loop response:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VIDAC = 1 and VICMAC = 0.
- Plot VODIFF vs frequency



After increasing (gm/id)1:



- Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW)

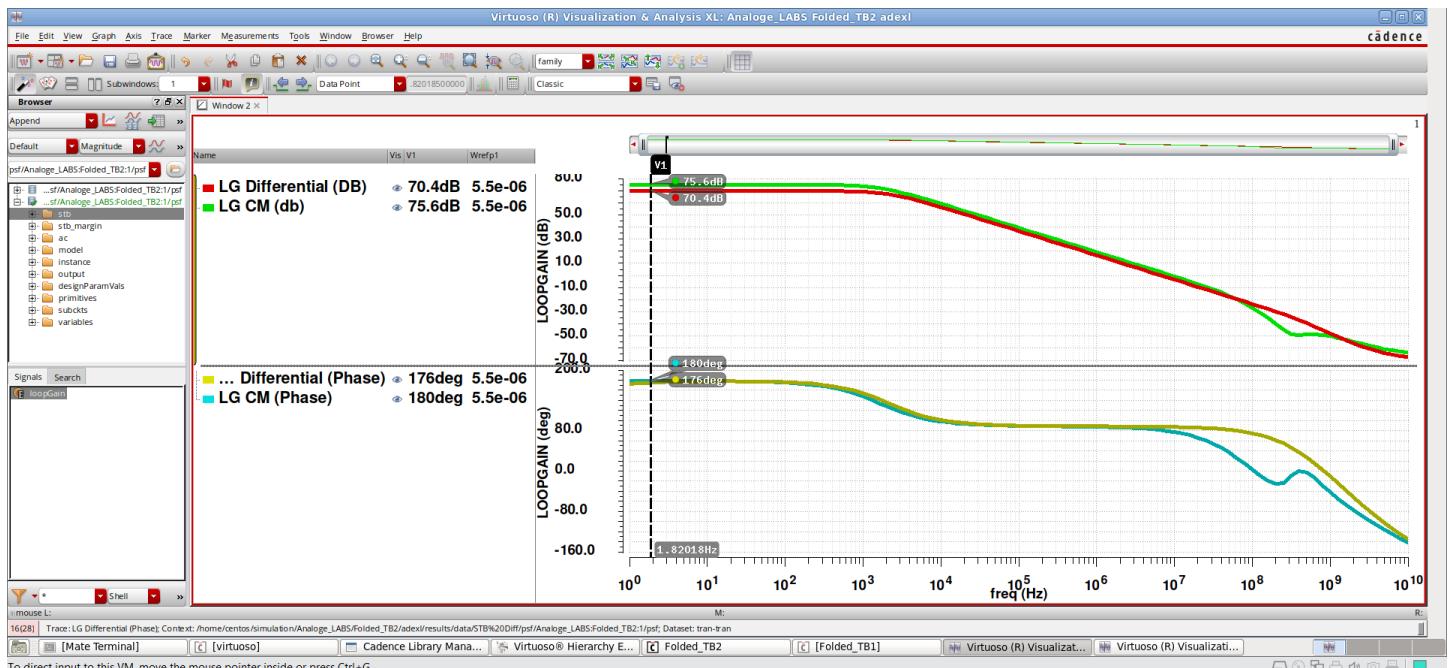
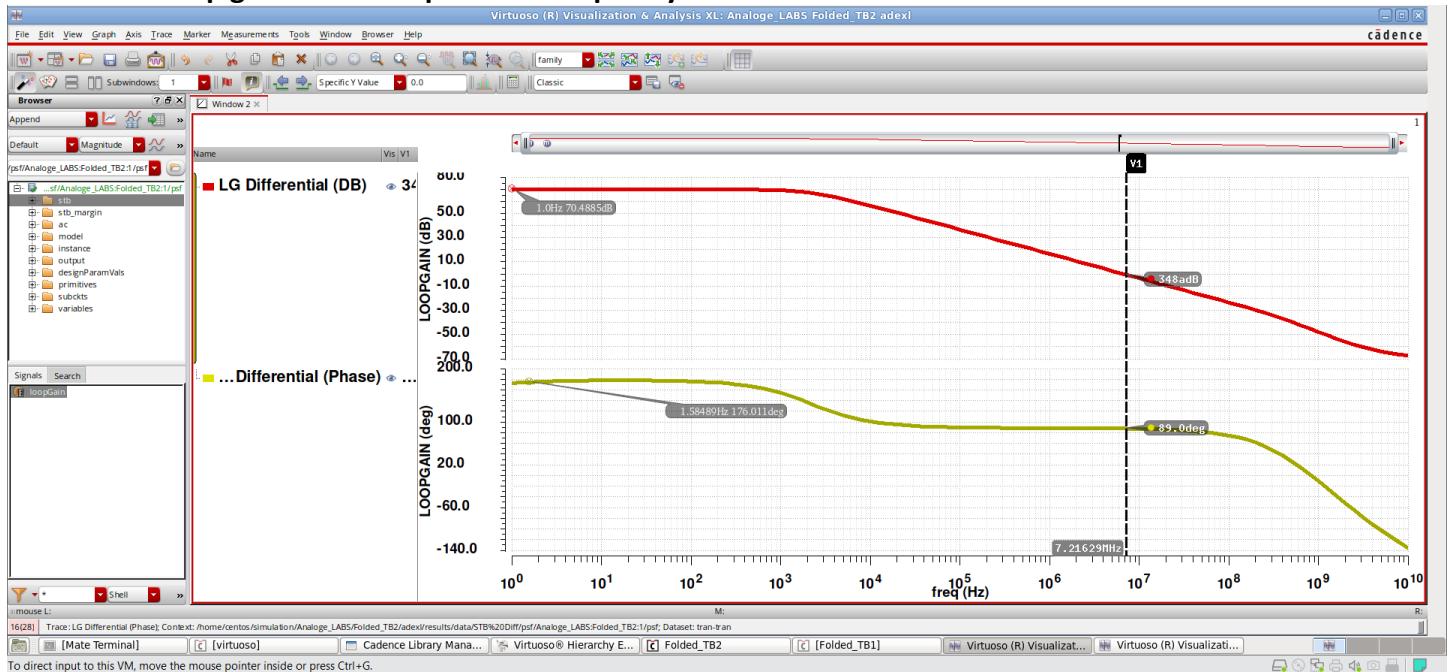
Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB2:1	Ao	1.999			
Analoge_LABS:Folded_TB2:1	Ao_db	6.018			
Analoge_LABS:Folded_TB2:1	BW	8.23M			
Analoge_LABS:Folded_TB2:1	GBW	16.3M			
Analoge_LABS:Folded_TB2:1	Fu	15.56M			

After increasing (gm/id)1:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB2:1	Ao	1.999			
Analoge_LABS:Folded_TB2:1	Ao_db	6.018			
Analoge_LABS:Folded_TB2:1	BW	9.595M			
Analoge_LABS:Folded_TB2:1	GBW	18.99M			
Analoge_LABS:Folded_TB2:1	FU	18.57M			
Analoge_LABS:Folded_TB2:1	PM	eval err			

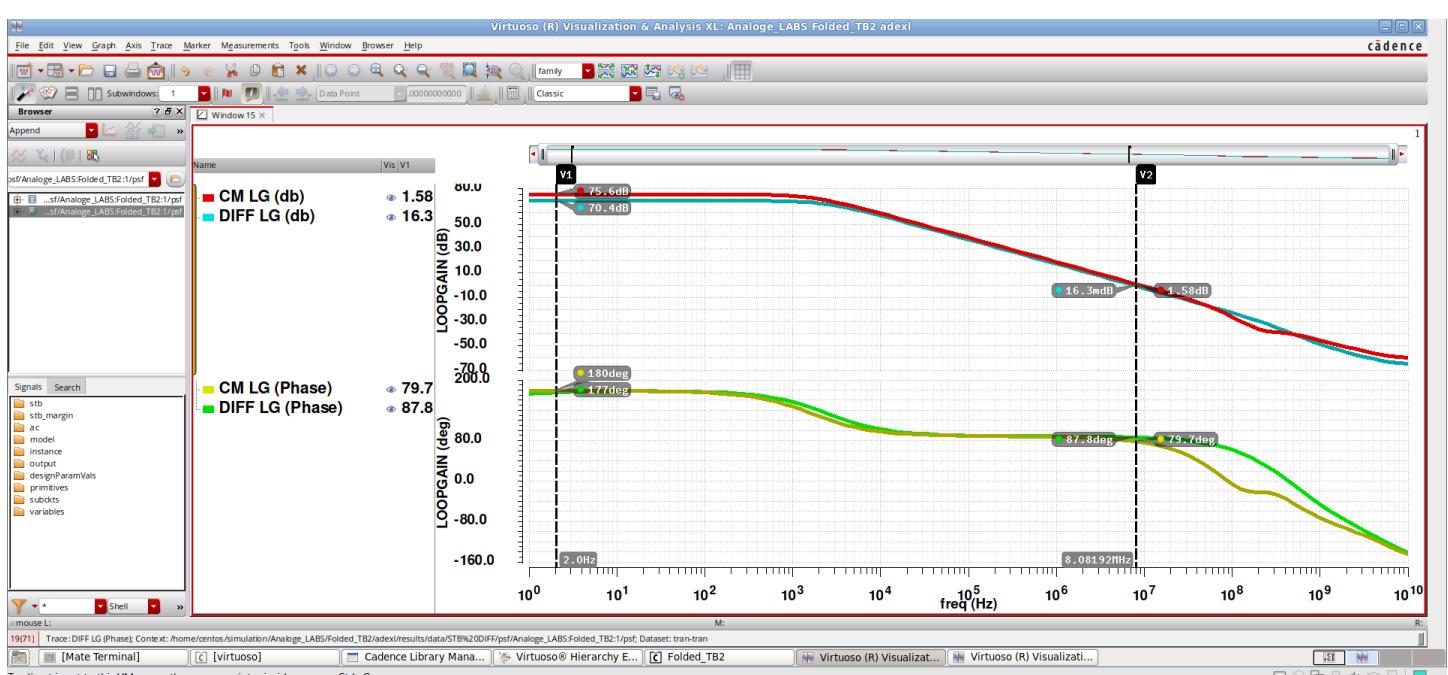
3) Differential and CMFB loops stability (STB analysis):

- Run STB analysis (in addition to AC analysis 1Hz:10Gz, logarithmic, 10 points/decade) two times: first using the OV source in the diff path, and second using the OV source in the CM path.
- Plot loop gain in dB and phase vs frequency for the two simulations overlaid.



Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB2:1	PM	89			
Analoge_LABS:Folded_TB2:1	GBW	7.107M			
Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB2:1	PM	78.97			
Analoge_LABS:Folded_TB2:1	GBW	9.803M			

After increasing (gm/id)1:



Differential

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB2:1	PM	87.82			
Analoge_LABS:Folded_TB2:1	GBW	8.003M			

CM

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB2:1	PM	77.76			
Analoge_LABS:Folded_TB2:1	GBW	9.745M			

- Compare GBW and PM of diff and CM loops. Comment.

As we see the CM LG is higher than the Differential LG.

$$CM\ LG \cong gm_6 * R_{outcm} * A_{verr} , \quad Diff\ LG \cong gm_1 * R_{outdiff} * \beta$$

As gm_6 almost equal to gm_1 ($ID_6=2*ID_1$, $(gm/id)_1=2(gm/id)_6$) , $R_{outcm} > R_{outdiff}$ (Routcm is degenerated) , $A_{verr} > \beta$, then the CM LG is greater than the Diff LG.

$$GBW_{CM} \approx gm_6 * \frac{A_{verr}}{C_{out}} , \quad GBW_{diff} = gm_1 * \frac{\beta}{C_{out}} , \text{ as } gm_6 \approx gm_1 , \quad A_{verr} > \beta , \text{ then the } GBW_{cm} > GBW_{diff}.$$

- Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation.

	Open Loop	Closed Loop
DC LG	80db	70.4db
GBW	48.56MHz	8.003MHz

Comment

The LG is less than the Differential open loop gain , as $LG = Avd * \beta$ and $\beta < 1$.

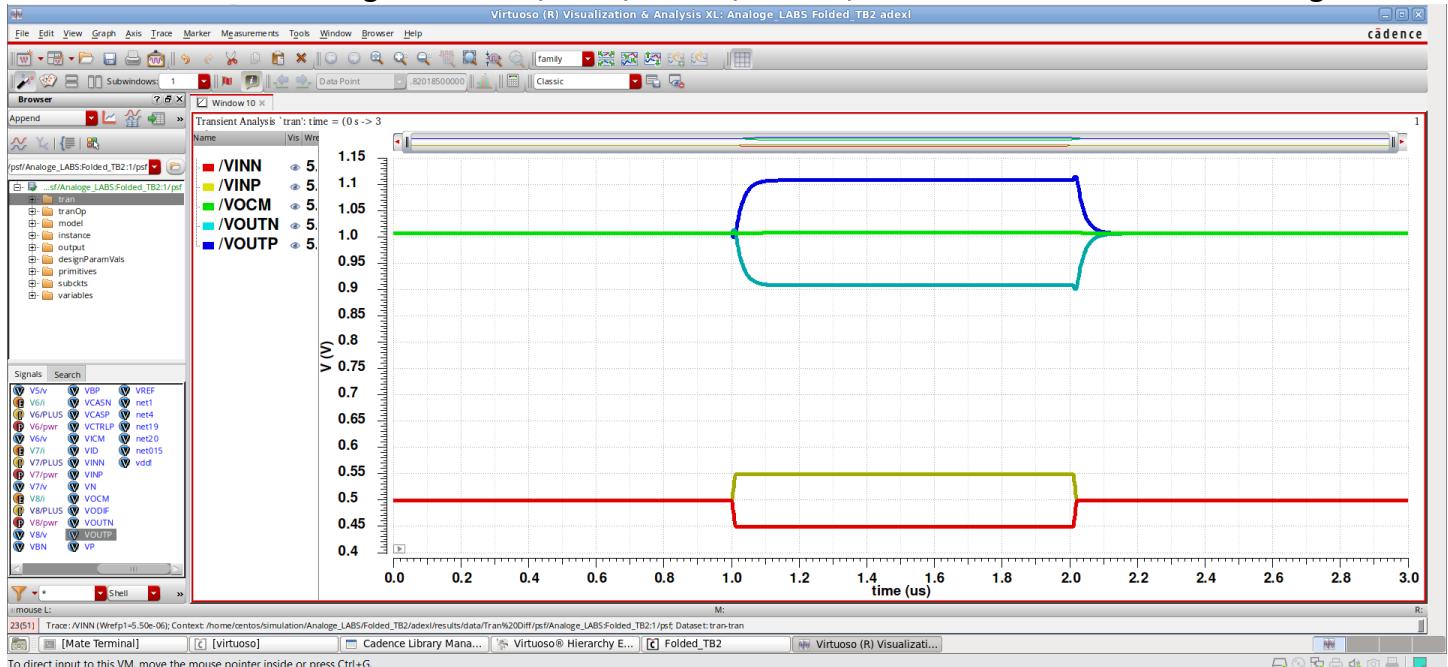
The GBW of LG is less than Differential open loop GBW , as $GBW_{LG} = \beta * GBW_{openloop}$.

PART 6: Closed Loop Simulation (Transient Analysis)

Report the following:

1. Differential and CMFB loops stability (transient analysis) + CL settling time: Differential input pulse

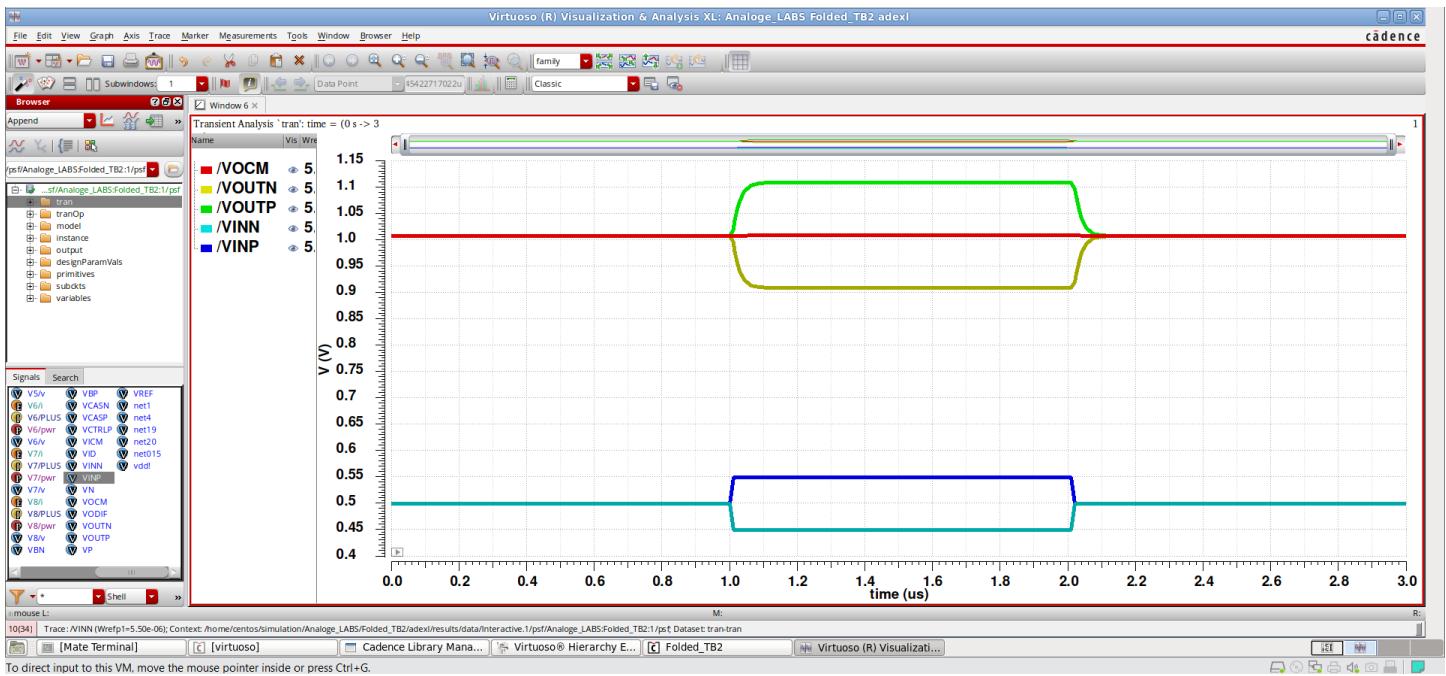
- Apply a differential input pulse (initial value = 0, pulse value = 100mV, delay = 1us, period = 2us, pulse width = 1us, rise = fall = 10ns).
- Run transient analysis for 3us with 10ns max step.
- Plot the transient signals at VINN, VINP, VOCM, VOUTN, and VOUTP overlaid in the same figure.



- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?
- ✓ No ,there is no ringing , that is as the PM=87deg , then the system is overdamped.
- Calculate the 1% settling time and compare it to the required specification. If the specification is not satisfied, what design changes could be a possible solution?

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB2:1	Ts	169.5n			

As we see the settling time is high , so that to achieve the Ts spec I will increase $(gm/id)_1$, I make $(gm/id)_1=20$, I will increase W1 , then $W1=91.64\mu m$.

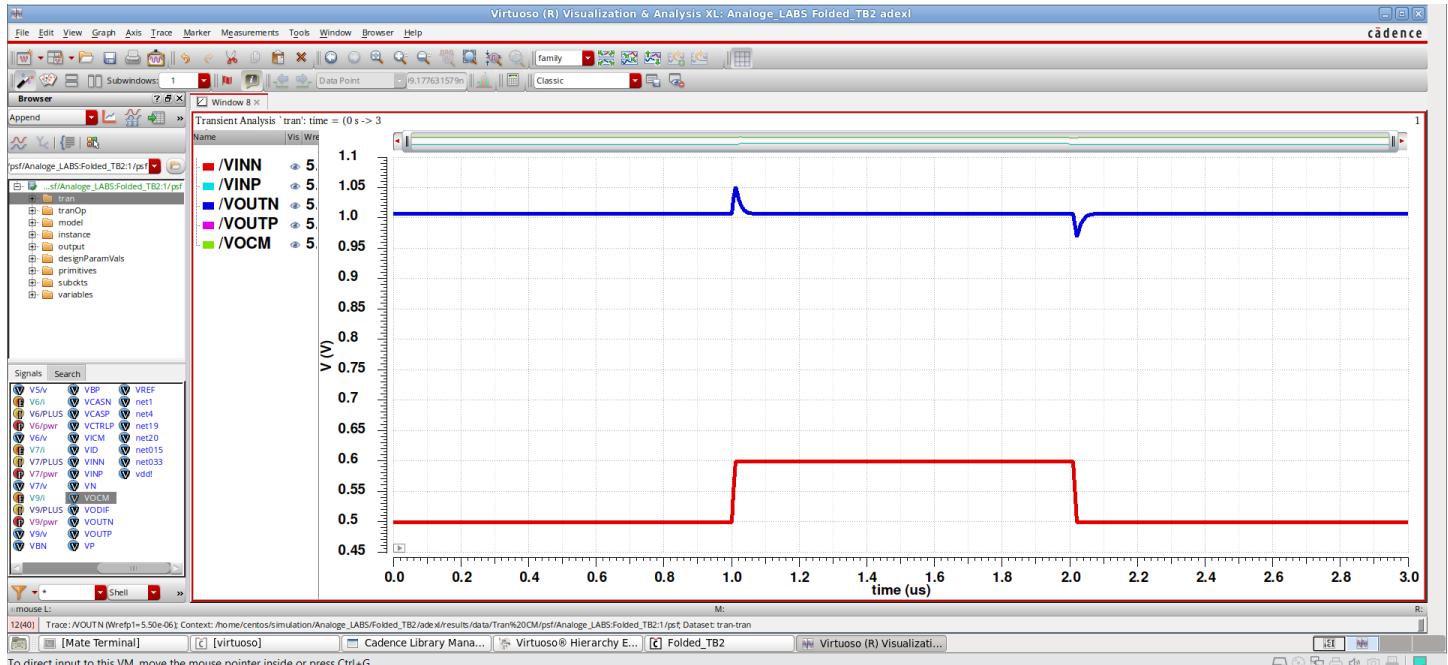


Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB2:1	Ts	94.11n			

As we see the settling time is decreased and now it meet the spec.

2. Differential and CMFB loops stability (transient analysis): CM input pulse

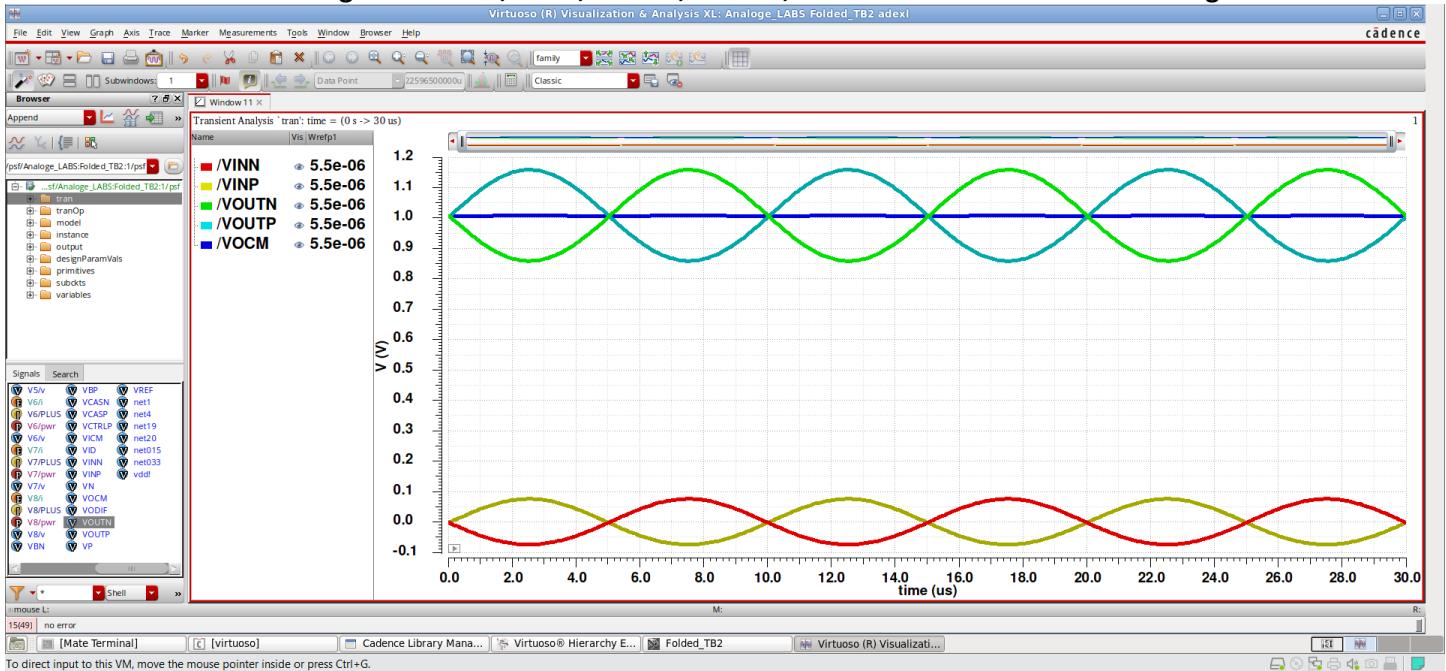
- Set differential input to zero and apply the same previous pulse at the balun CM input.
- Run transient analysis for 3us to test the fully differential capacitive amplifier stability.
- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



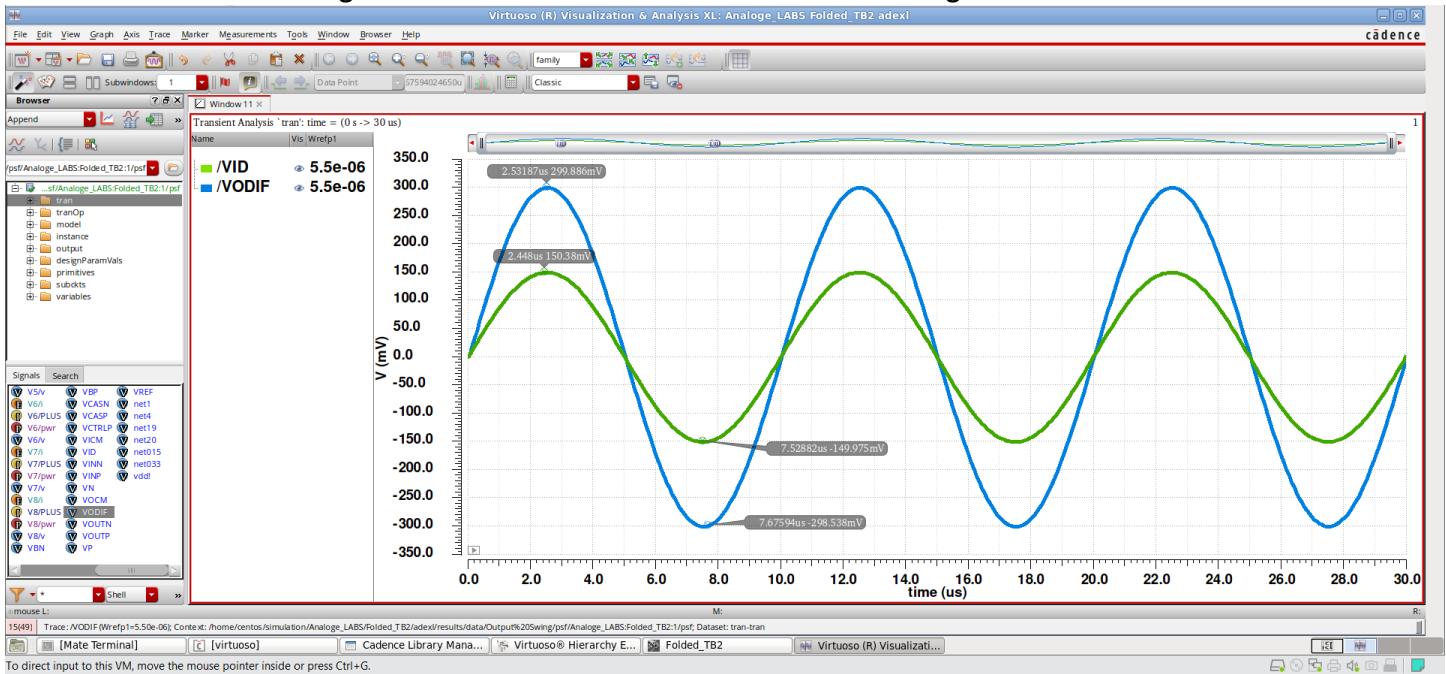
- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?
- ✓ No ,there is no ringing as PM=77 deg then the system is overdamped.

3. Output swing:

- Apply a differential sinusoidal input with freq = 100kHz and amplitude = 150mV.
- Run transient analysis for three periods (30us) with 0.1us max time step.
- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



- Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.



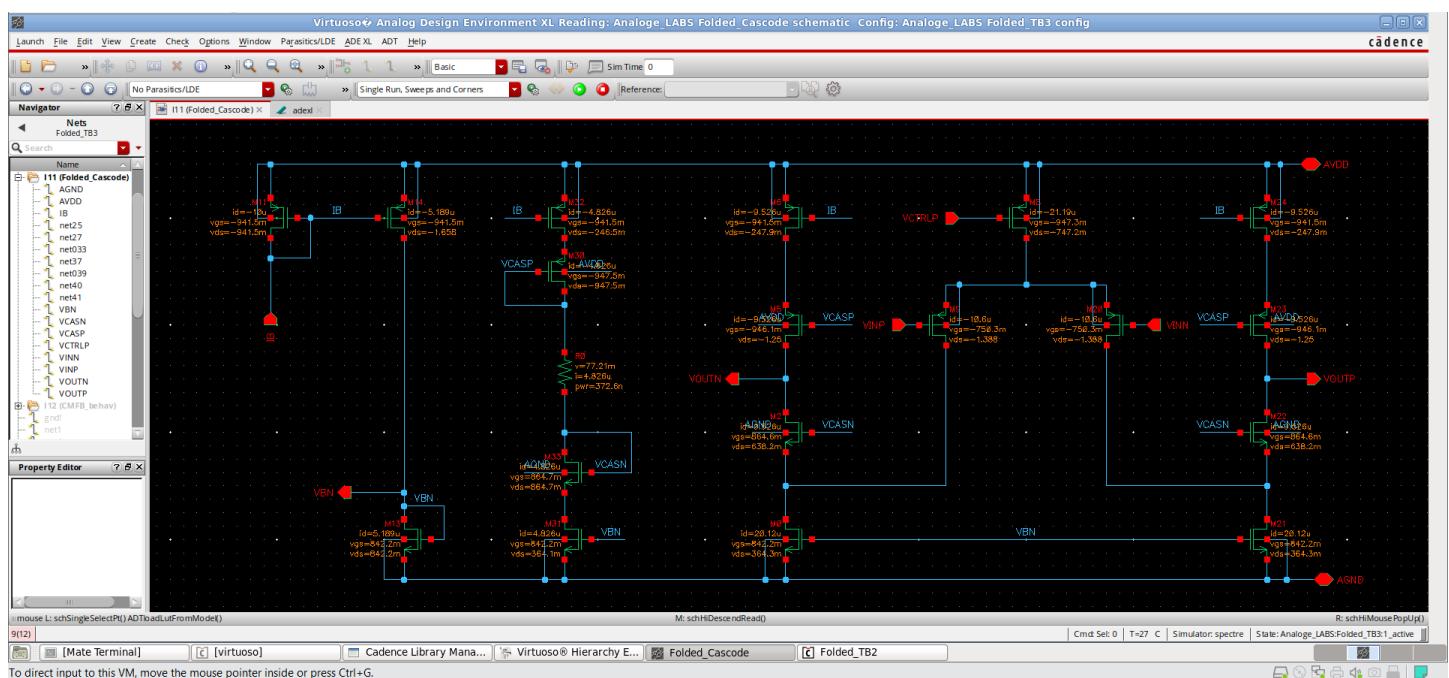
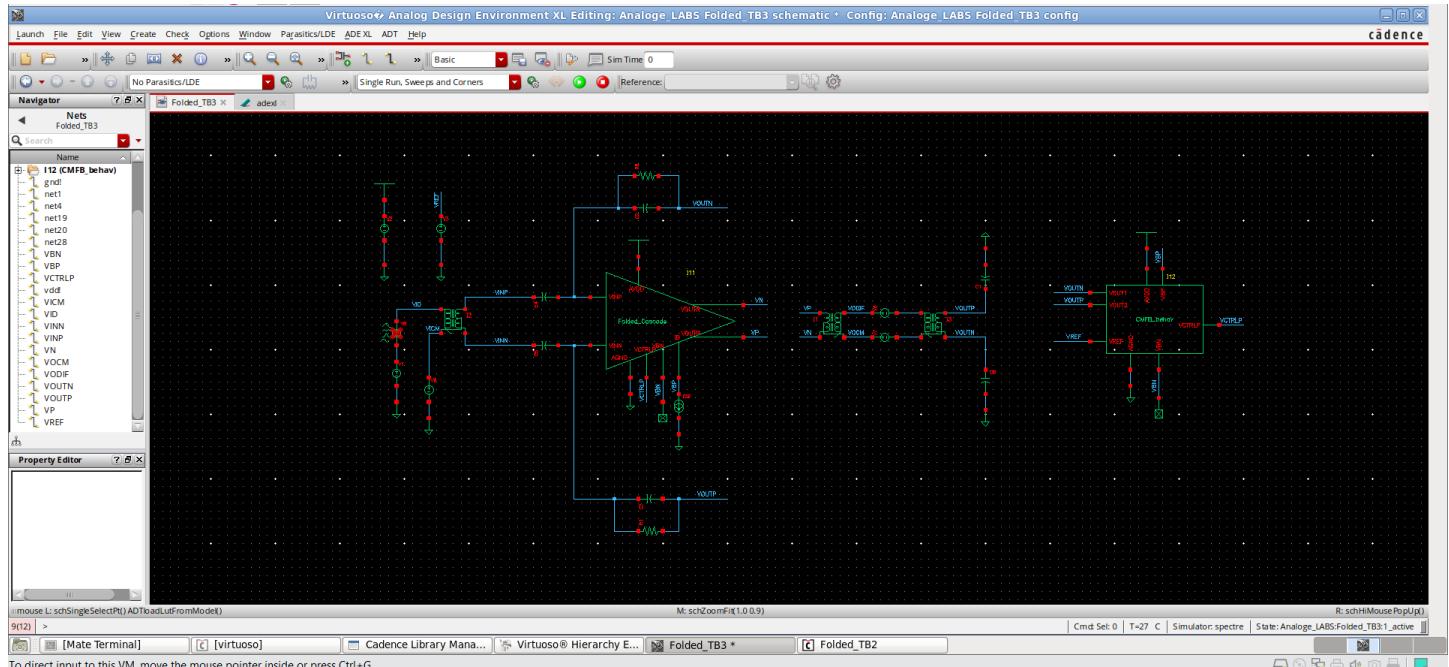
- Calculate the diff input and output peak-to-peak swings and the closed loop gain.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB2:1	peakToPeak(VT("/VODIF"))	599.8m			
Analoge_LABS:Folded_TB2:1	peakToPeak(VT("/VID"))	300m			

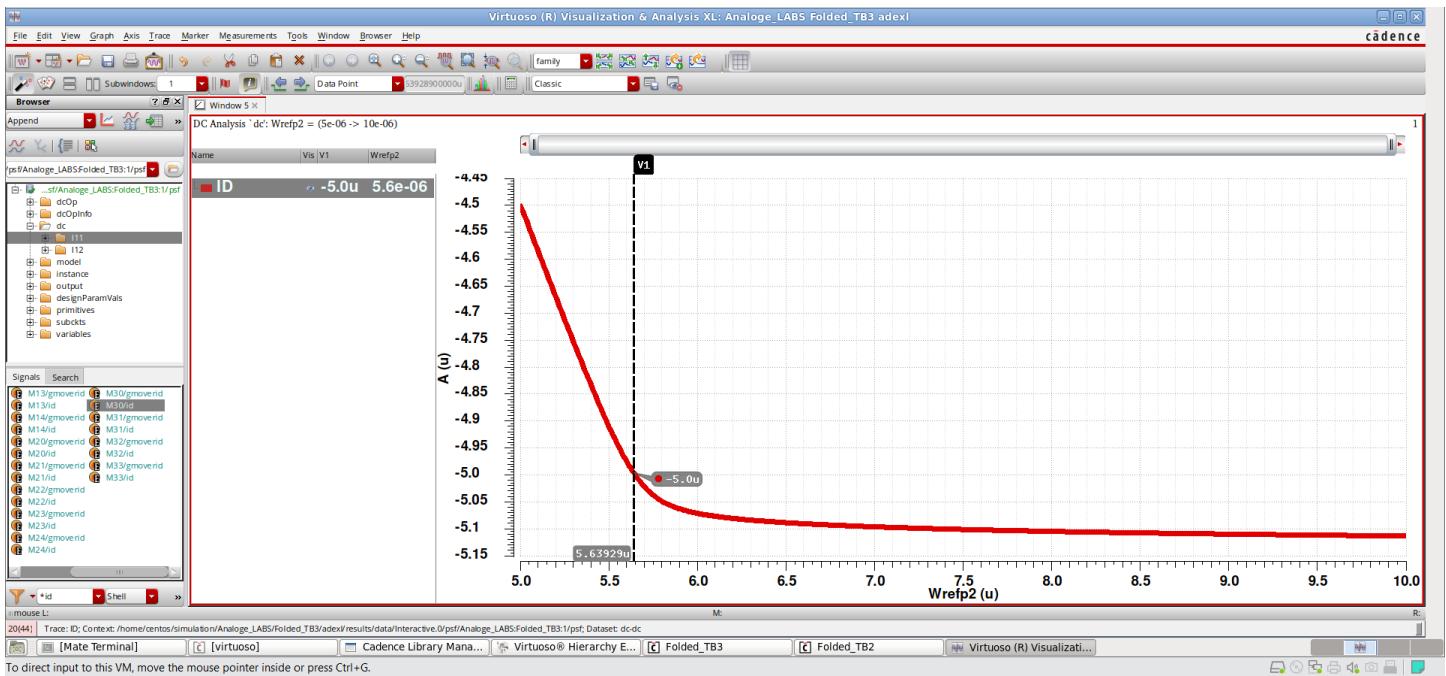
$$A_{vcl} = \frac{V_{oppk}}{V_{inppk}} = \frac{599.8m}{300m} = 1.999 \nu / \nu.$$

PART 5: Closed Loop Simulation (AC and STB Analysis)

Create a new testbench with the OTA connected in closed-loop feedback configuration using capacitive feedback as shown below. Note that the CM DC level provided before the input balun is useless because it is blocked by the capacitor.

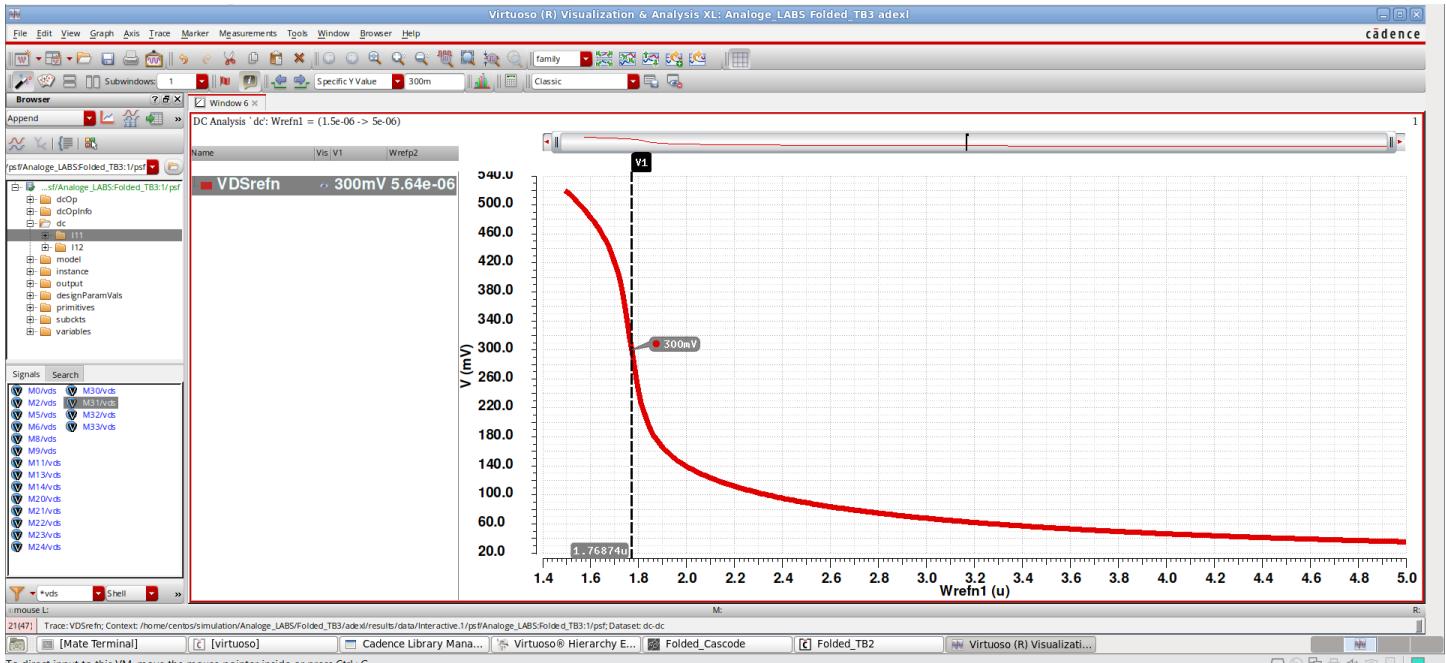


as we see Vcasn is higher than the designed value and the current in the bias branch is less than the required ,so I will sweep Wrefp1 and Wrefpn to fix the current and Vcasn and Vcasp.



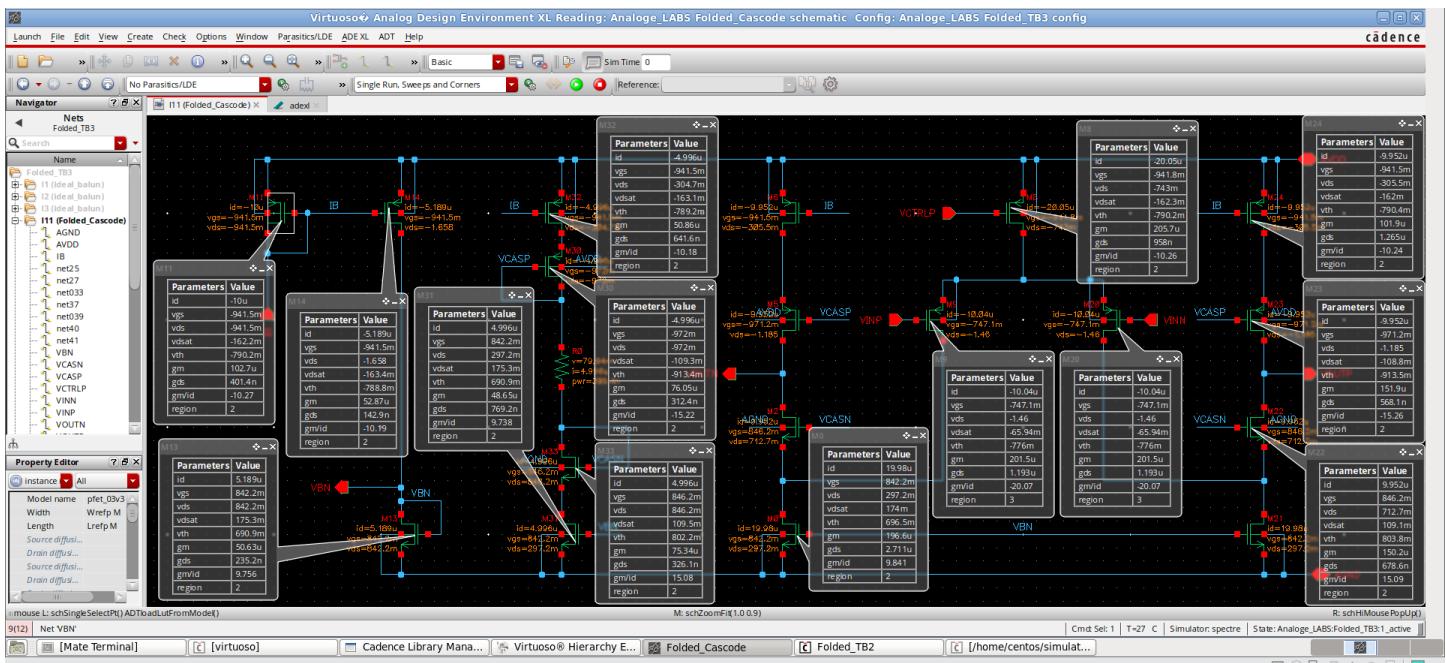
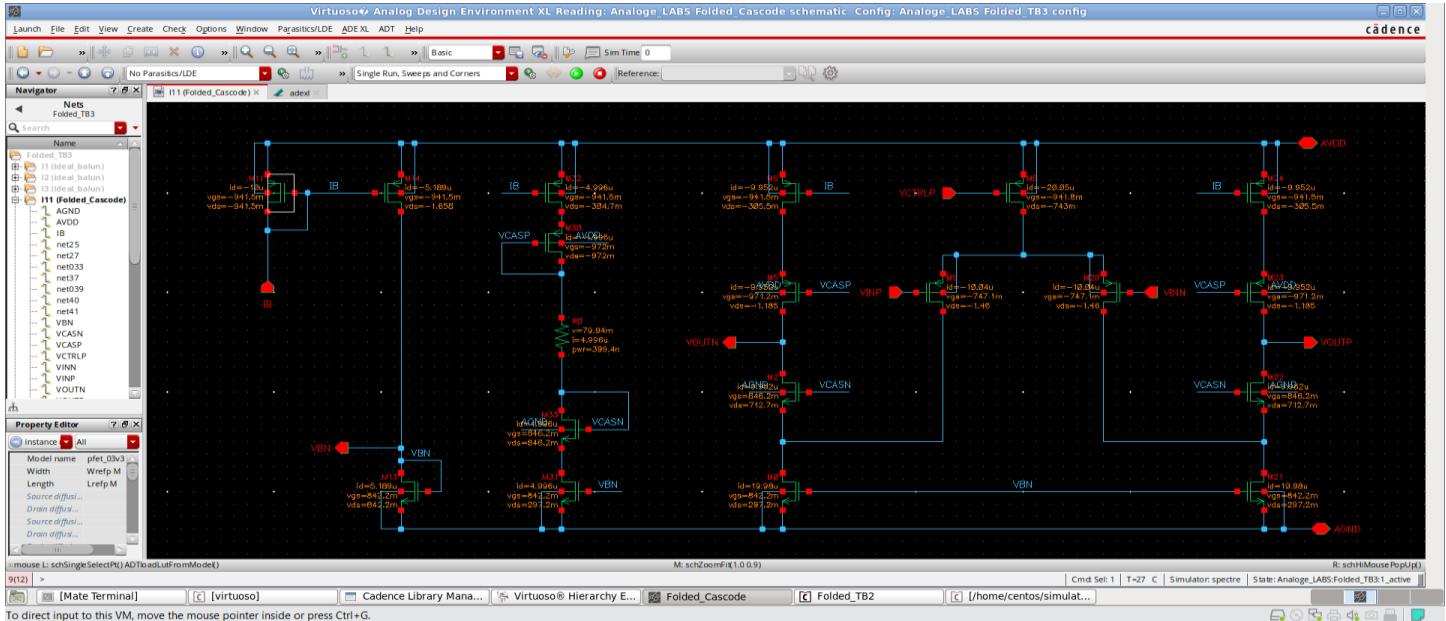
Wrefp2=5.64um.

As W5 has the same VGS and VDS as Wrefp2 , so to Set the current ID5=10uA(double the current IDrefn1) , then W5 must equal W5=2*Wrefp2=11.28uA.

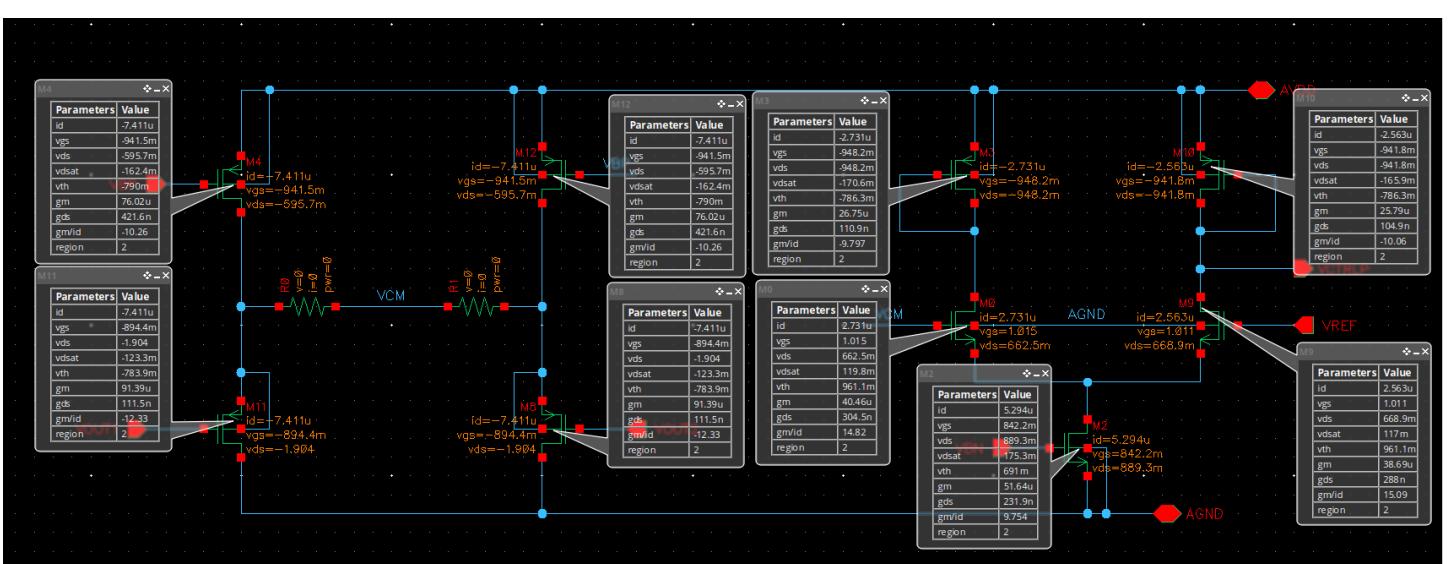
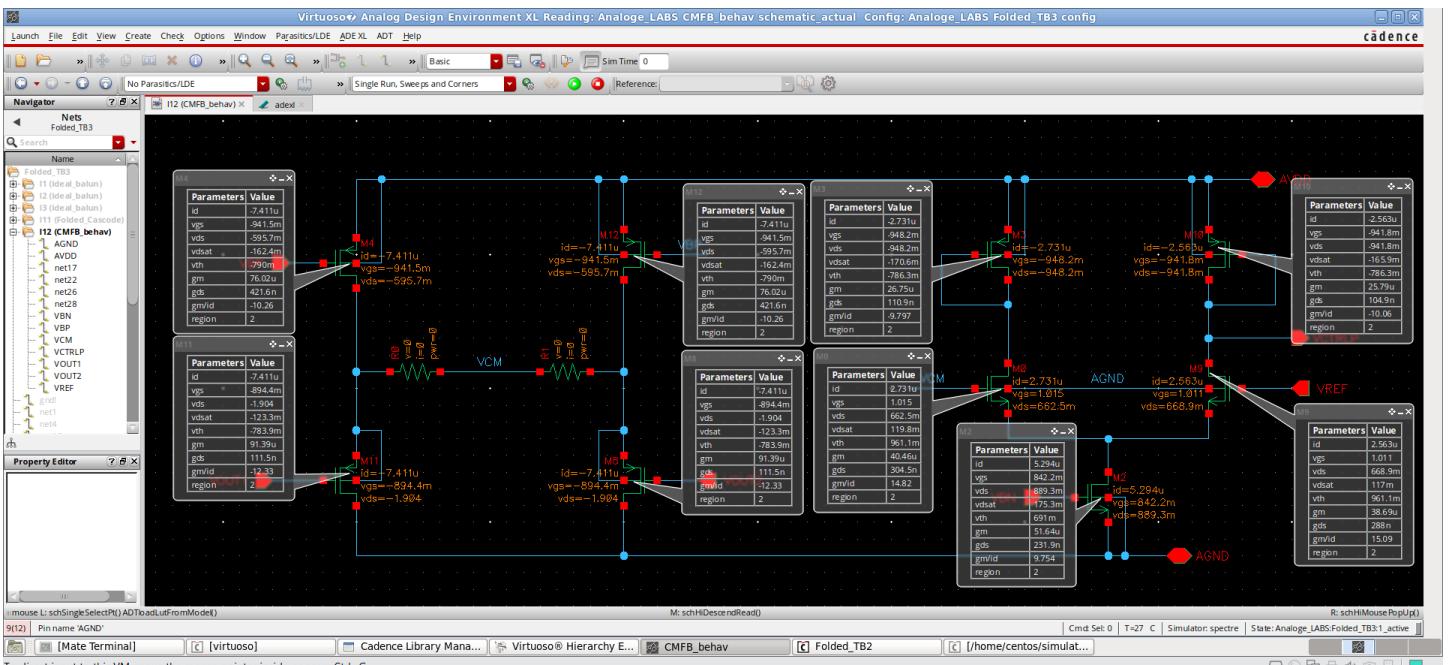
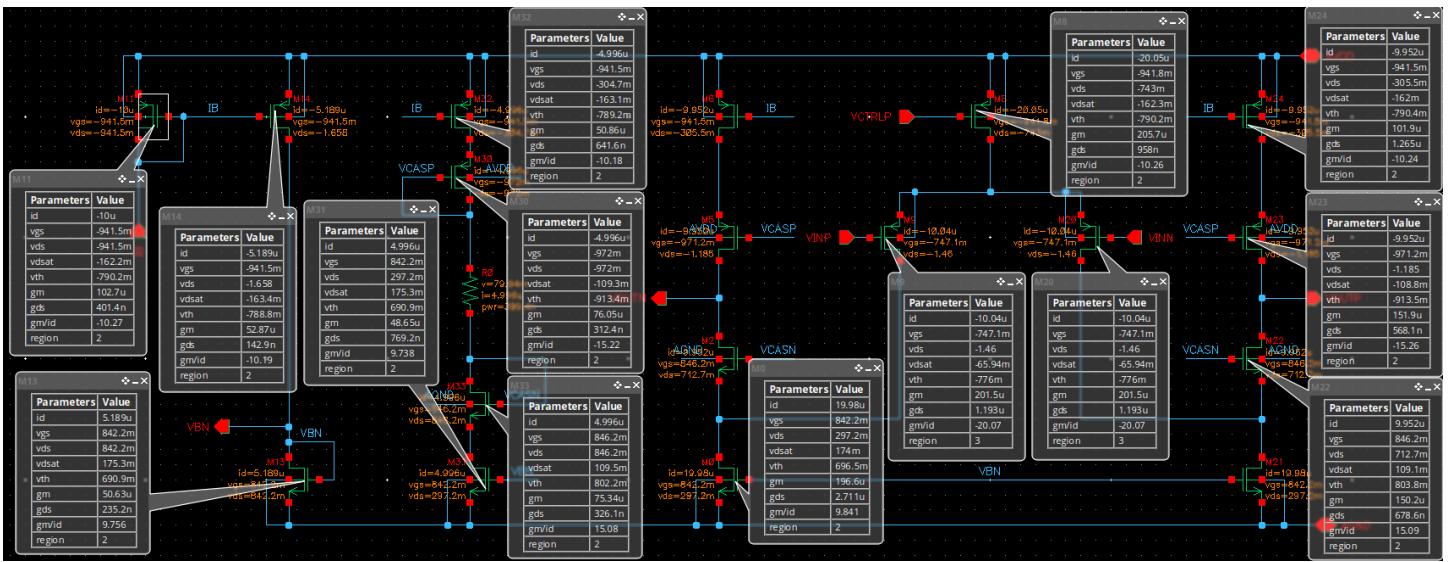


Wrefn1=1.77um.

Report the following:

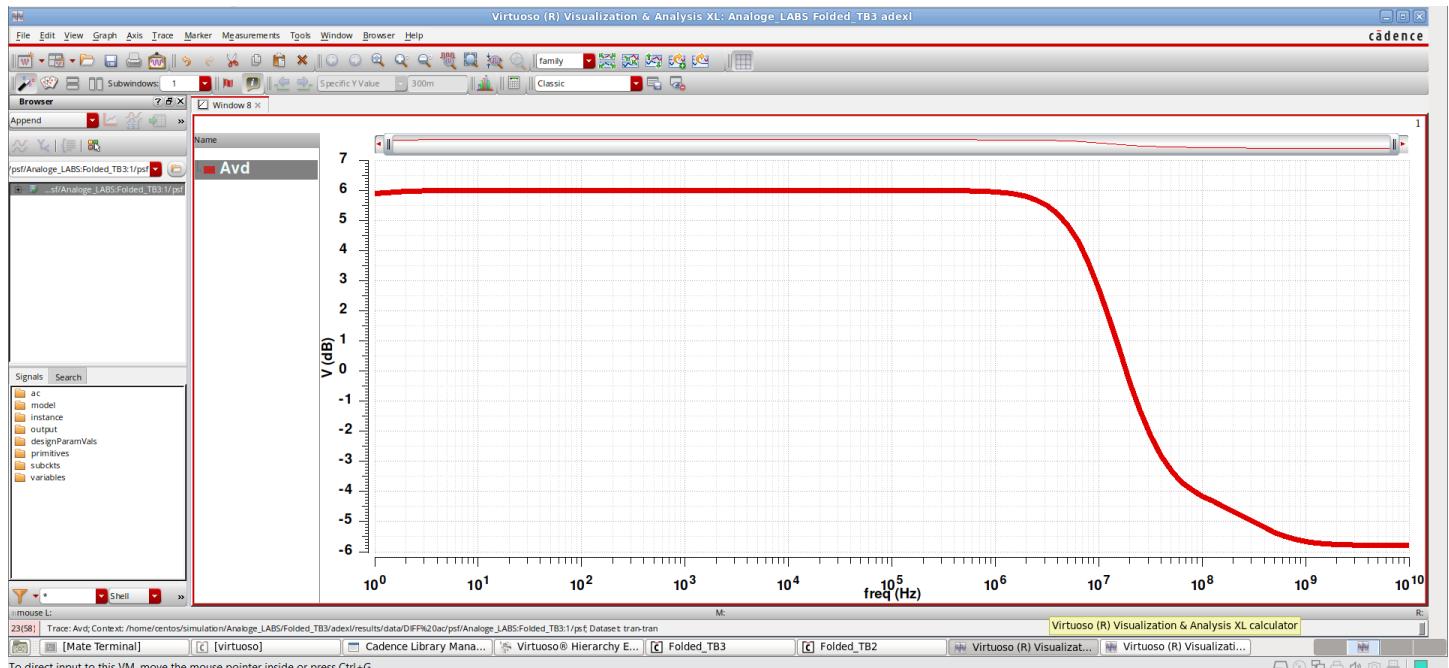


- What is the CM level at the OTA output? Why?
- ✓ $V_{out} = V_{DS3} + V_{DS2} = 712.7m + 297.2m = 1.0099V$.
- What is the CM level at the OTA input? Why?
- ✓ $V_{IN} = V_{DD} - V_{DS6} - V_{GS1} = 2.5 - 743m - 747.1m = 1.0099V$.



1) Differential closed-loop response:

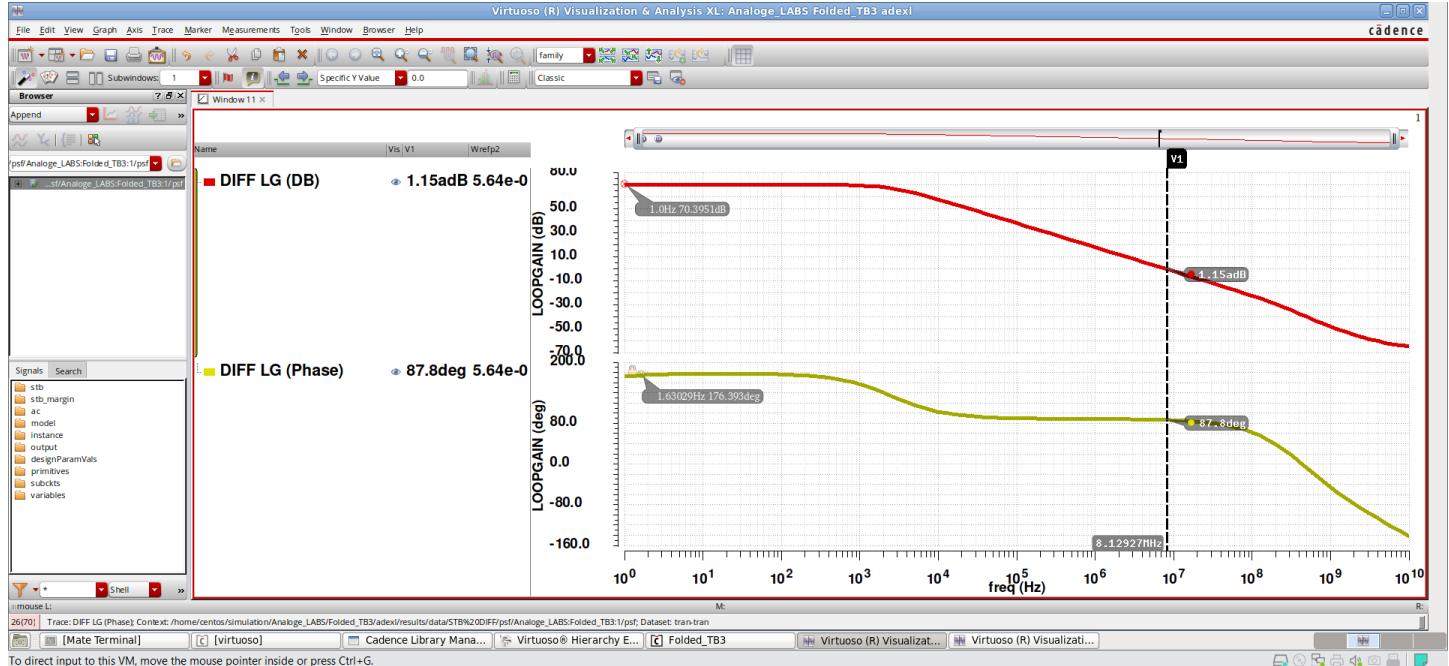
- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VIDAC = 1 and VICMAC = 0.
- Plot VODIFF vs frequency



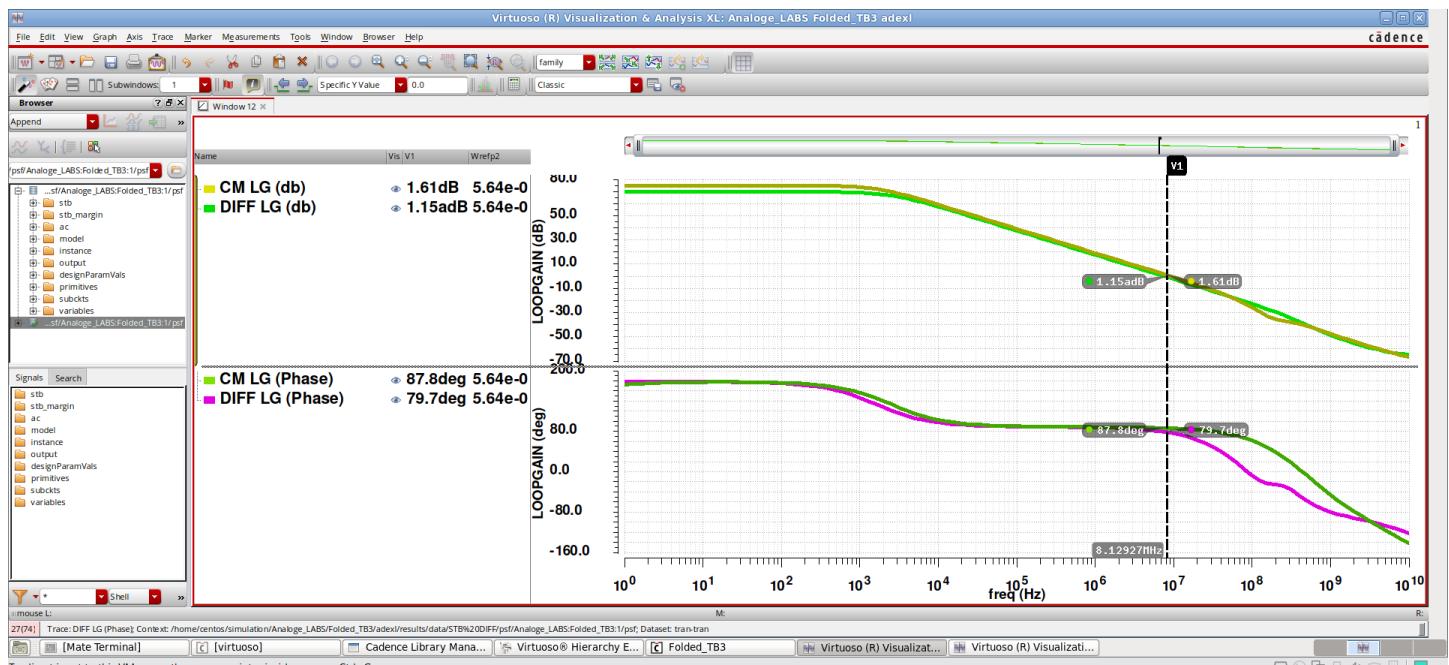
Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB3:1	Ao	1.999			
Analoge_LABS:Folded_TB3:1	Ao_db	6.018			
Analoge_LABS:Folded_TB3:1	BW	9.628M			
Analoge_LABS:Folded_TB3:1	Fu	18.64M			
Analoge_LABS:Folded_TB3:1	GBW	19.06M			

4) Differential and CMFB loops stability (STB analysis):

- Run STB analysis (in addition to AC analysis 1Hz:10Gz, logarithmic, 10 points/decade) two times: first using the OV source in the diff path, and second using the OV source in the CM path.
- Plot loop gain in dB and phase vs frequency for the two simulations overlaid.
- Compare GBW and PM of diff and CM loops. Comment.



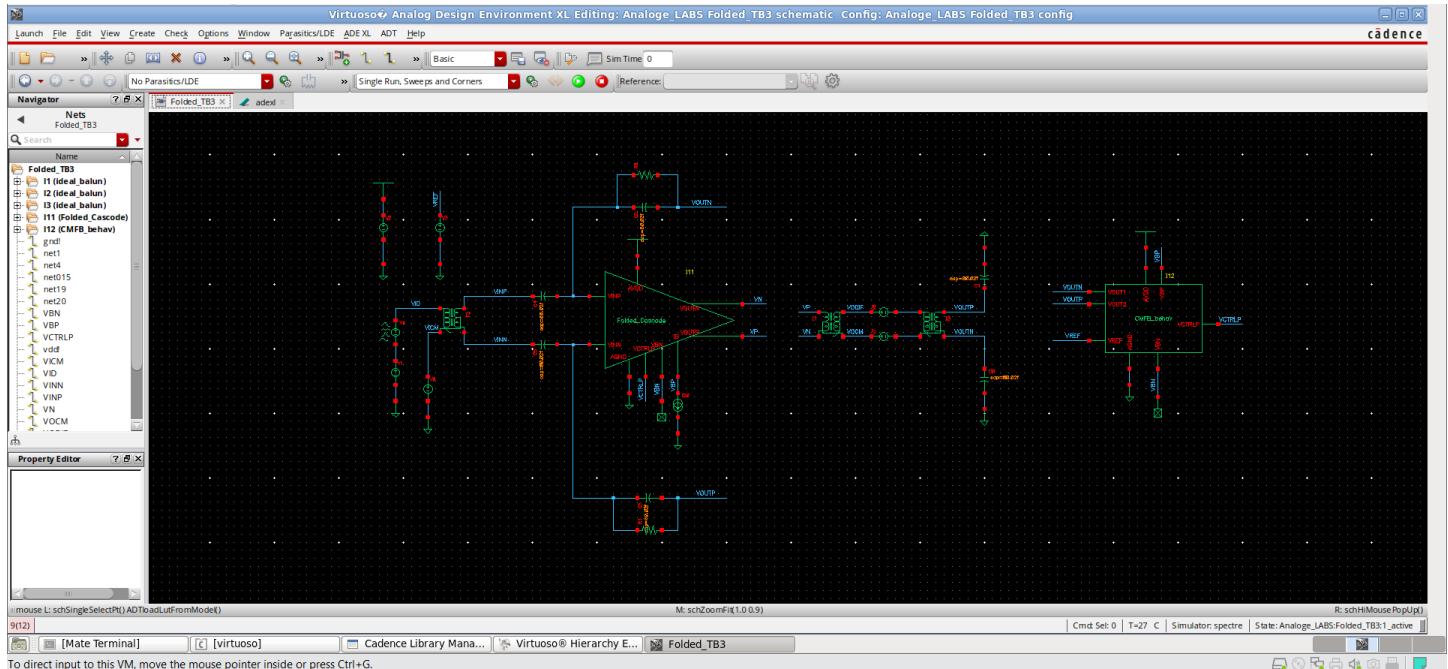
Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB3:1	PM	87.81			
Analoge_LABS:Folded_TB3:1	GBW	8.028M			



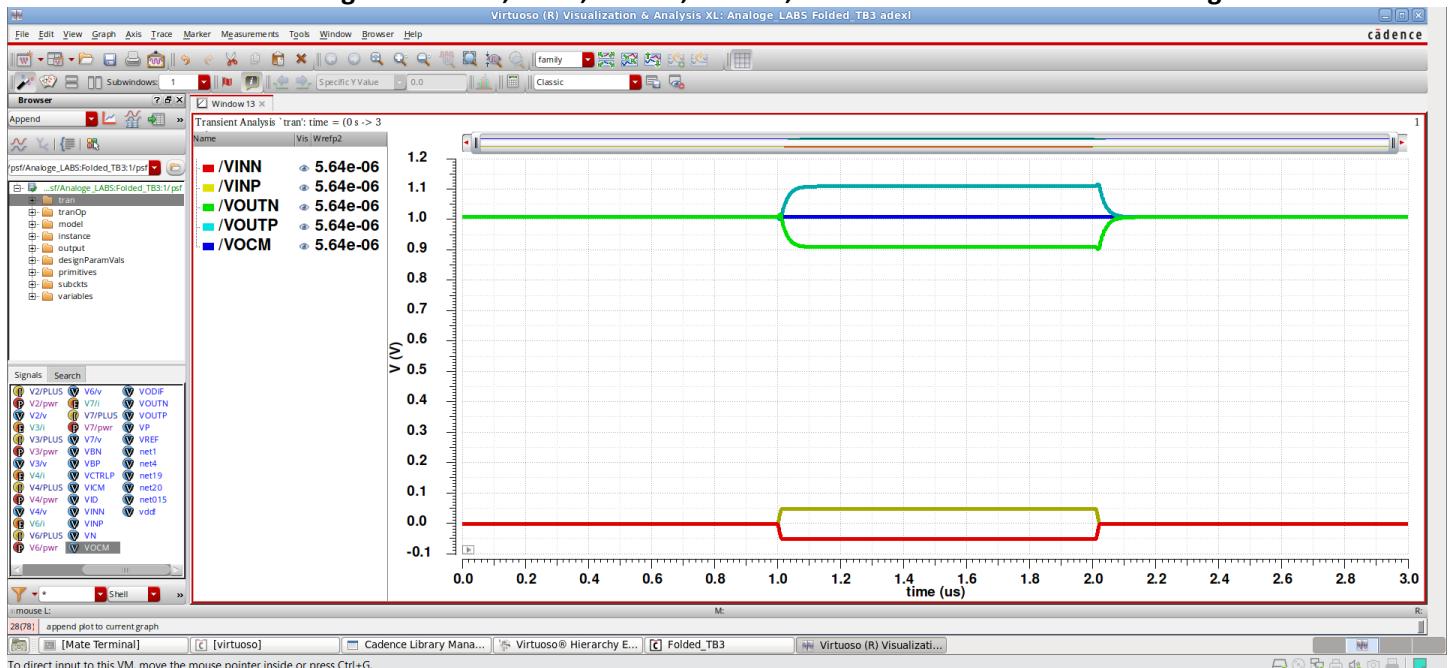
Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB3:1	PM	77.57			
Analoge_LABS:Folded_TB3:1	GBW	9.632M			

PART 6: Closed Loop Simulation (Transient Analysis)

1) Differential and CMFB loops stability (transient analysis) + CL settling time: Differential input pulse



- Apply a differential input pulse (initial value = 0, pulse value = 100mV, delay = 1us, period = 2us, pulse width = 1us, rise = fall = 10ns).
- Run transient analysis for 3us with 10ns max step.
- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

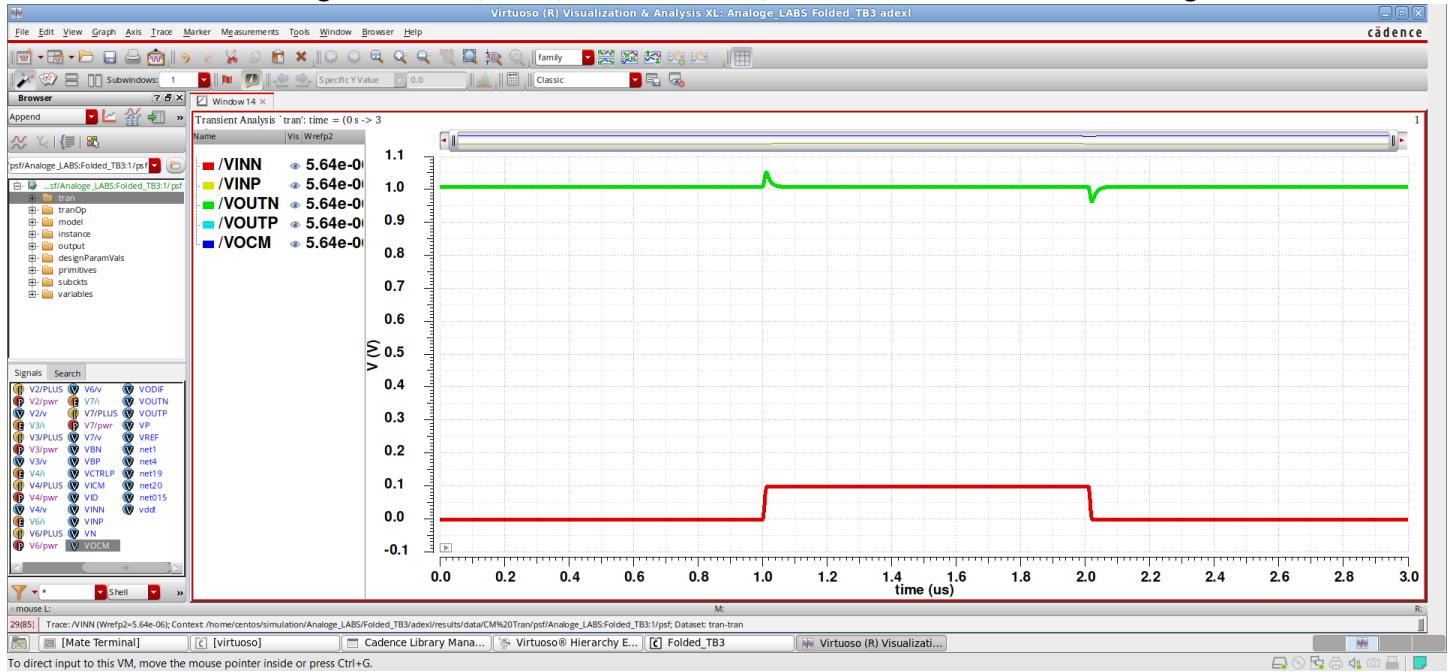


- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?
- Calculate the 1% settling time and compare it to the required specification. If the specification is not satisfied, what design changes could be a possible solution?

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analogue_LABS:Folded_TB3:1	TS	87.24 n			

2) Differential and CMFB loops stability (transient analysis): CM input pulse

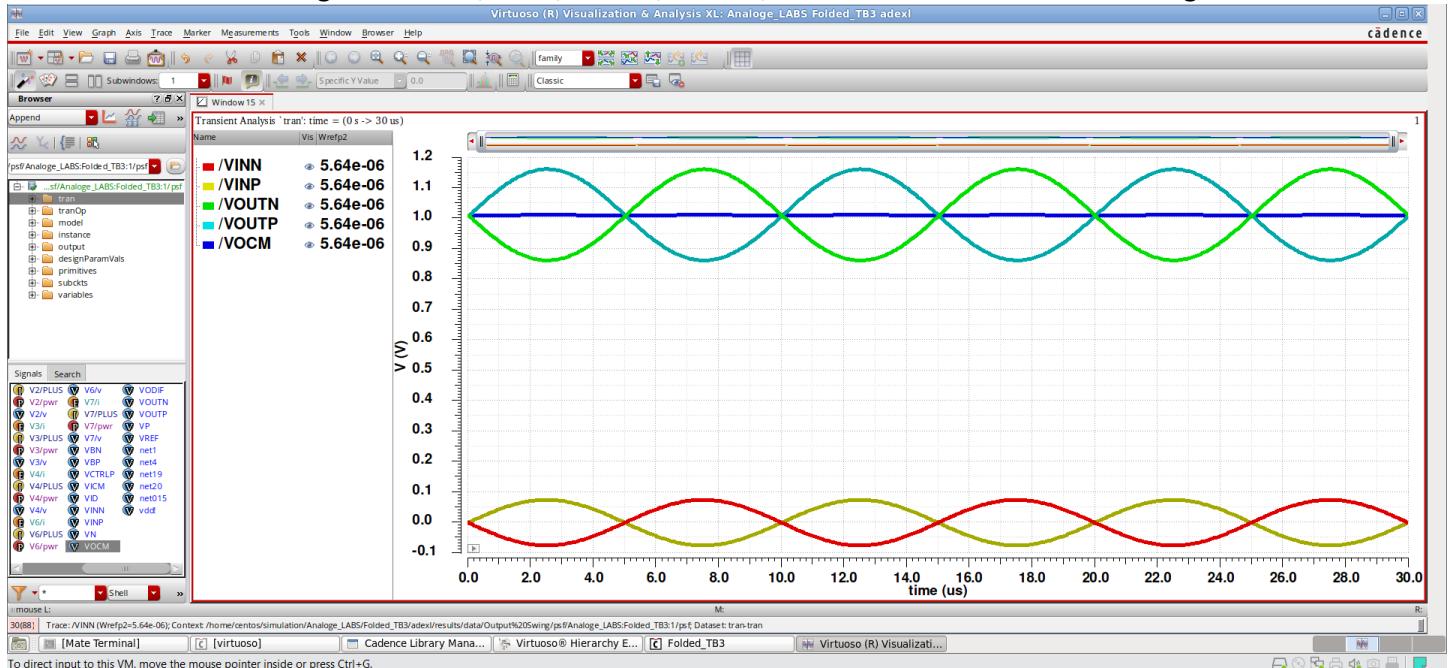
- Set differential input to zero and apply the same previous pulse at the balun CM input.
- Run transient analysis for 3us to test the fully differential capacitive amplifier stability.
- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



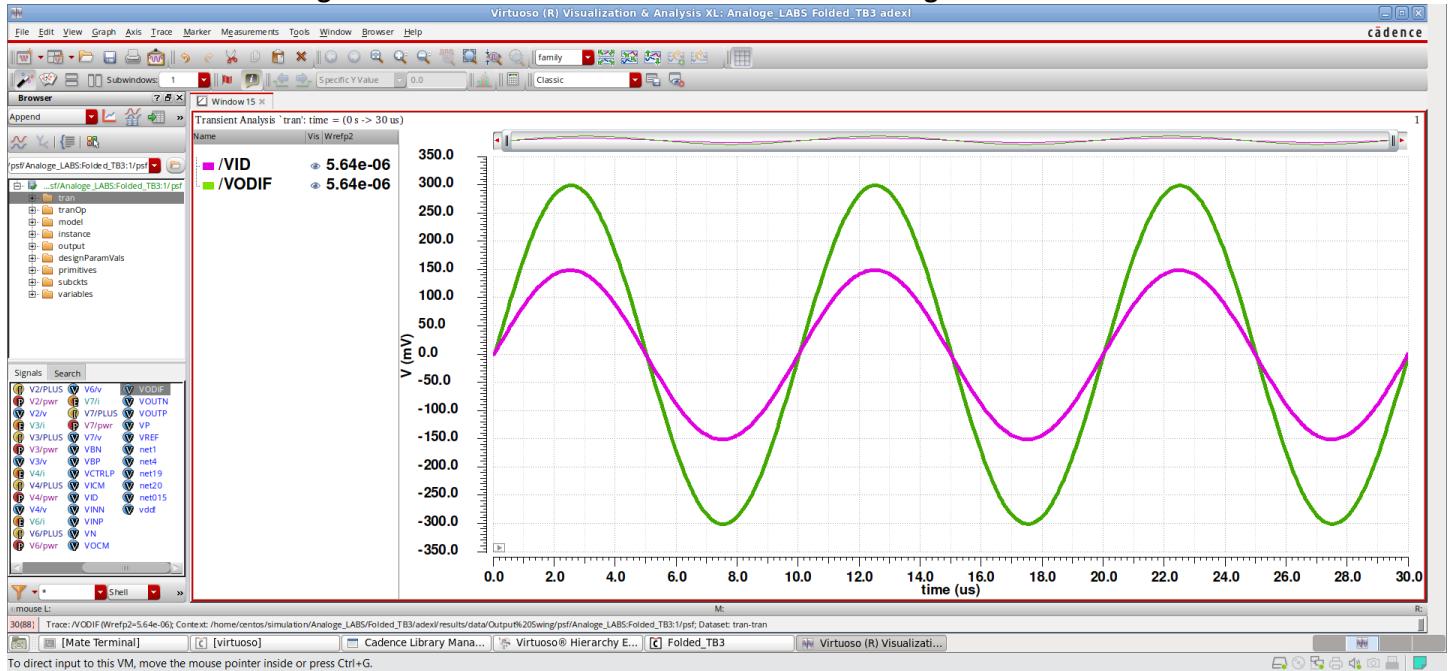
- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?
- ✓ No ,there is no ringing .

3) Output swing:

- Apply a differential sinusoidal input with freq = 100kHz and amplitude = 150mV.
- Run transient analysis for three periods (30us) with 0.1us max time step.
- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



- Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.



- Calculate the diff input and output peak-to-peak swings and the closed loop gain.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Folded_TB3:1	VIN_ppk	300m			
Analoge_LABS:Folded_TB3:1	Vout_ppk	599.8m			

$$A_{vcl} = \frac{Vout_{ppk}}{VIN_{ppk}} = 1.9993 \text{ v/v.}$$