

وَمَا أُوتِينَهُ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Ain Shams University – Faculty of Engineering – ECE Dept. – Integrated Circuits Lab.
Dr. Hesham Omran

Analog IC Design

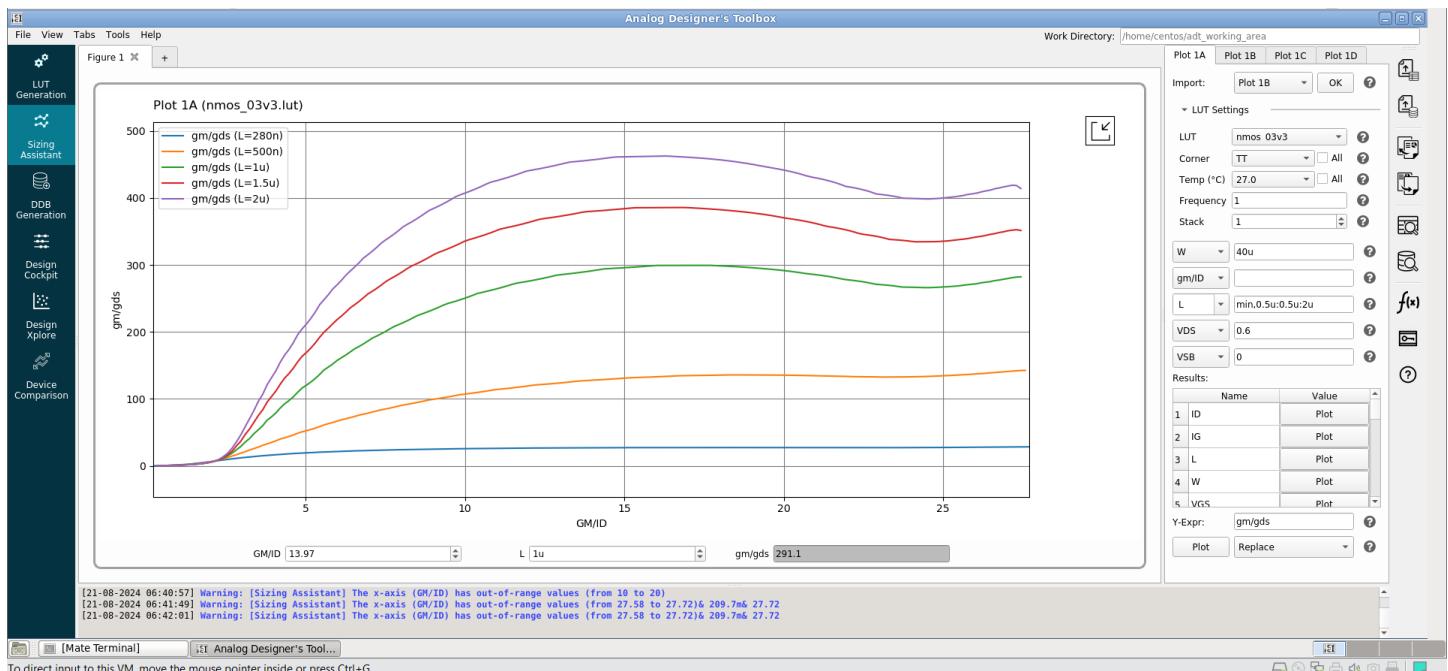
Lab 09 (Mini Project 01)

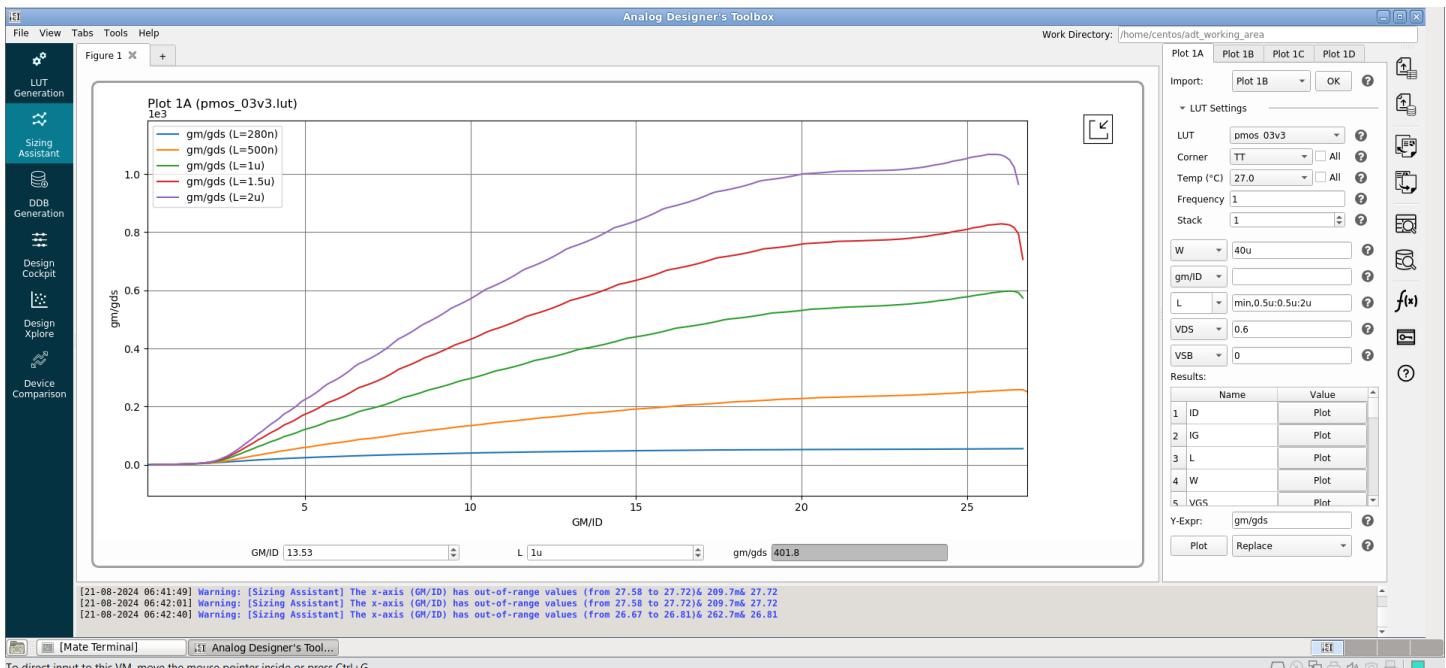
Two-Stage Miller OTA

PART 1: gm/ID Design Charts

Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set $VDS = VDD/3$ and $L = 0.18\mu, 0.5\mu:0.5\mu:2\mu$.

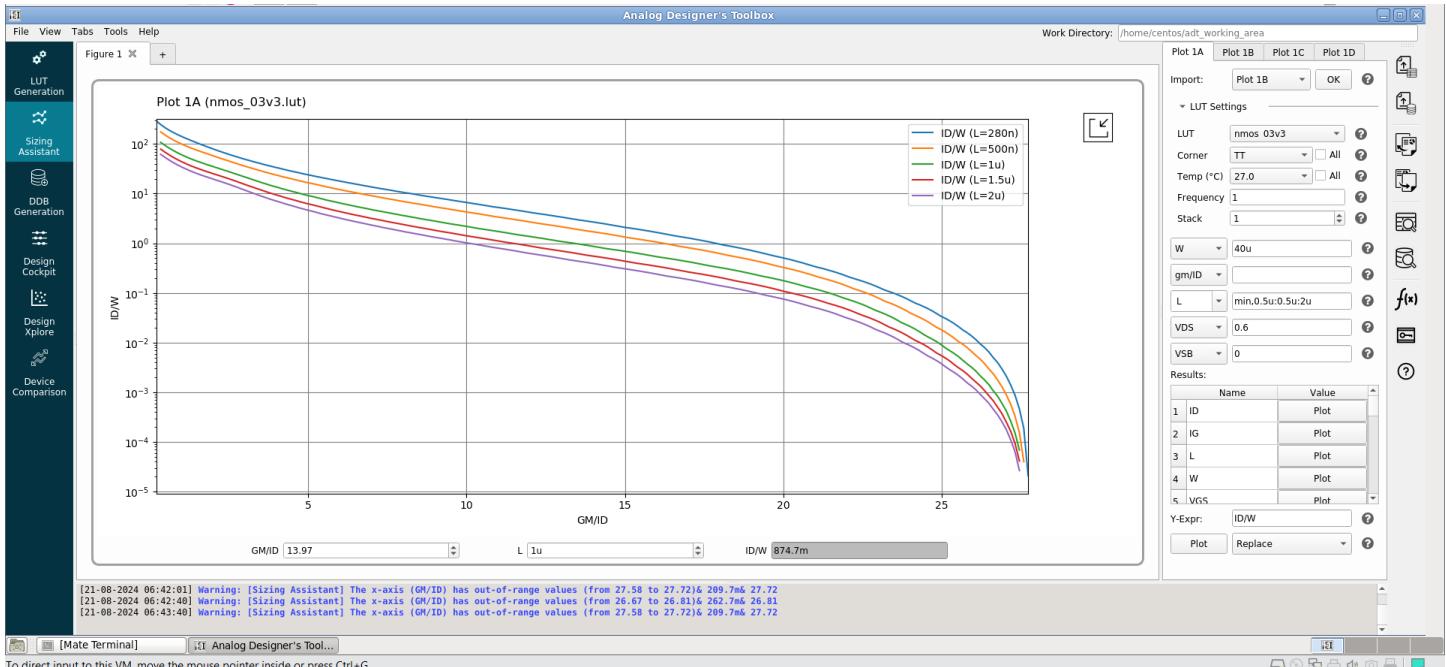
1) gm/gds



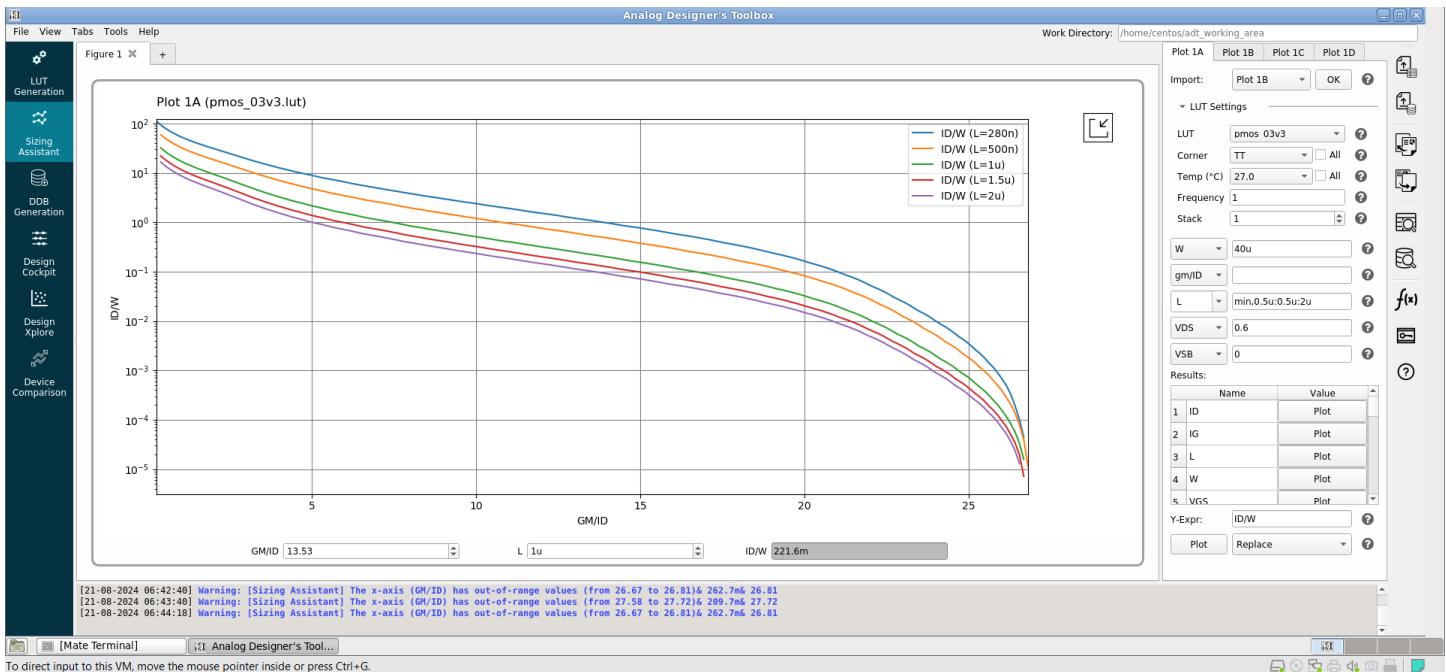


To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

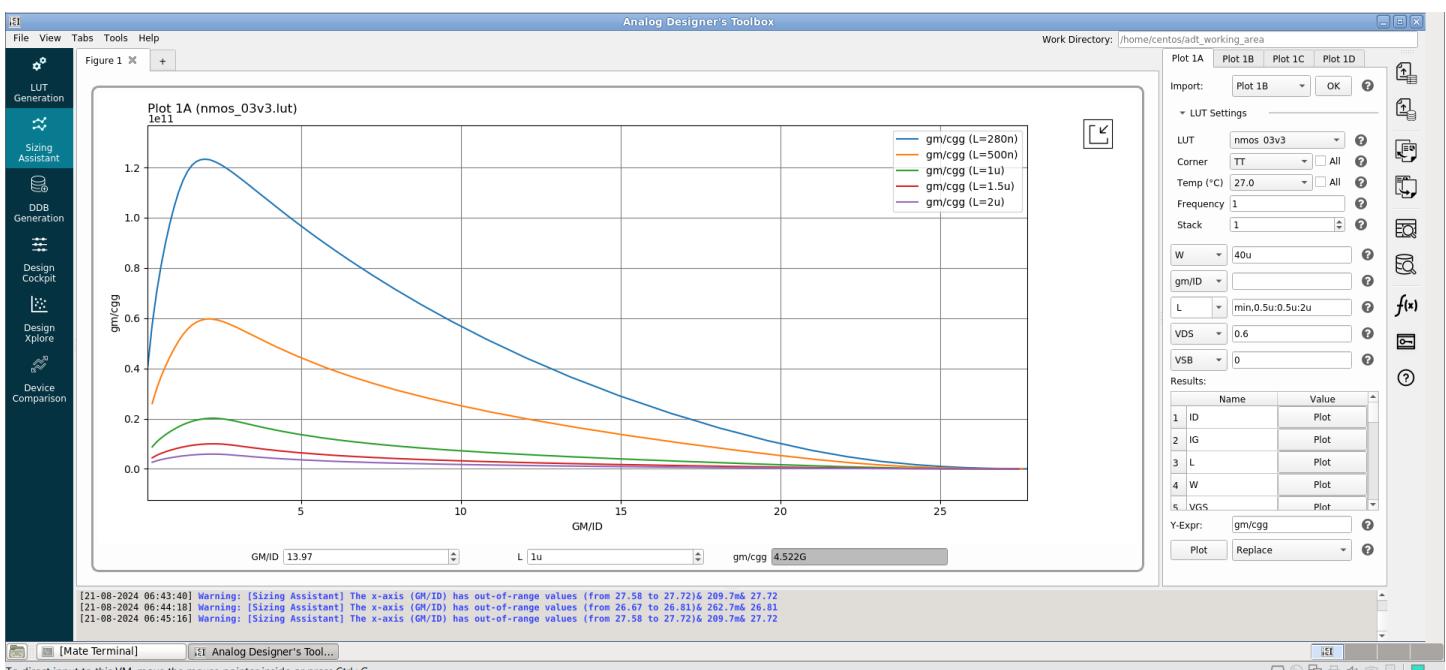
2) ID/W

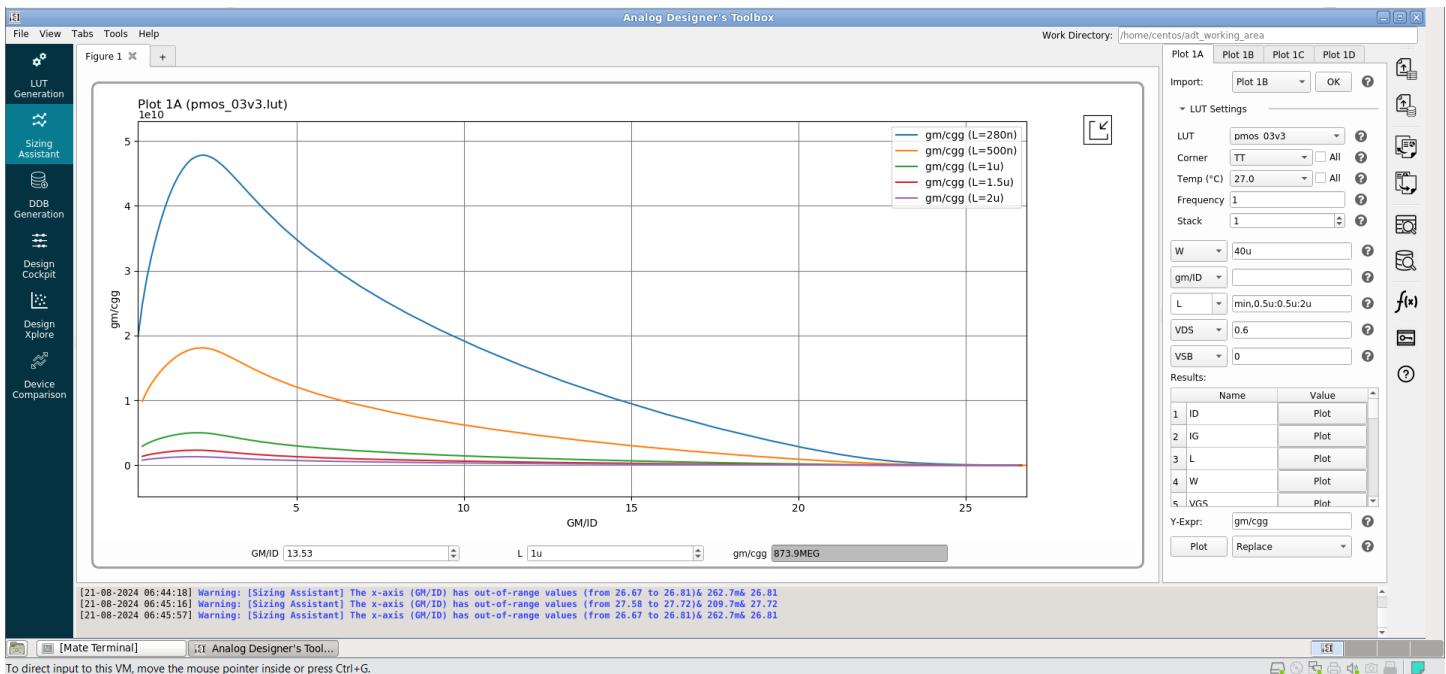


To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

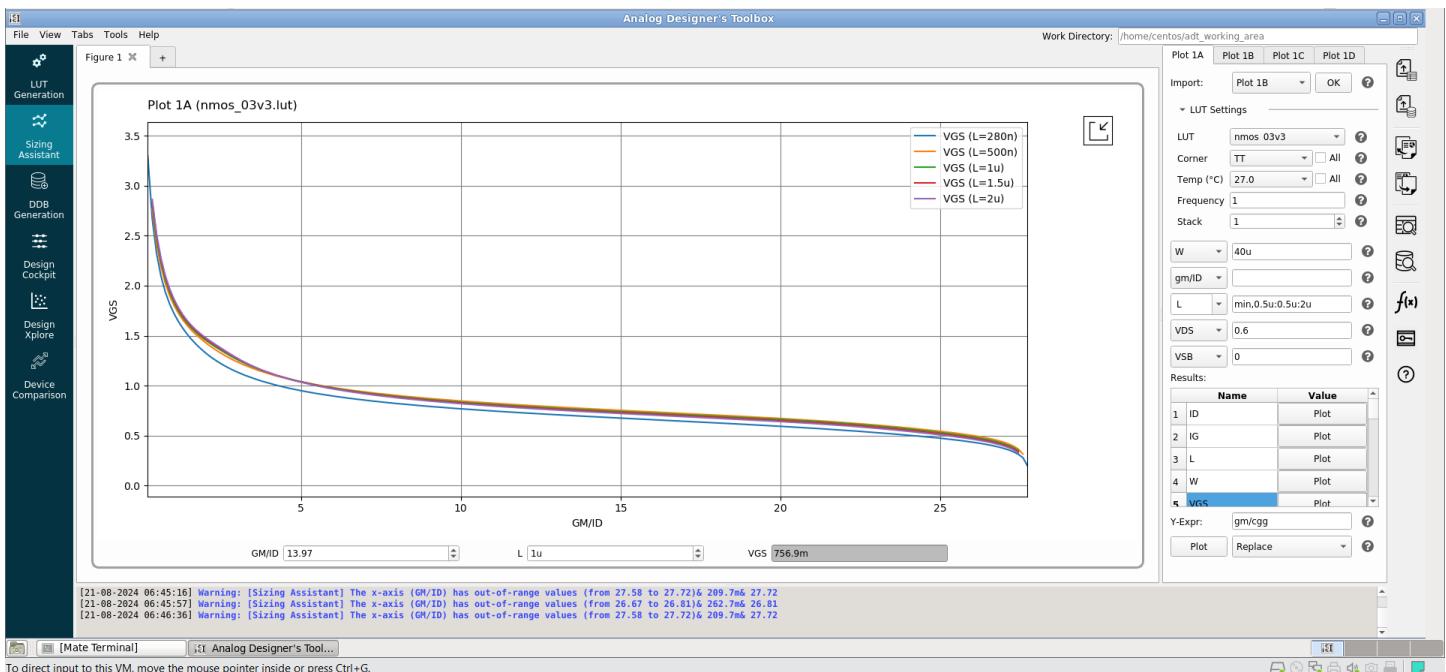


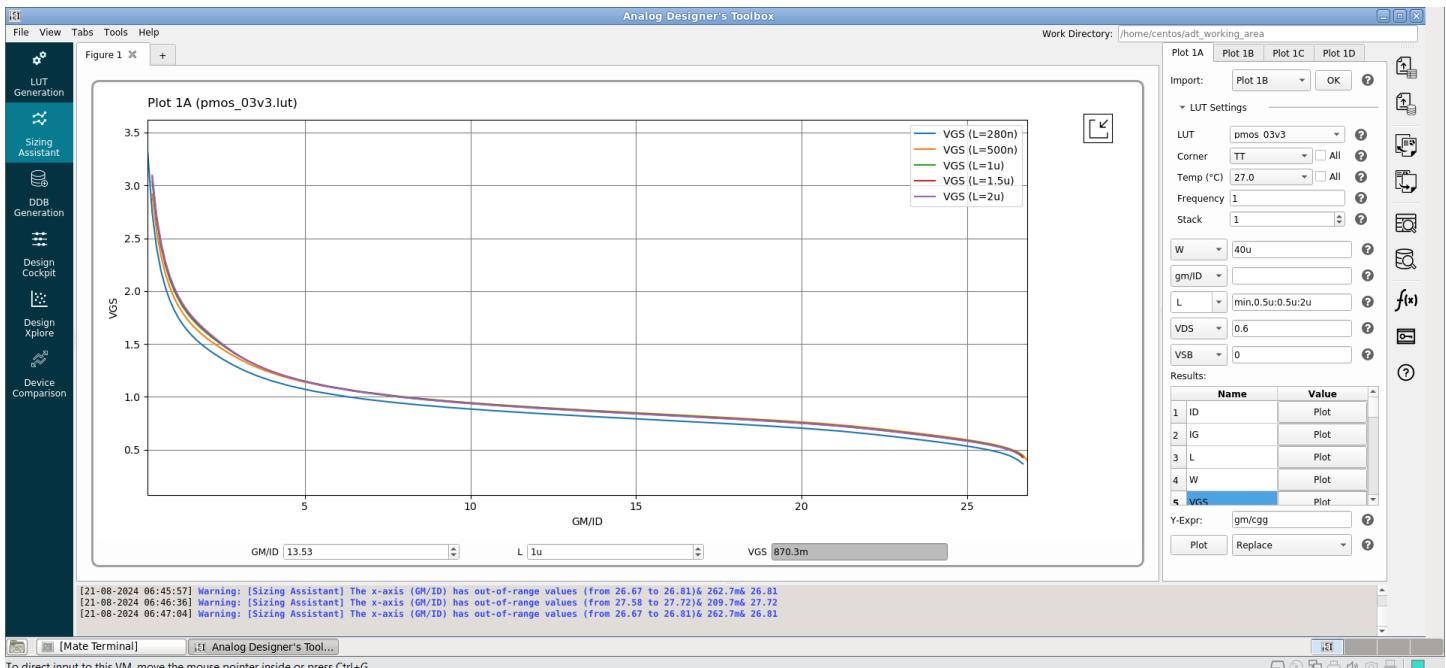
3) gm/Cgg





4) VGS





PART 2: OTA Design

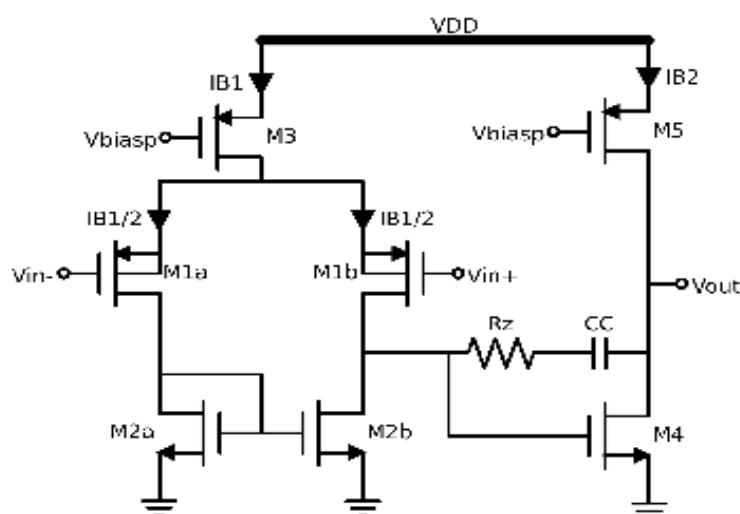
Use gm/Id methodology to design a differential input, single-ended output two-stage Miller-compensated OTA. The OTA is to be used as a buffer (unity gain feedback configuration) to probe sensitive internal signals in a complex mixed-signal design. The OTA should achieve the specs below.

Technology	0.18um
Supply Voltage	1.8V
Static gain error	<=.05%
CMRR @ DC	74db
Phase margin	>=70
OTA Current Consumption	60uA
CMIR_High	1V
CMIR_Low	.2V
Output Swing	.2-1.6 V
Load	5pF
Buffer Closed Loop rise time	<=70ns
Slew rate	5V/us

1. Detailed design procedure and hand analysis. Justify why you used NMOS or PMOS input pair for each stage.

❖ Due to the body effect the CMIR_High is not feasible , so that we choose to be CMIR_High=.8V.

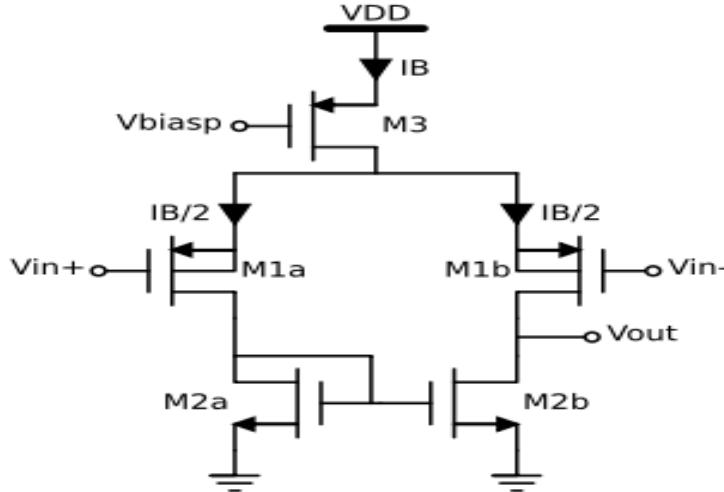
- ✓ As static gain error<=.05% , static gain error $=\frac{1}{LG}$, then $LG>=2000V/V =66db$.
- ✓ As PM $>=70deg$, then $wpnd>=4*wu$ then $\frac{Gm2}{CL} >= \frac{4Gm1}{Cc}$.
- ✓ As Trise $<=70ns$, Trise $=2.2\tau$,then $\tau<=31.82ns$ then $GBW=\frac{1}{\tau}>=31.43Mrad/s$.
- ✓ As SR=5V/uS , $SR=\frac{IB1}{Cc}$, then $IB1=SR*Cc$.



❖ If we assumed $C_c = .5 \times C_L = 2.5 \text{ pF}$.

- ✓ $IB_1 = SR \times C_c = 12.5 \mu\text{A}$, $IB_2 = I_{\text{total}} - IB_1 = 60 \mu\text{A} - 12.5 \mu\text{A} = 47.5 \mu\text{A}$.
- ✓ As $gm_{1,2} = GBW \times C_c = 78.56 \mu\text{S}$, as we neglect the self-capacitances of the transistors we should increase $gm_{1,2}$, so that $gm_{1,2} = 85 \mu\text{S}$, $(gm/ID)_{1,2} = 13.6 \text{ S/A}$.
- ✓ As $\frac{Gm_2}{C_L} = \frac{4Gm_1}{C_c}$ (from PM spec), then $Gm_2 = 8 \times Gm_1 = 680 \mu\text{S}$, $(gm/ID)_2 = 14.32 \text{ S/A}$.
- ✓ As $Av = Av_1 \times Av_2$, if we assume Av_1 double Av_2 , then $Av_1 = 36 \text{ db}$, $Av_2 = 30 \text{ db}$.
- ✓ As $Av_1 = 36 \text{ db}$, $CMRR = 74 \text{ db}$, then $Av_{cm} = -38 \text{ db}$.

➤ First Stage:



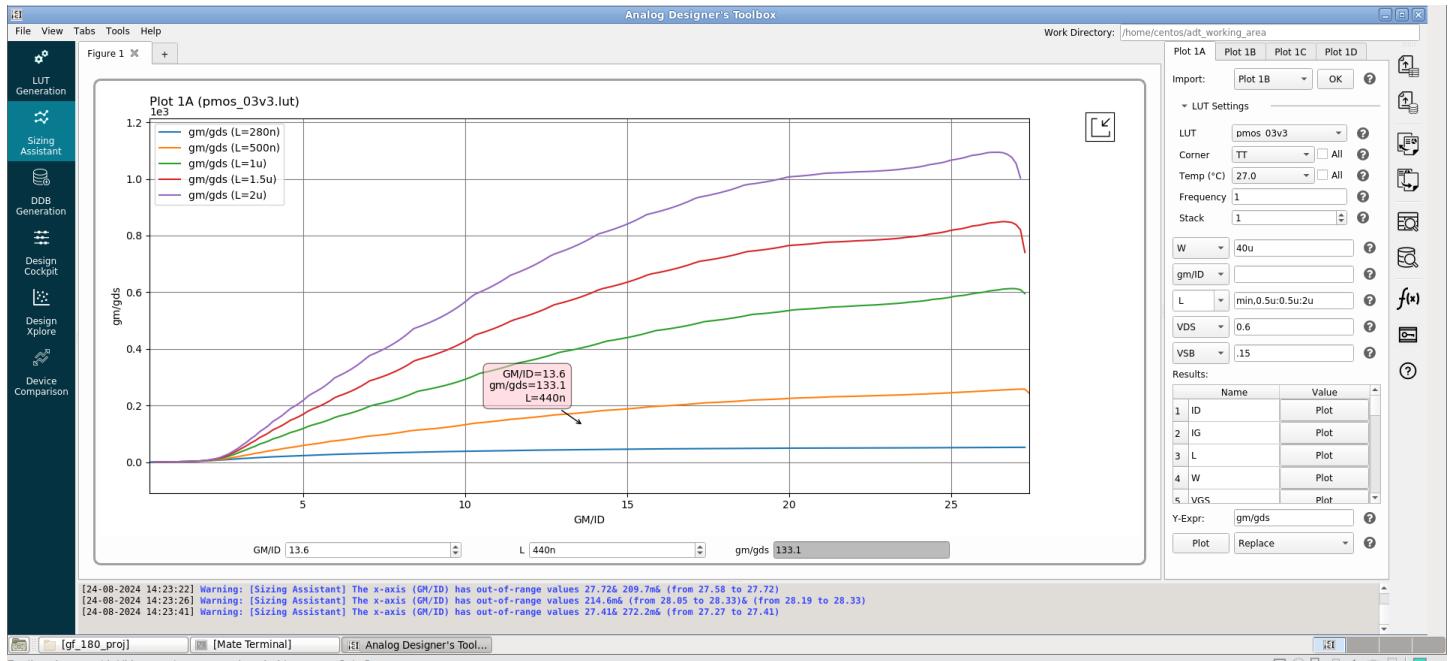
Givens:

- $A_{vd}=36\text{db}$.
- $A_{vcm}=-38\text{db}$
- **CMIR=.2-.8V (as the CMIR close to ground rail and away from VDD we choose 5T_OTA with PMOS input Pair).**
- $I_{SS}=I_B=12.5\mu\text{A}$.
- $(Gm/ID)_{1,2}=13.6$.

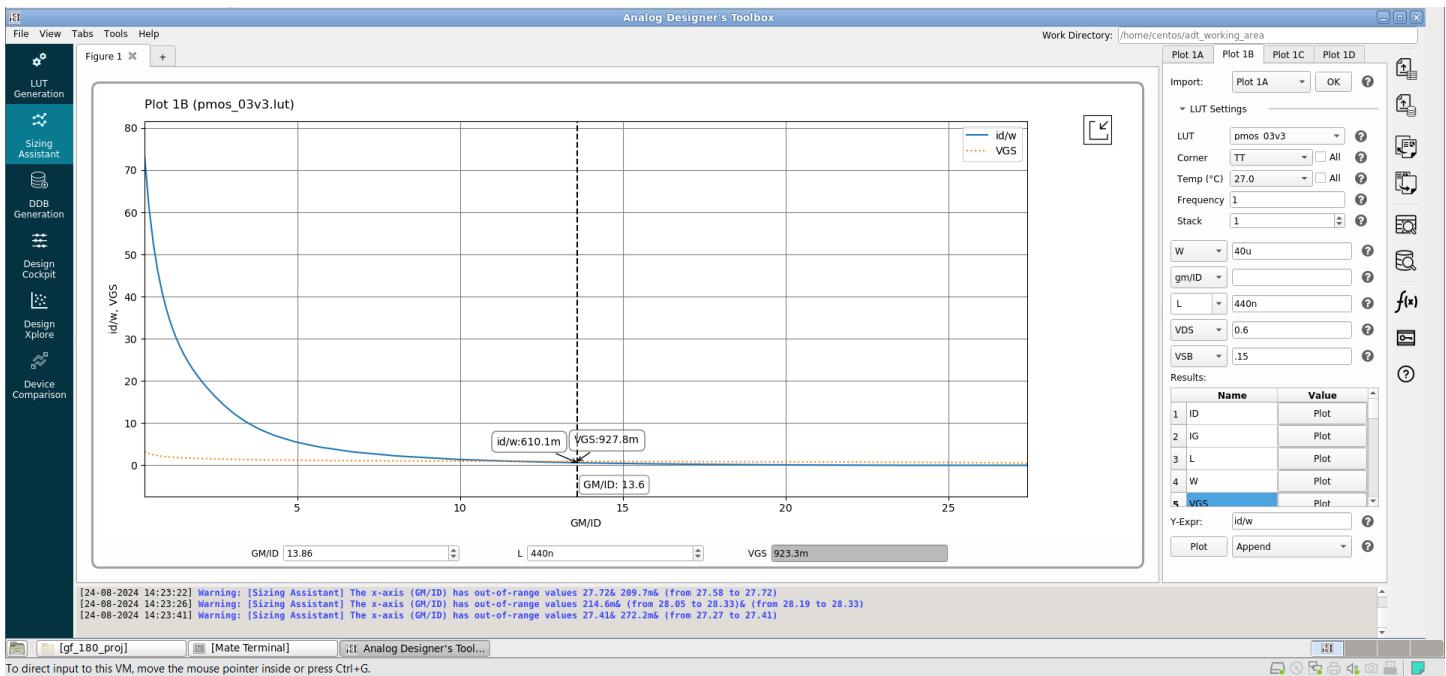
Design Steps:

1. Input Pair:

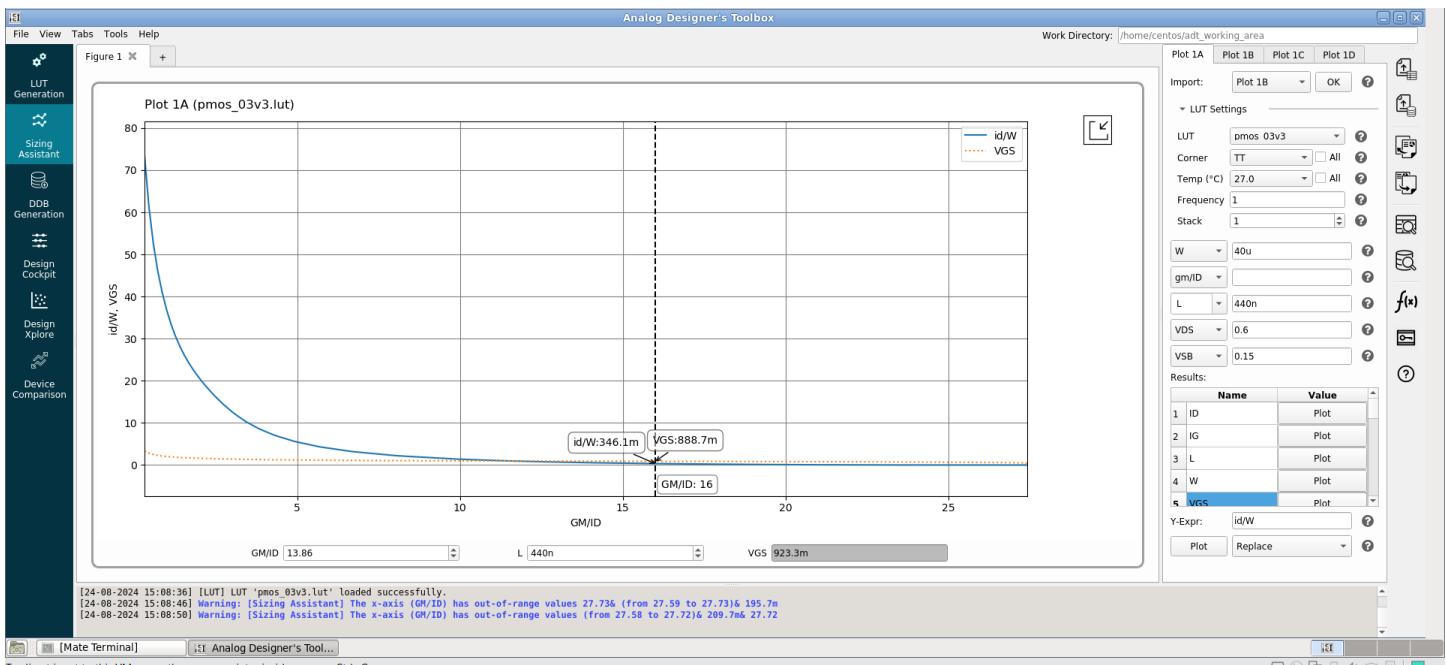
- ✓ as $A_{vd}=\frac{gm_{1,2}}{gds_{1,2}+gds_{3,4}}$, assume $gds_{1,2}=gds_{3,2}$, then $A_{vd}=\frac{gm_{1,2}}{2*gds_{1,2}}$ or $(gm/gds)_{1,2}=2A_{vd}>=126.2\text{V/V}$.
- ✓ to include body effect of the input PMOS we assume $|V_{sb}|=150\text{mV}$.



L_{1,2}=440nm , ID/W=610.1m , W_{1,2}=10.25μm , V_{GS1,2}=917.8mV.



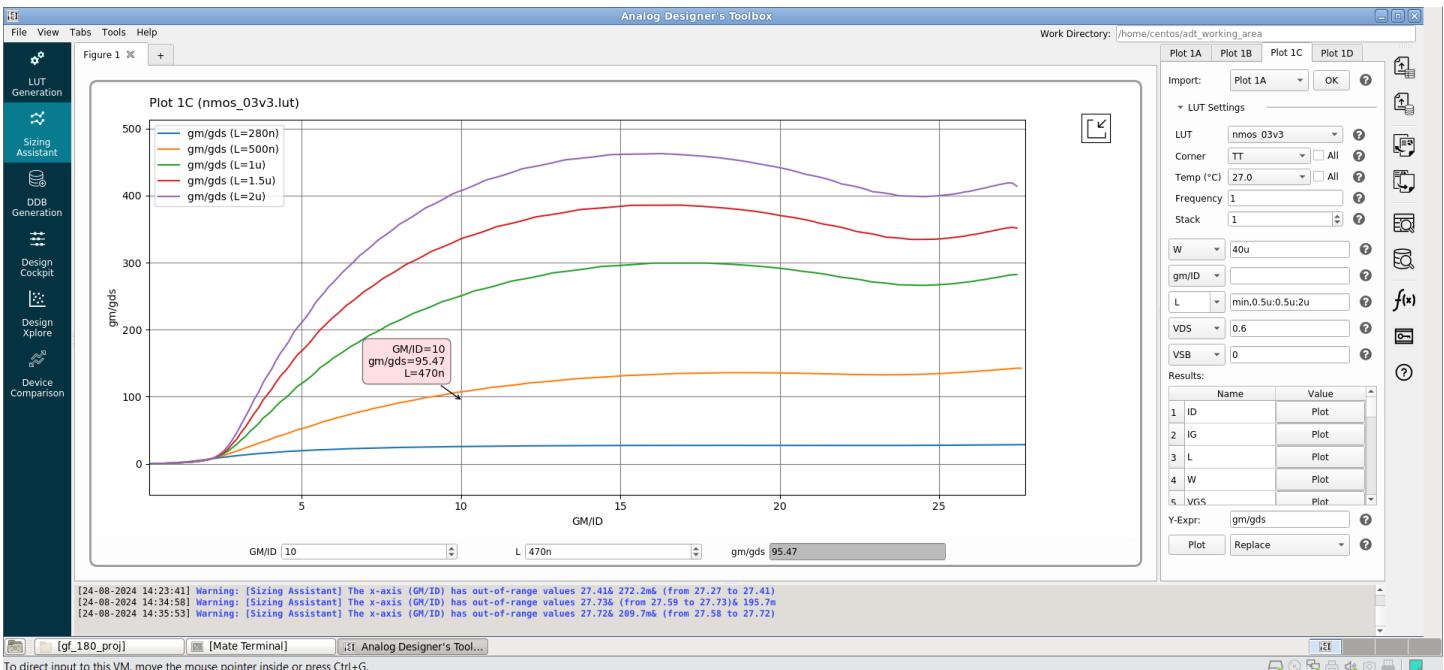
To reduce VGS we increase the gm/ID this will increase the gain and GBW (GBW may not increase that is as gm/ID increase the width increase and the capacitances increases) , so that we choose gm/ID=16.



The new ID/W=.3461 , W1,2=18.06um , VGS1,2=888.7mV.

2. CM Load:

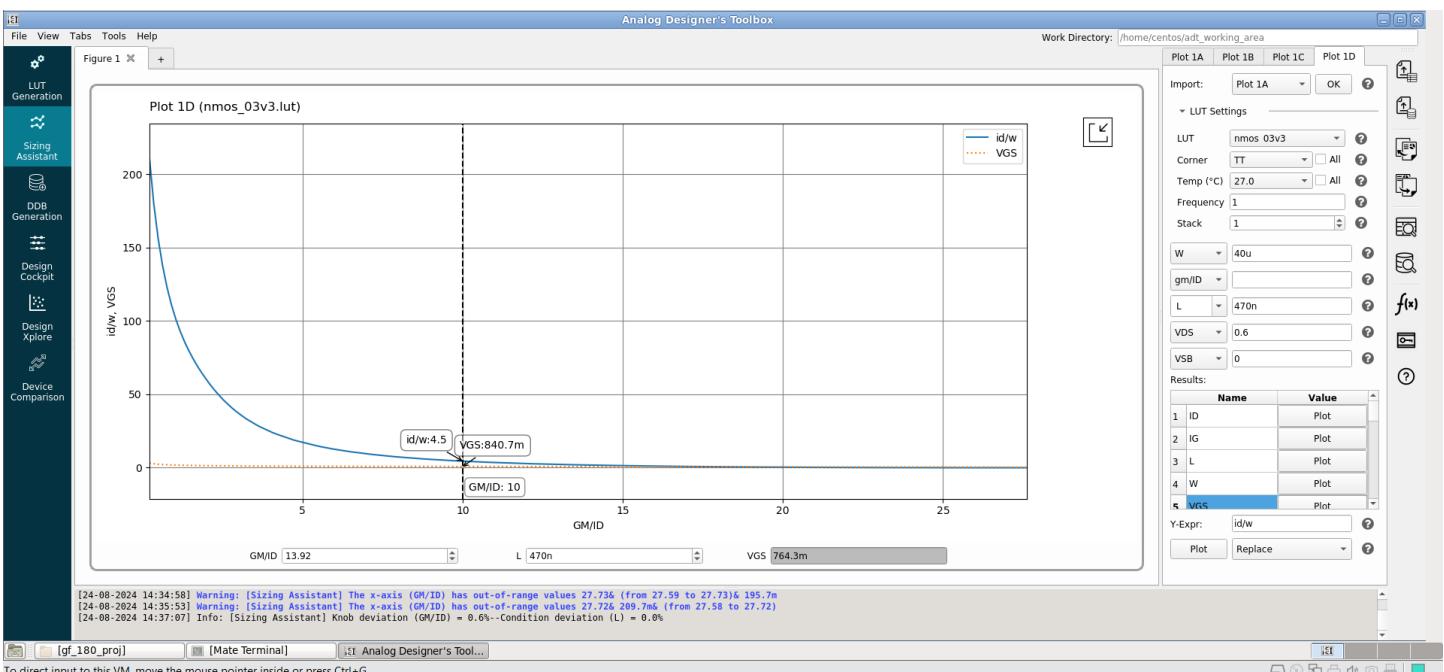
- ✓ Gds3,4=gds1,2=.674uS.
- ✓ As CMIR-low=VGS3,4-|Vth1,2|<.2V , VGS3,4<976mV.
- ✓ We assume gm/ID=10 , then gm/gds= 93V/V.

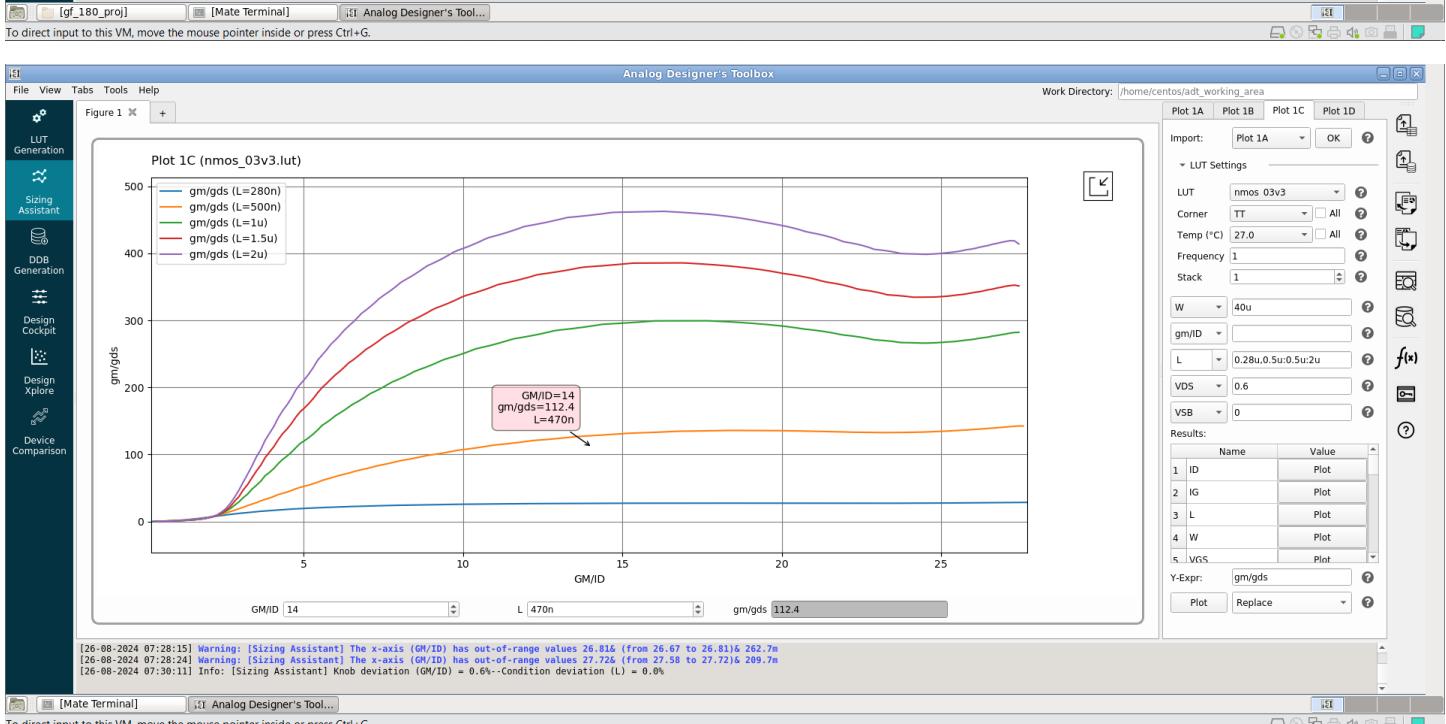
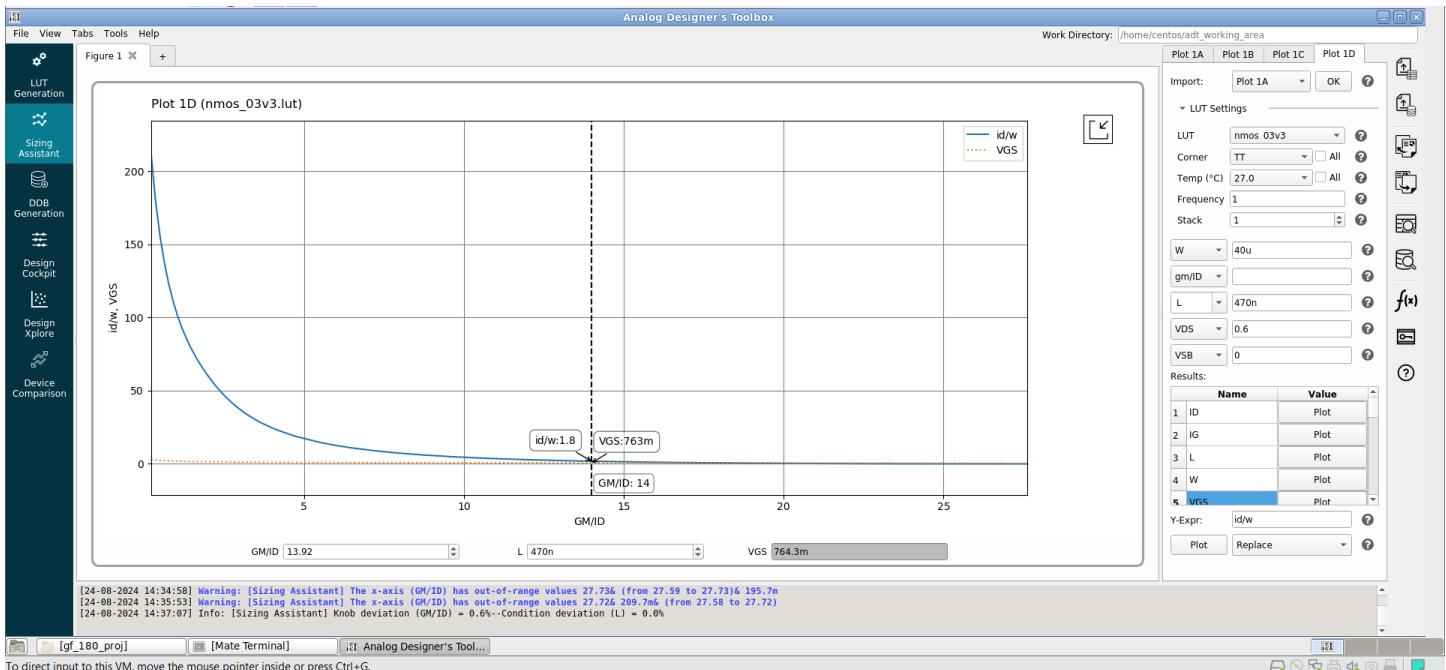


L_{3,4}=470nm , VGS_{3,4}=840.8mV so that VGSQ<VGSm_{ax} , ID/W=4.503 then W_{3,4}=1.4um.

Note : this large VGS we cause systematic offset ,so that we choose gm/ID=14,The increase in gm/ID will increase the gain which is good.

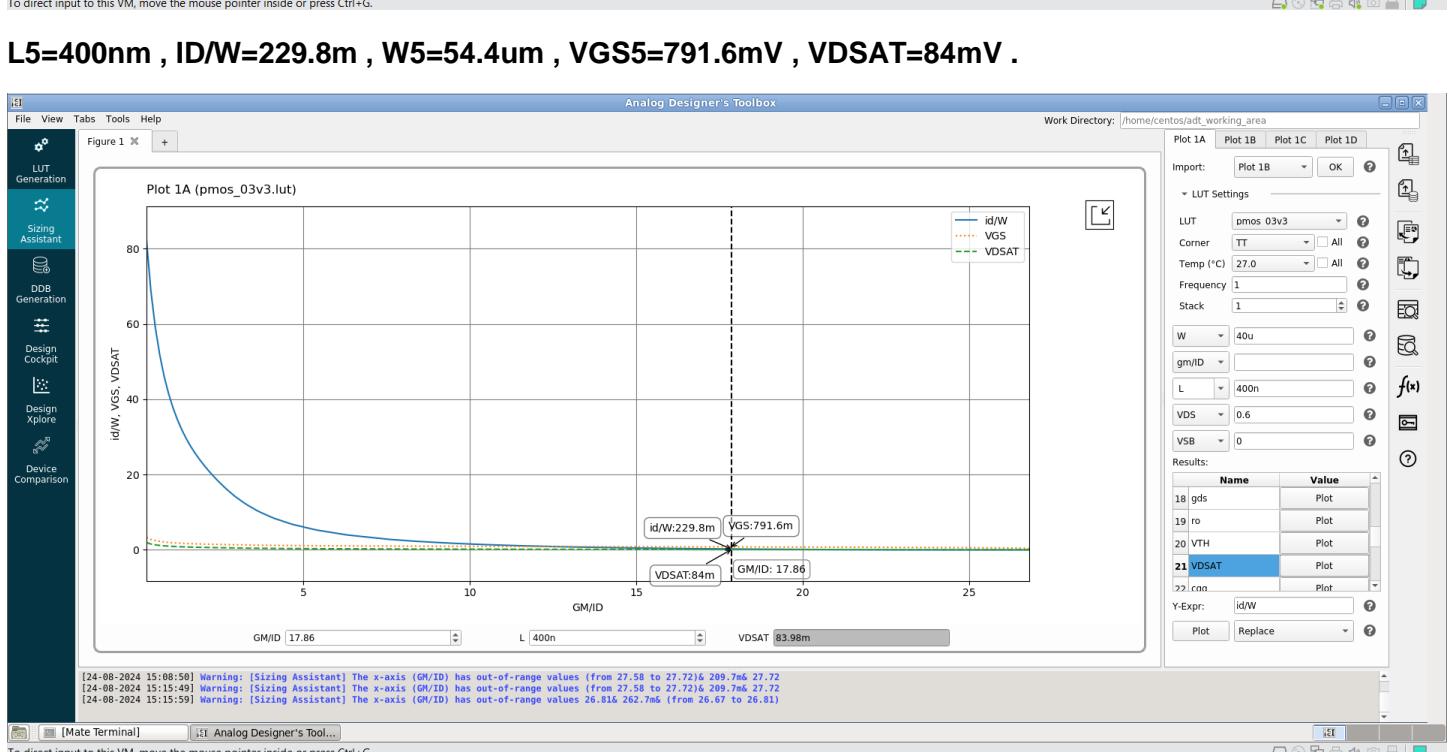
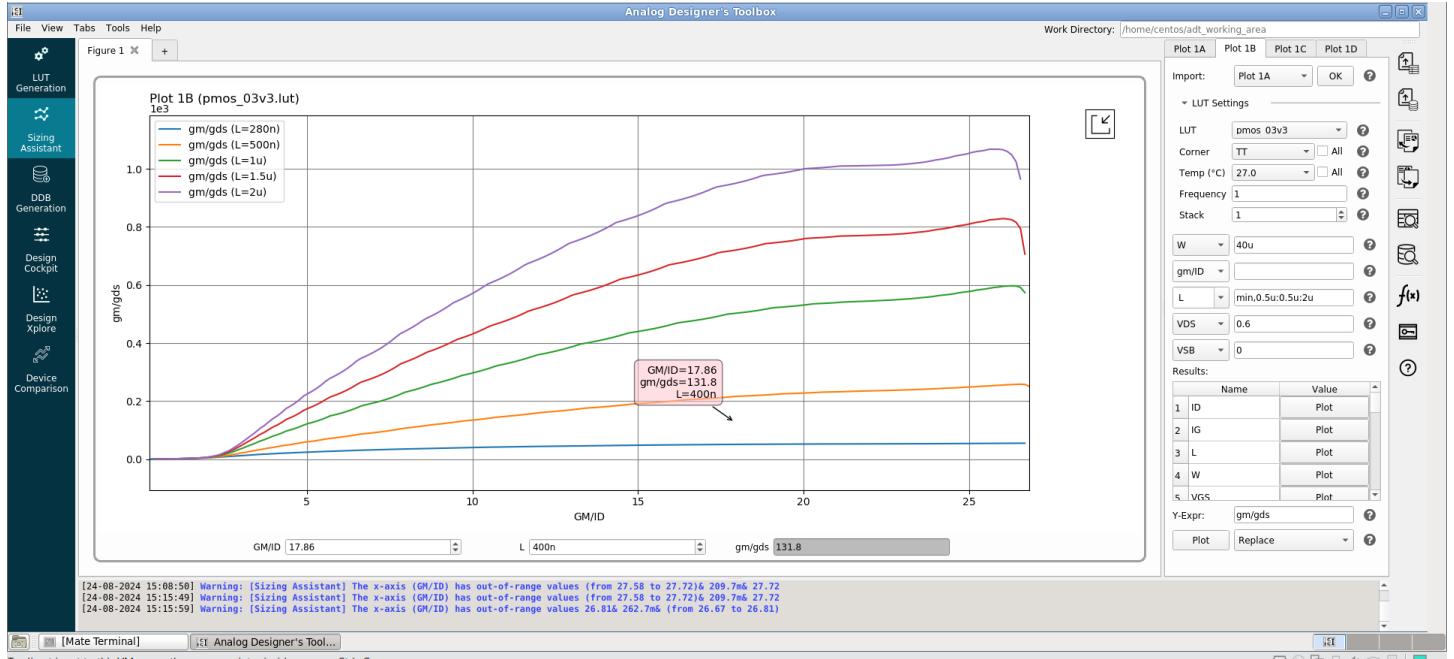
The new ID/W=1.8 , then W_{3,4}=3.47um , VGS_{3,4}=763m.



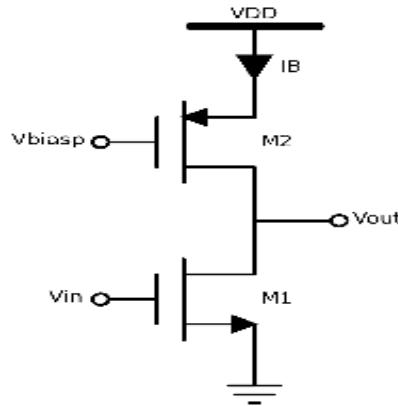


3. Tail CS:

- ✓ as $A_{VCM} = \frac{gds5}{2gm3,4} = -38\text{db} = .01$, then **gds5=1.75uS**.
- ✓ as $CMIR_{high} = VDD - V^*5 - |VGS1,2| > .8$, then $V^*5 < 82\text{mV}$ or $gm/ID > 24.4$, this is very large gm/ID , so that we need to increase the gm/ID of the input pair.
- ✓ after increase in gm/ID of the input pair, $V^*5 <= 112\text{mV}$ or $gm/ID > 17.86$.
- ✓ $gm/gds = 127.6\text{V/V}$.



➤ Second Stage:

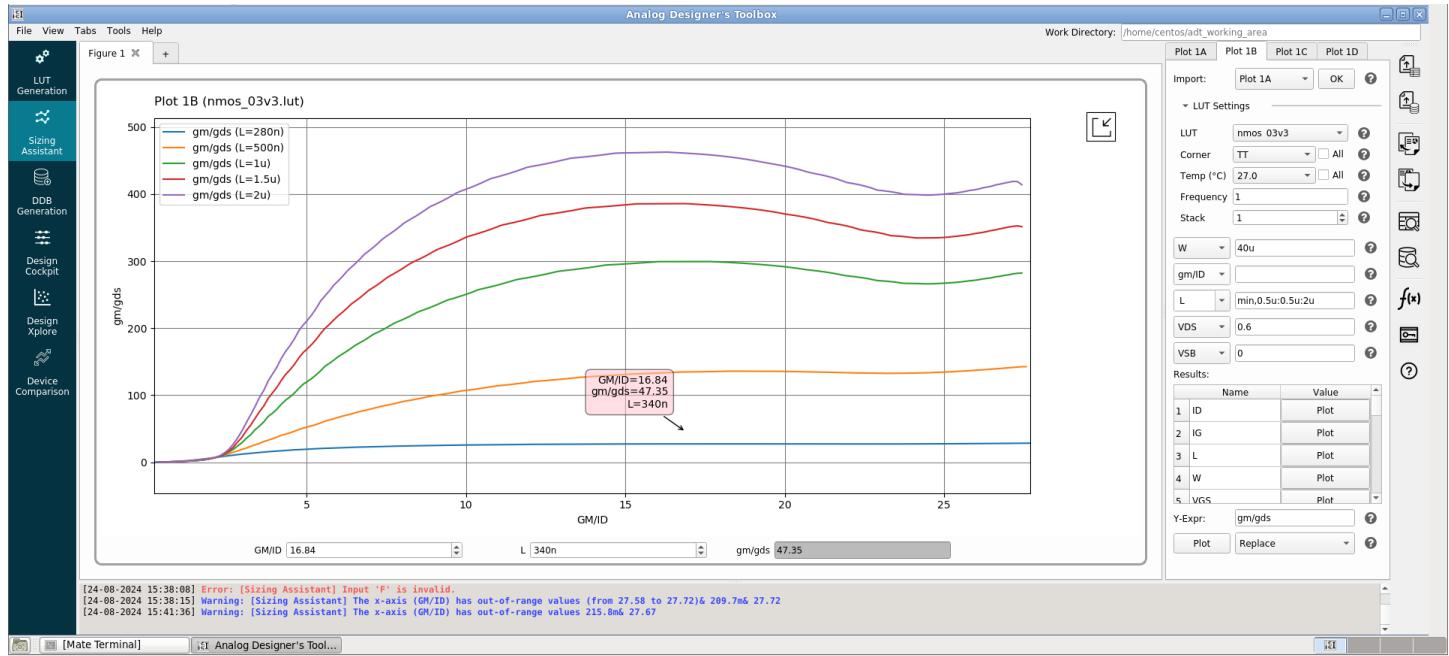


Givens:

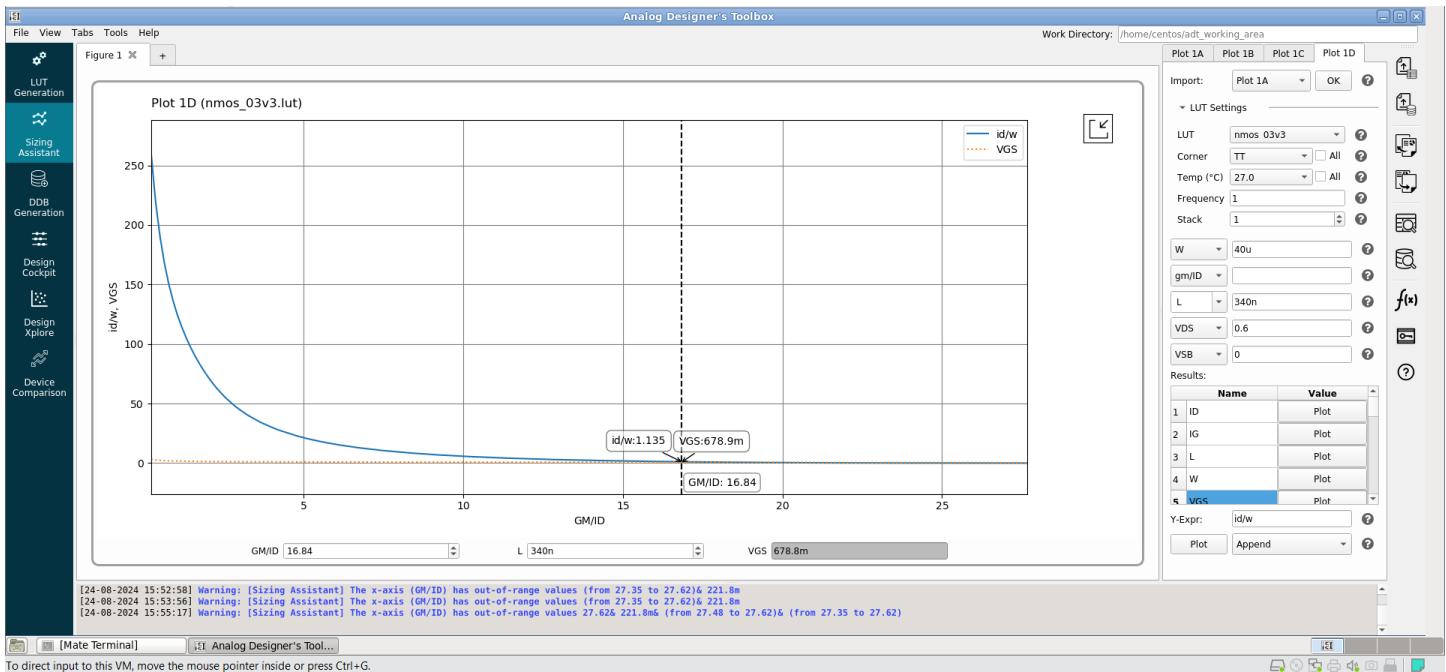
- AV=30db
- GM2=680uS , (gm/ID)6=14.32 , as we increase (gm/ID)1,2 and gm1,2=100uS , we need to increase Gm2=800uS , then gm/ID=16.84 .
- L7=L5=400nm , (gm/ID)7=(gm/ID)5=17.86 .
- As ID5=IB1=12.5uA , ID7=IB2=47.5uA , then W7= $\frac{ID7}{ID5} * W5 = 206.72\mu m$.
- As gds is proportional to W , then gds7=6.65uS.

NMOS:

$$\text{As } Av = \frac{gm_6}{gds_6 + gds_7} = \frac{800u}{gds_6 + 6.65u} = 32 , gds_6 = 14.6uS , (gm/gds)_6 = 44V/V.$$

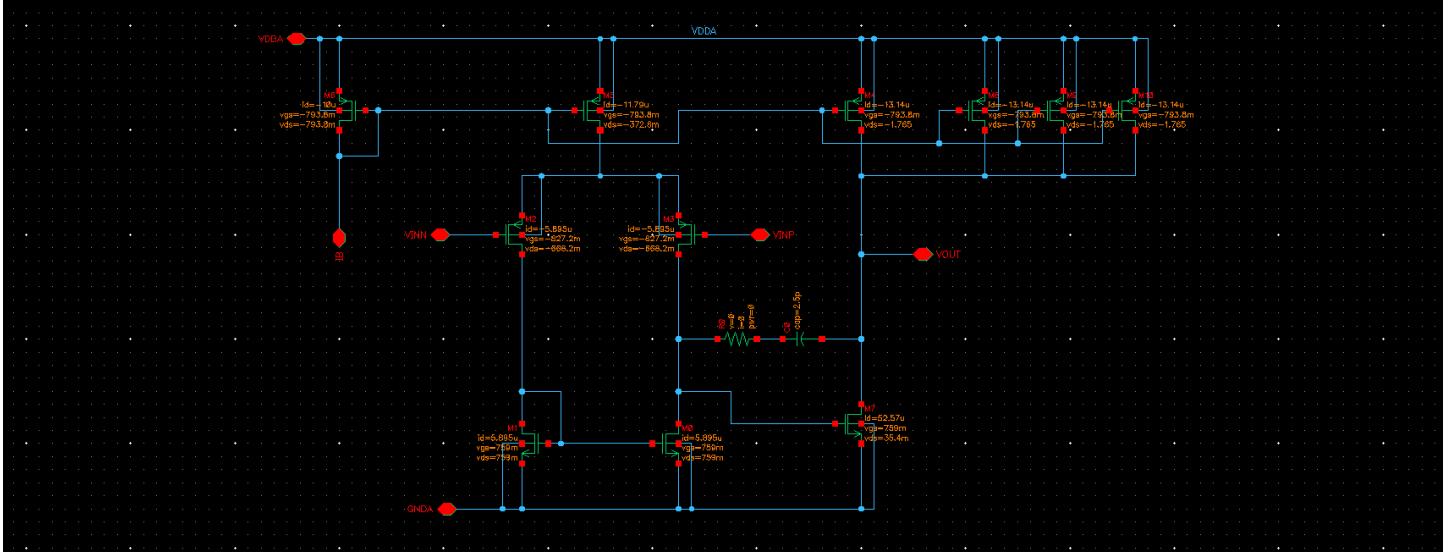


L6=340nm , ID/W=1.135 , W6=41.85um , VGS6=678.8mV.

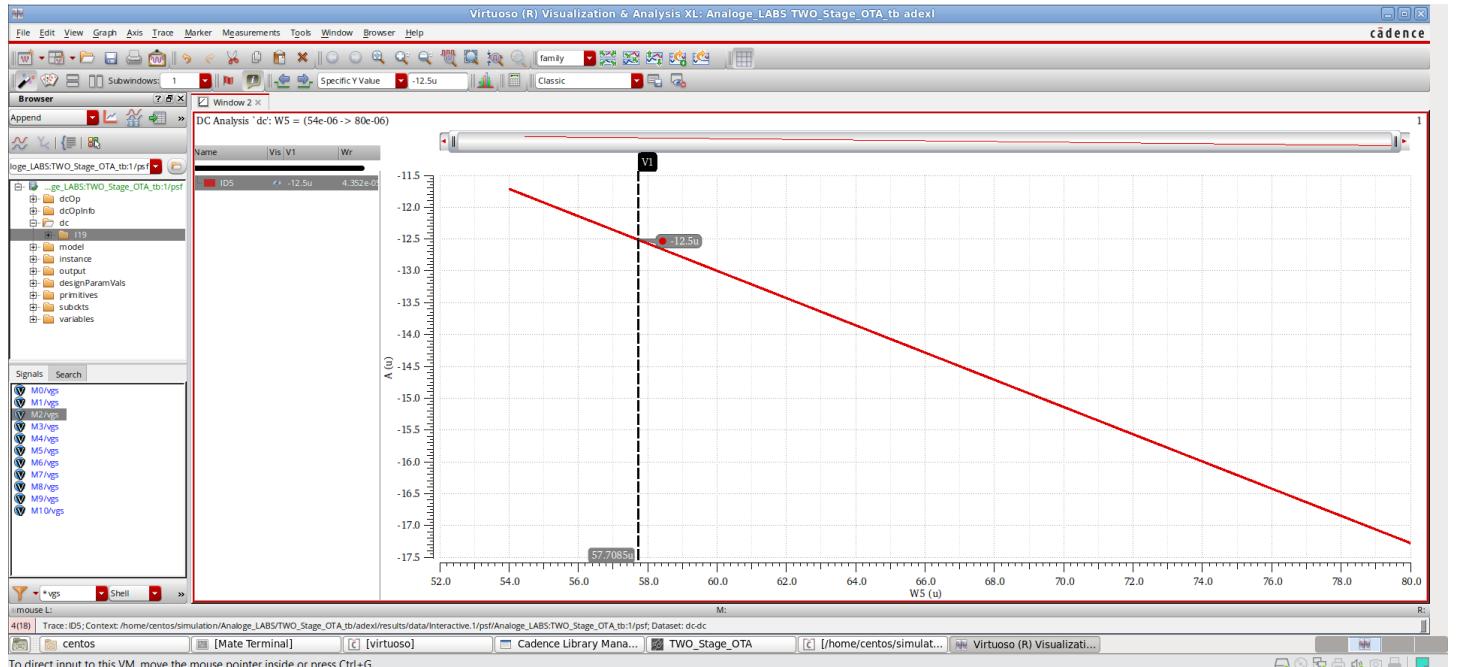


But this $VGS=678.8\text{mV}$ is less than $VGS_{3,4}=764.3\text{mV}$, so that we need to sweep W_3 & L_3 to cancel the systematic offset Voltage, we will do that in the testbench.

	M1,2	M3,4	M5	M6	M7	Mref
W	18.06um	3.47um	54.4um	41.85um	206.72um	43.52um
L	440nm	470nm	400nm	340nm	400nm	400nm
ID	6.25uA	6.25uA	12.5uA	47.5uA	47.5uA	10uA
Gm/ID	16S/A	14S/A	17.86S/A	16.84S/A	17.86S/A	17.86S/A
gm	100uS	87.5uS	223.25uS	799.9uS	839.8uS	178.6uS
vdsat	102.8mV	119.3mV	85.07mV	88.8mV	85.07mV	85.07mV
VGS	891.1mV	765.2mV	793.9mV	680.4mV	793.9mV	793.9mV
Vov	47.9mV	58.9mV	17mV	4.1mV	17mV	17mV
V*	125mV	142.86mV	111.98mV	118.76mV	111.98mV	111.98mV

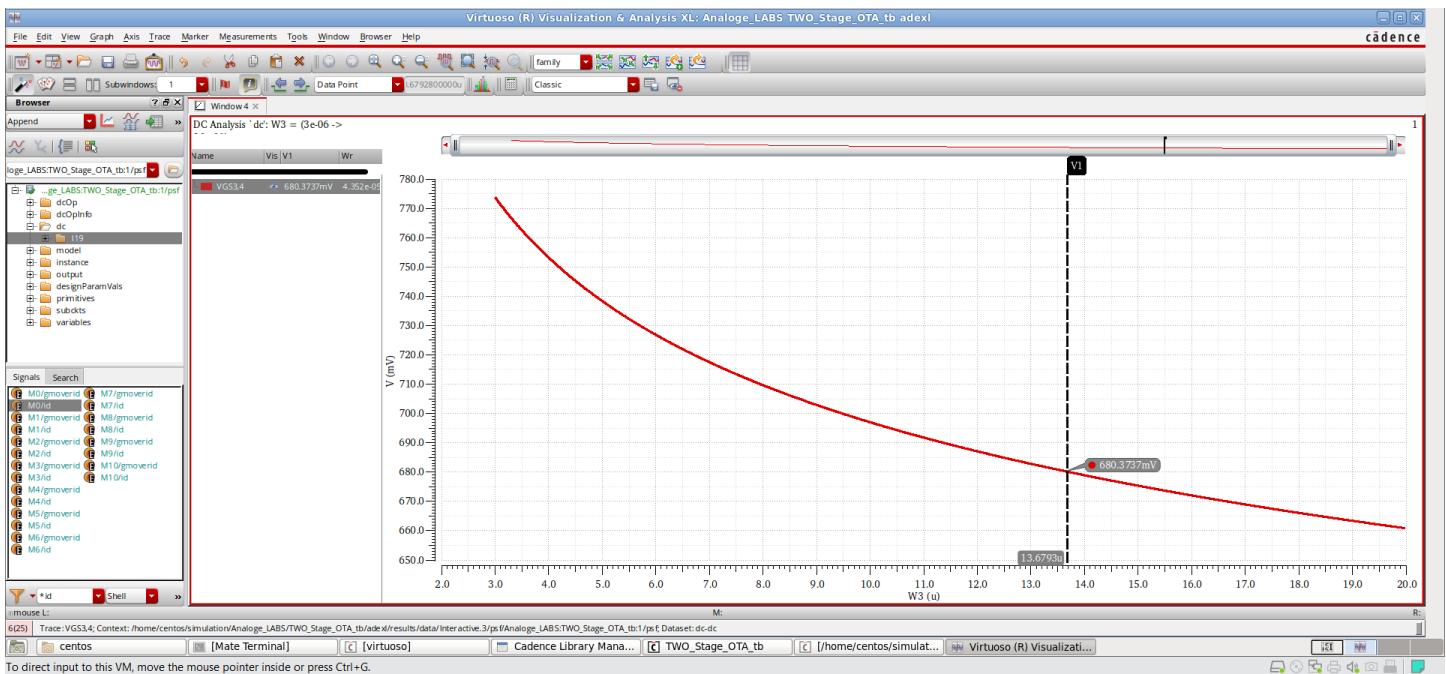


To increase the current of the first stage we sweep W5.

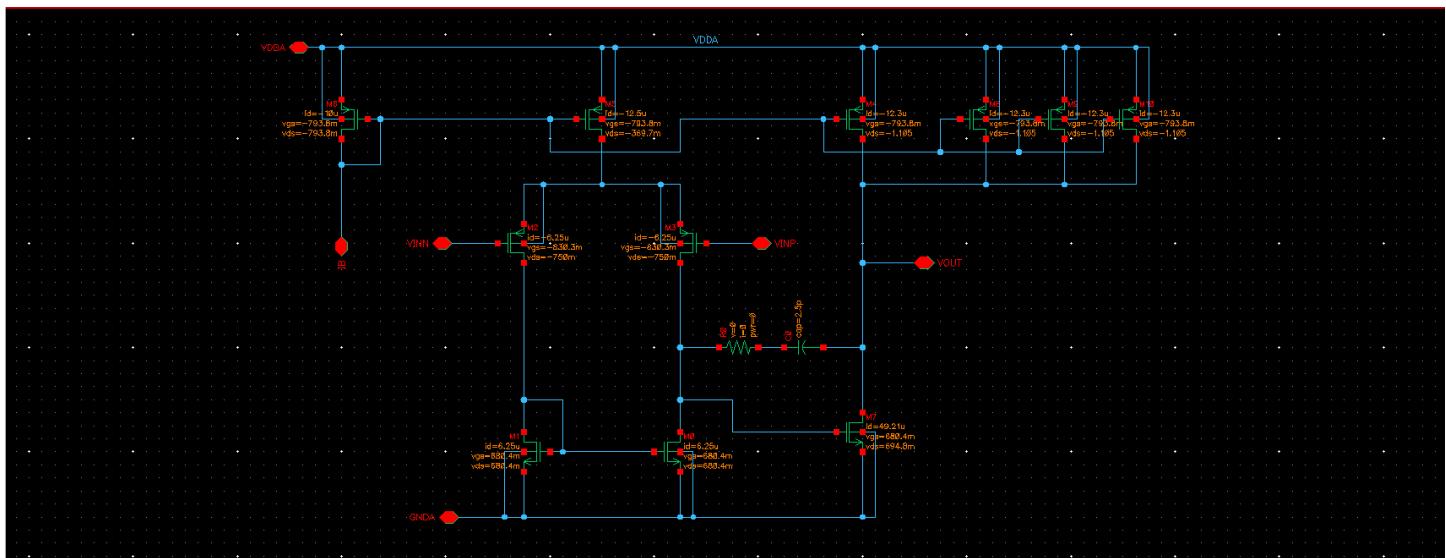


W5=57.7μm.

To cancel the systematic offset voltage we sweep W3 to reduce VGS3.

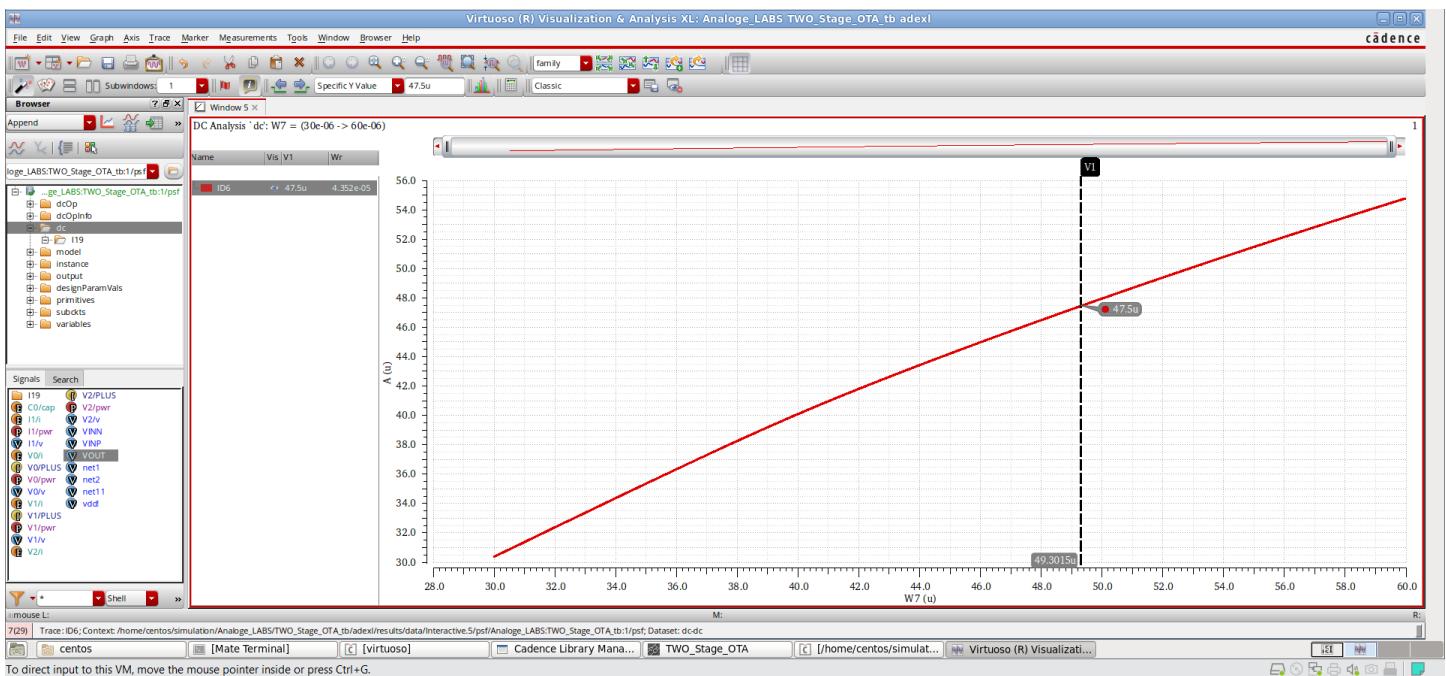


W3=13.68um.

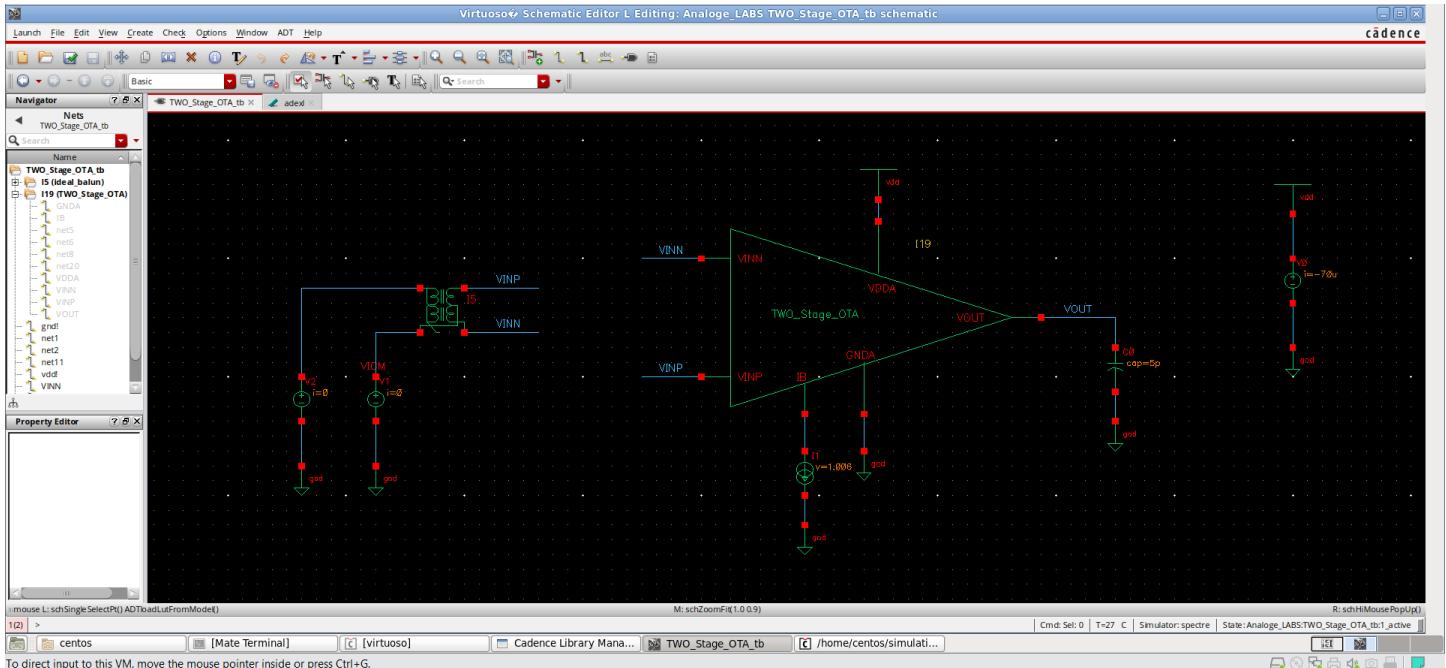


To set $IB2=47.5\mu A$, we sweep $W7$.

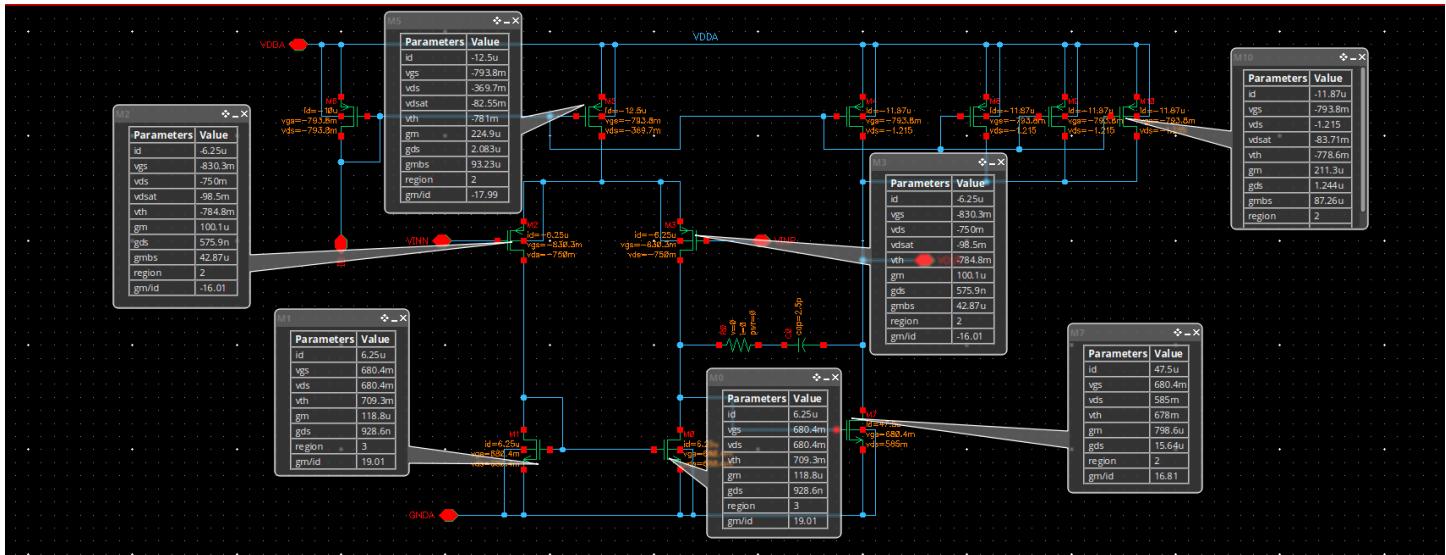
W7=4*49.3uA.



PART 3: Open-Loop OTA Simulation



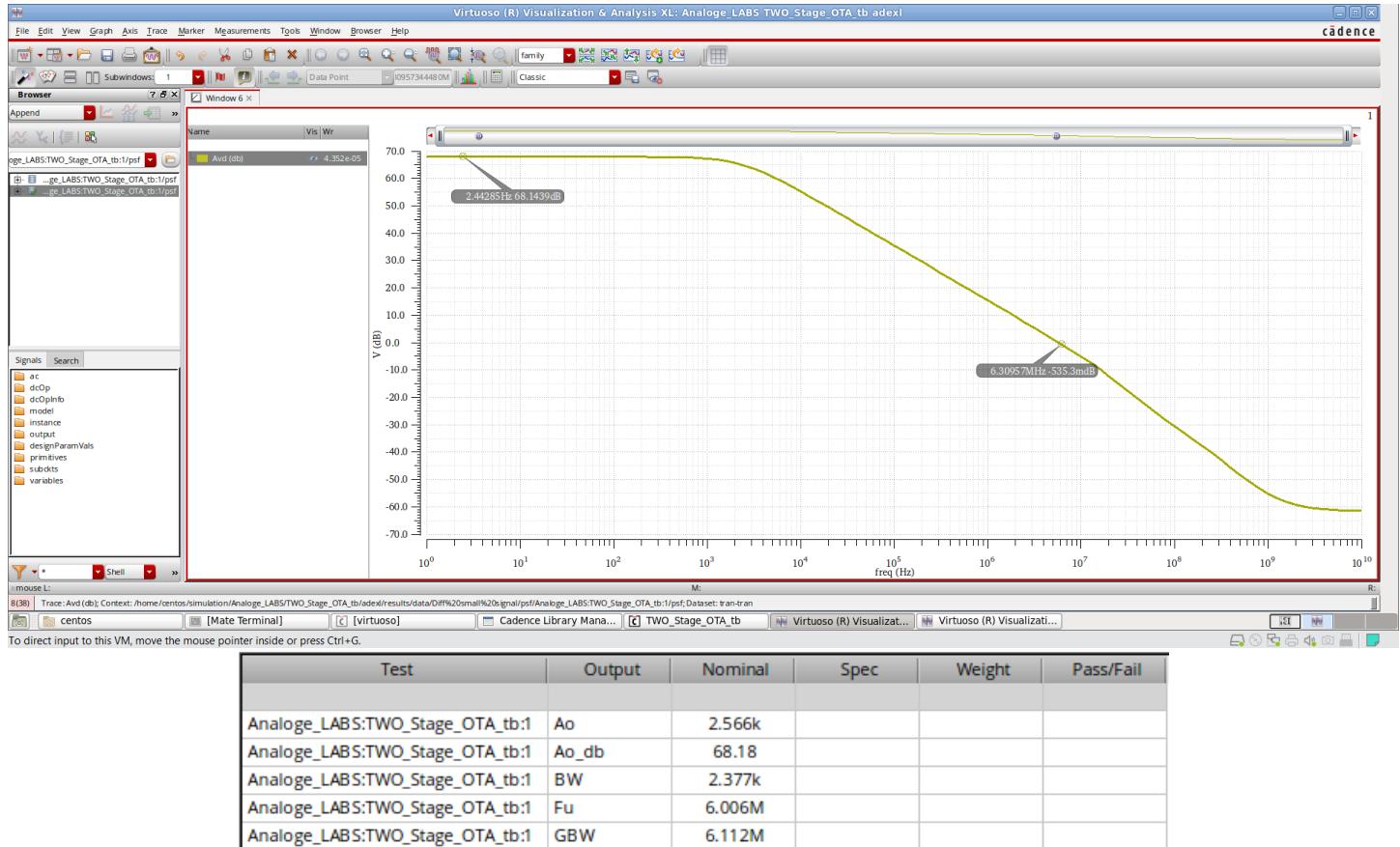
1) Schematic of the OTA and bias circuit with DC node voltages clearly annotated.



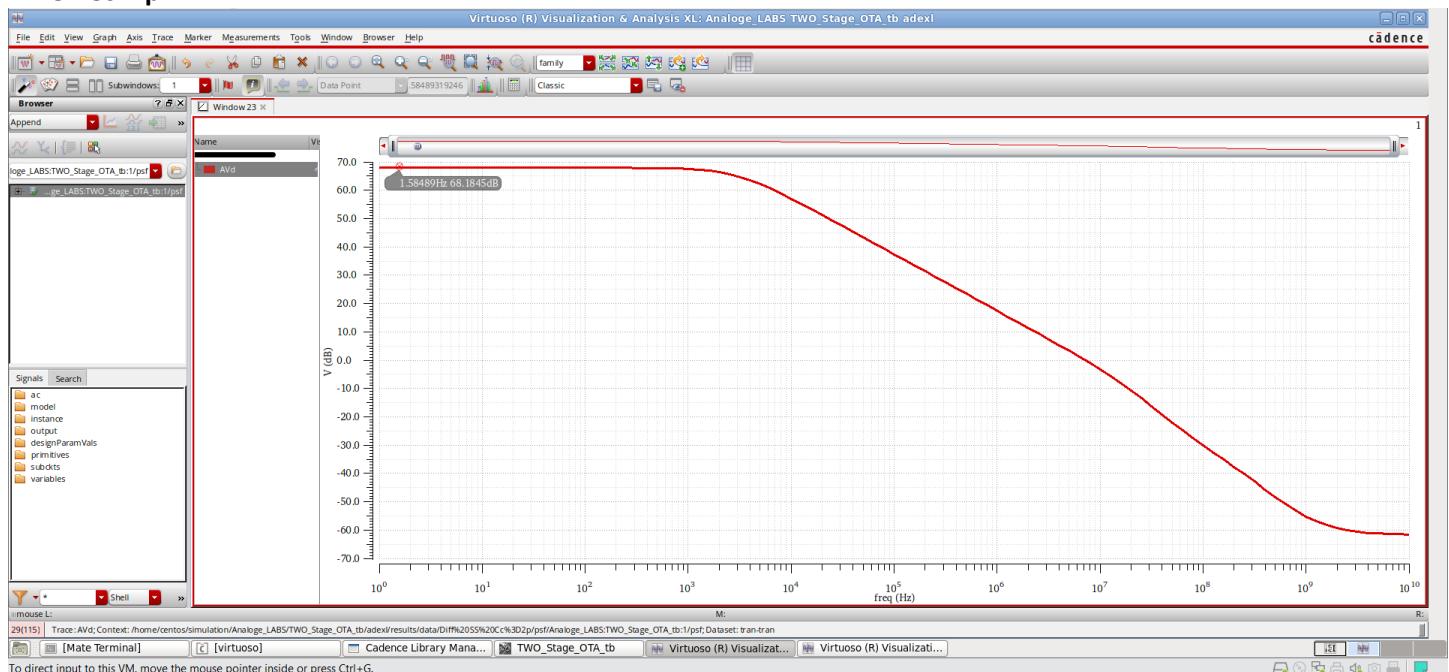
- Use $V_{ICM} = VDD/3$.
- Is the current (and gm) in the input pair exactly equal?
 - ✓ Yes , the gm and ID are exactly equal.
- What is DC voltage at the output of the first stage? Why?
 - ✓ $V_{out1}=680.4\text{mV}$, V_{out1} follow the mirror node.
- What is DC voltage at the output of the second stage? Why?
 - ✓ $V_{out2}=585\text{mV}$, this value is random value as the output node is high impedance node and the OTA not in feedback connection so that not set clearly.

2) Diff small signal ccs:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VIDAC = 1 and VICMAC = 0.
- Use VICK = VDD/3.
- Plot diff gain (in dB) vs frequency.



When Cc=2p:



Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:TWO_Stage OTA_tb:1	Ao	2.566k			
Analoge_LABS:TWO_Stage OTA_tb:1	Ao_db	68.18			
Analoge_LABS:TWO_Stage OTA_tb:1	BW	2.964k			
Analoge_LABS:TWO_Stage OTA_tb:1	FU	7.386M			
Analoge_LABS:TWO_Stage OTA_tb:1	GBW	7.623M			

- Compare simulation results with hand calculations in a table.

✓ $\text{Avd} = A1 * A2 = \frac{gm1,2}{gds1,2 + gds3,4} * \frac{gm6}{gds6 + gds7} = 2.5773 \text{KV/V} = 68.223 \text{db.}$

✓ $\text{BW} = \frac{1}{2\pi Cc * (1+A2) * (ro2||ro4)} = 3.013 \text{KHZ}$, this value is slightly higher than the simulated value as we no include the self-capacitance of the transistors.

✓ $F_u = \frac{gm1,2}{2\pi Cc} = 7.966 \text{MHz.}$

✓ $\text{GBW} = F_u = 7.966 \text{MHz}$

	Hand Analysis	Simulation
Avd	2.577K =68.22db	2.566K =68.18db
BW	3.013KHz	2.964KHz
GBW	7.966MHz	7.623MHz
Fu	7.966MHz	7.386MHz

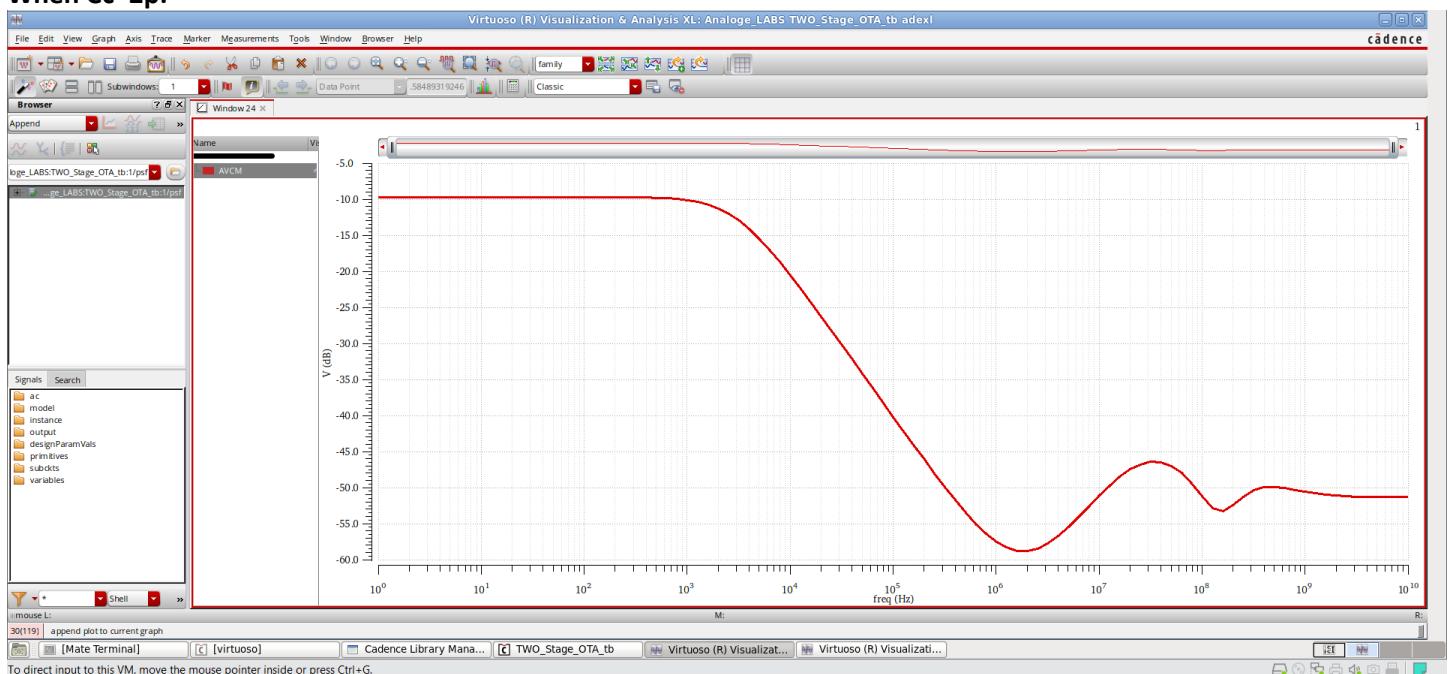
3) CM small signal ccs:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VICMAC = 1 and VIDAC = 0.
- Use VCM = VDD/3.
- Plot CM gain in dB vs frequency.



Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:TWO_Stage_OTA_tb:1	Ao	331.7m			
Analoge_LABS:TWO_Stage_OTA_tb:1	Ao_db	-9.586			
Analoge_LABS:TWO_Stage_OTA_tb:1	BW	2.377k			
Analoge_LABS:TWO_Stage_OTA_tb:1	GBW	790			

When $C_c=2p$:



Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABs:TWO_Stage OTA_tb:1	Ao	331.7m			
Analoge_LABs:TWO_Stage OTA_tb:1	Ao_db	-9.586			
Analoge_LABs:TWO_Stage OTA_tb:1	BW	2.964k			
Analoge_LABs:TWO_Stage OTA_tb:1	GBW	985.4			

- Compare simulation results with hand calculations in a table.

✓ $\text{Avcm} = \frac{gds5}{2gm3,4} * A2 = 339.6 \text{mV/V} = -9.38 \text{db.}$

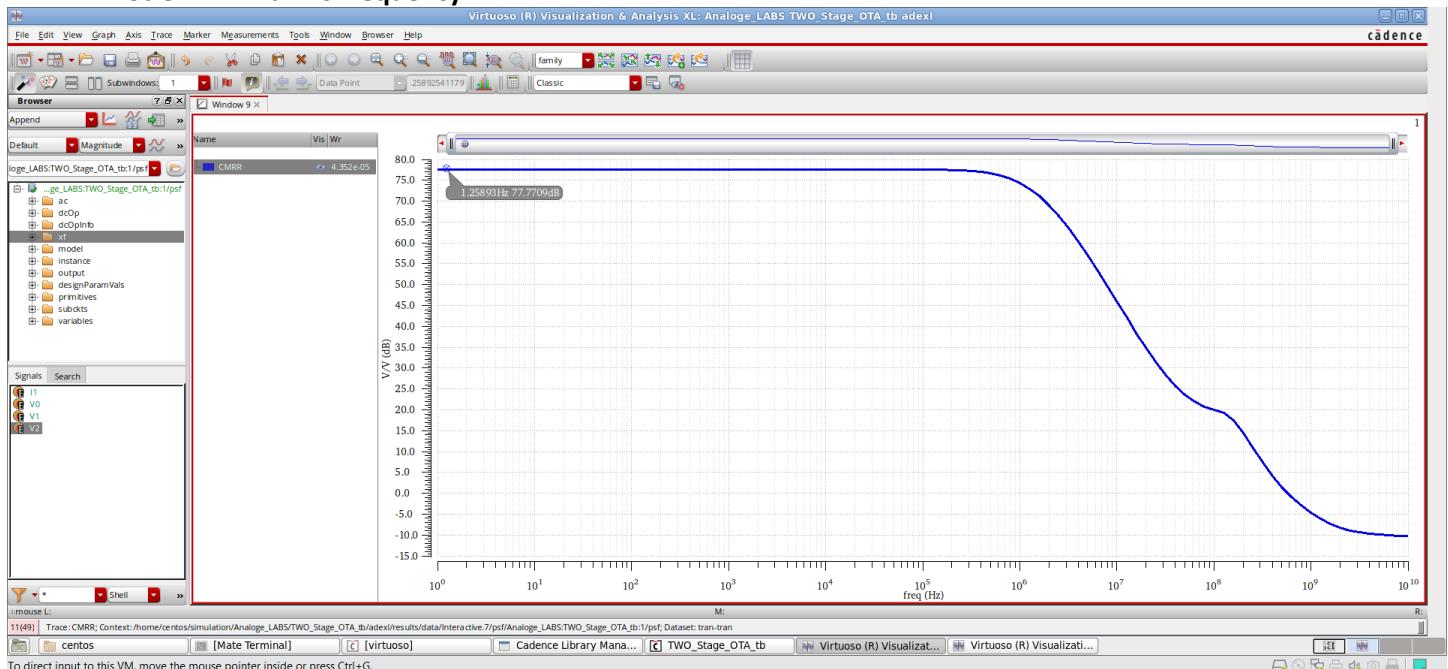
✓ $\text{BW} = \frac{1}{2\pi Cc * (1+A2) * (ro2||ro4)} = 3.013 \text{KHZ.}$

✓ $\text{GBW} = \text{Avcm} * \text{BW} = 1.023 \text{KHz}$

	Hand Analysis	Simulation
Avd	339.6m = -9.38db	331.7m = -9.586db
BW	3.013KHz	2.964KHz
GBW	7.966MHz	985.4MHz

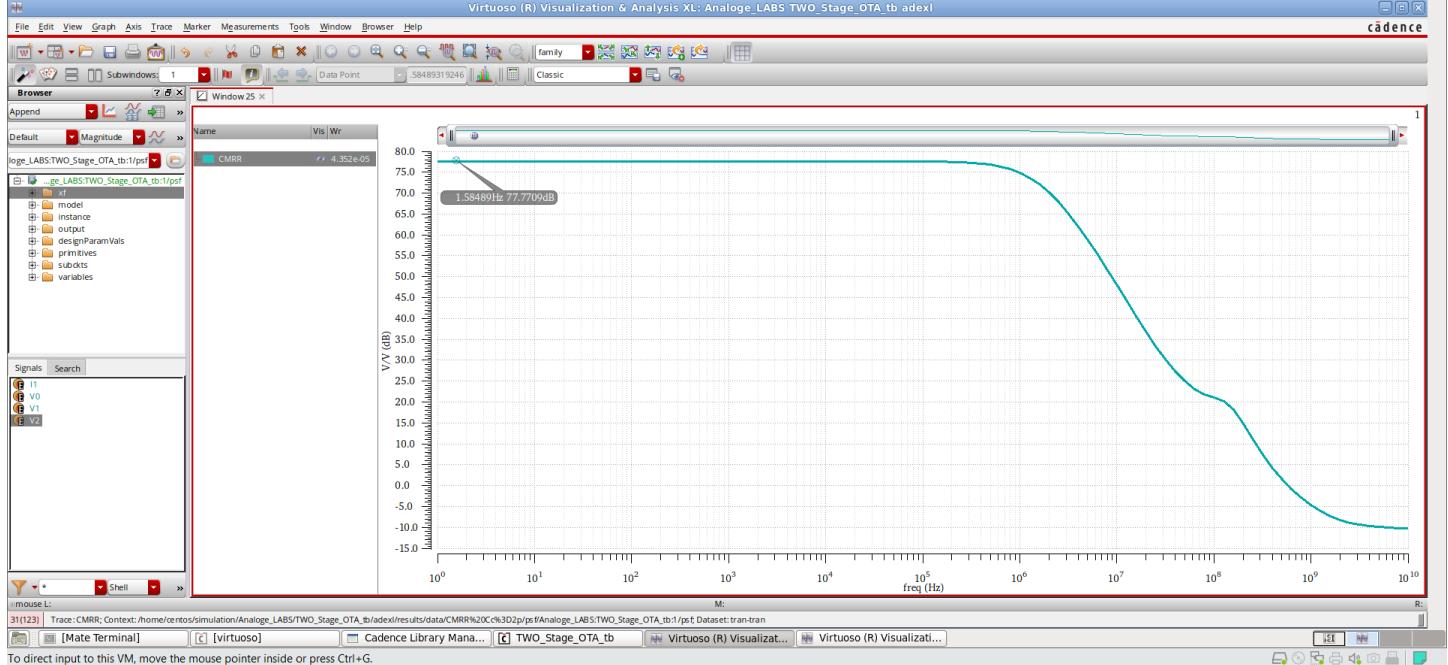
4) (Optional) CMRR:

- Use $V_{CM} = VDD/3$.
- Plot CMRR in dB vs frequency.



To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

When $C_c=2pF$:



To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

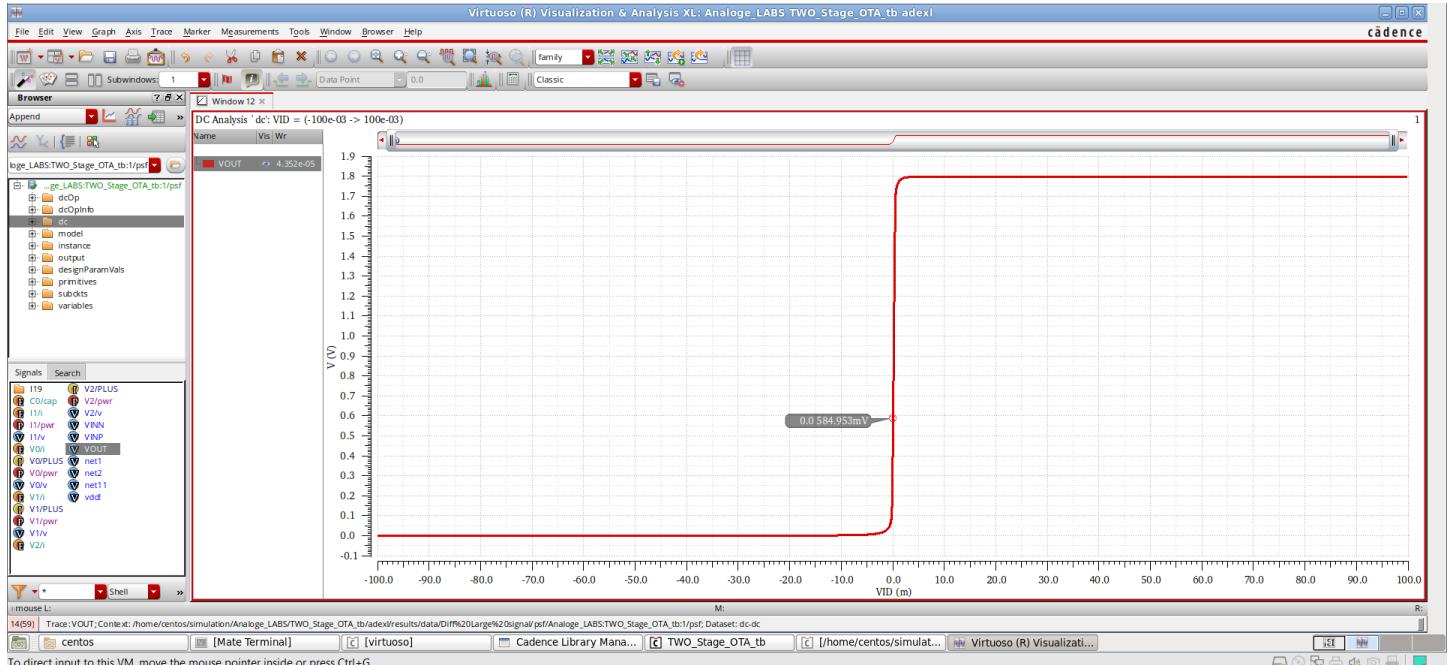
- Compare simulation results with hand calculations in a table.

✓ $CMRR = \frac{A_{vd}}{A_{vcm}} = 7.59K = 77.6\text{db}$.

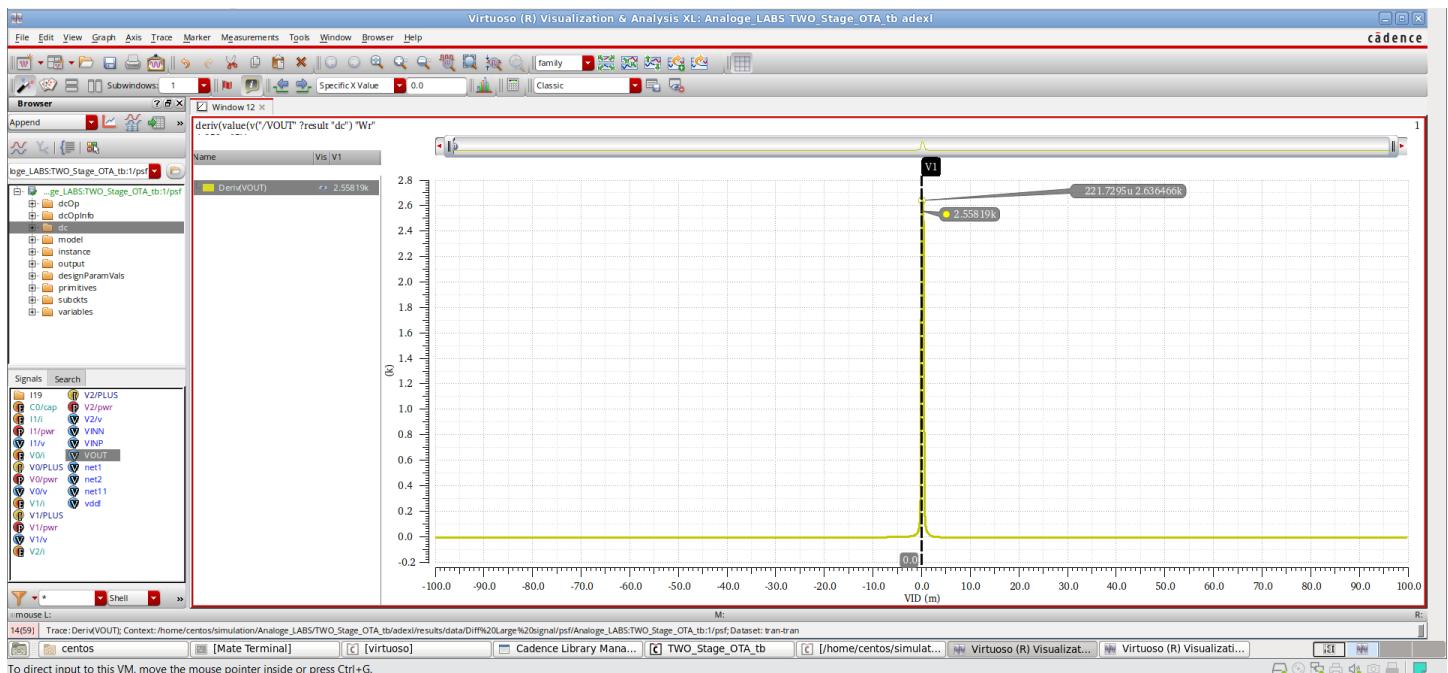
	Hand Analysis	Simulation
CMRR	7.59K = 77.6db	77.77db

5) (Optional) Diff large signal ccs:

- Use VICM = VDD/3.
- Use DC sweep (not parametric sweep) VID = -0.1:1m:0.1. You must use a small step because the gain region is very small (steep slope).
- From the plot, what is the value of Vout at VID = 0. Compare it with the value you obtained in DC OP.
- ✓ Vout=584.953mV at VID=0 , this value is equal to Vout from DC OP (Vout,op=585mV)
- Plot VOUT vs VID.

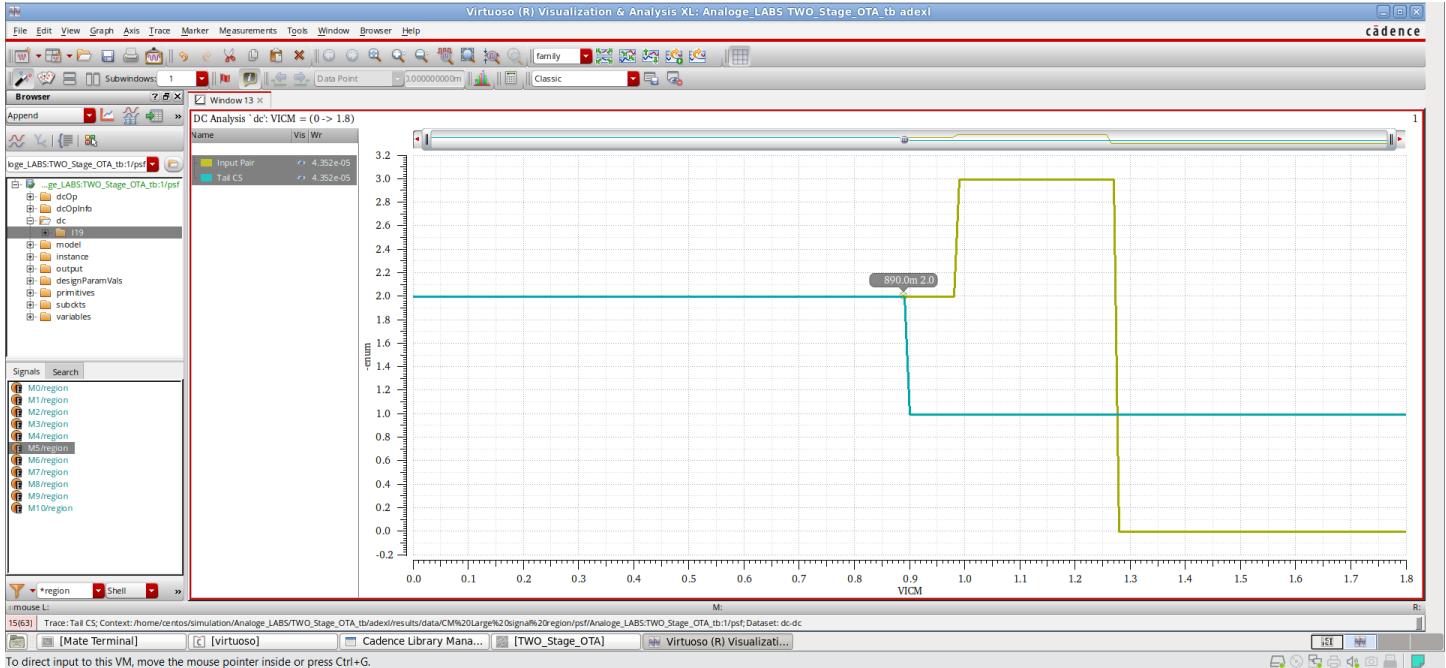


- Plot the derivative of VOUT vs VID. Is the peak less than the value of Avd obtained from ac analysis? Why?
- ✓ $\frac{dV_{out}}{dt} = 2.5582K$ at VID=0 , which is roughly equal to Avd (Avd=2.56K) , but the peak Value equal =2.64K which is higer Avd.



6) CM large signal ccs (region vs VICM):

- Use DC sweep (not parametric sweep) VICM = 0:10m:VDD.
- Plot “region” OP parameter vs VICM for the input pair and the tail current source (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown).



- Plot “region” OP parameter vs VICM for the input pair and the tail current source.
- Find the CM input range (CMIR). Compare with hand analysis in a table.
- ✓ $VGS3,4 - |VGS1,2 - V^*| \leq VICM \leq VDD - V^* 5 - |VGS1,2|$.
- ✓ $-24.98\text{mV} \leq VICM \leq 858.53\text{mV}$.

	Hand Analysis	Simulation
CMIR_Low	-24.98mV	0V
CMIR_High	858.53mV	890mV

7) (Optional) CM large signal ccs (GBW vs VICM):

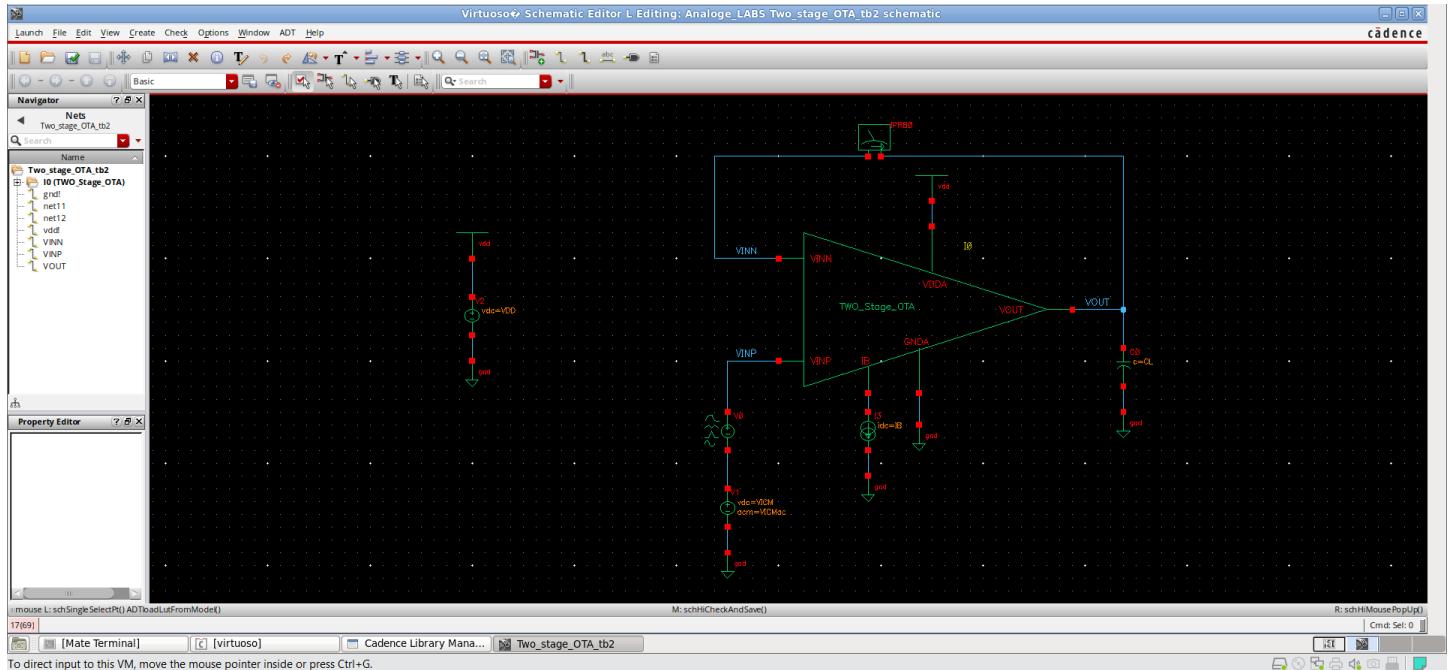
- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VIDAC = 1 and VICMAC = 0.
- Use parametric sweep (not DC sweep) VICM = 0:25m:VDD.
- Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region parameter).



- Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW₃.

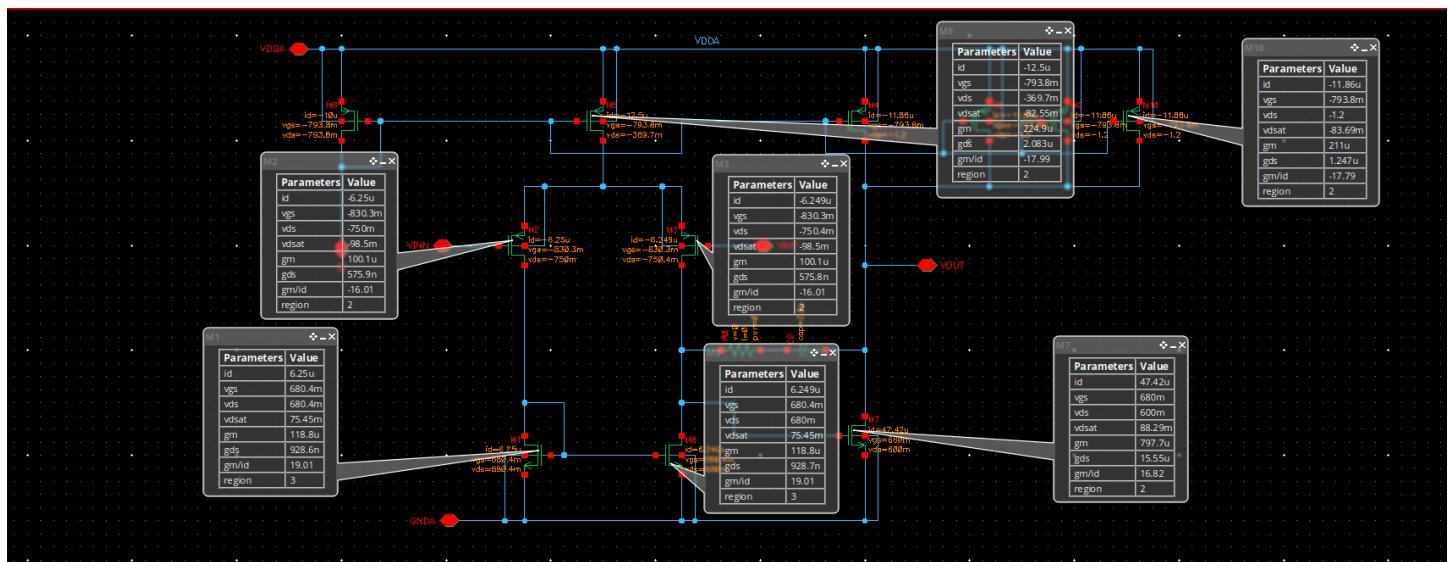
PART 4: Closed-Loop OTA Simulation

Create a new testbench with the OTA connected in a unity gain buffer feedback configuration (the shown schematic is from the 5T OTA lab). Place a current probe (iprobe) or a zero voltage source in the feedback loop.



Report the following:

- 1) Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.

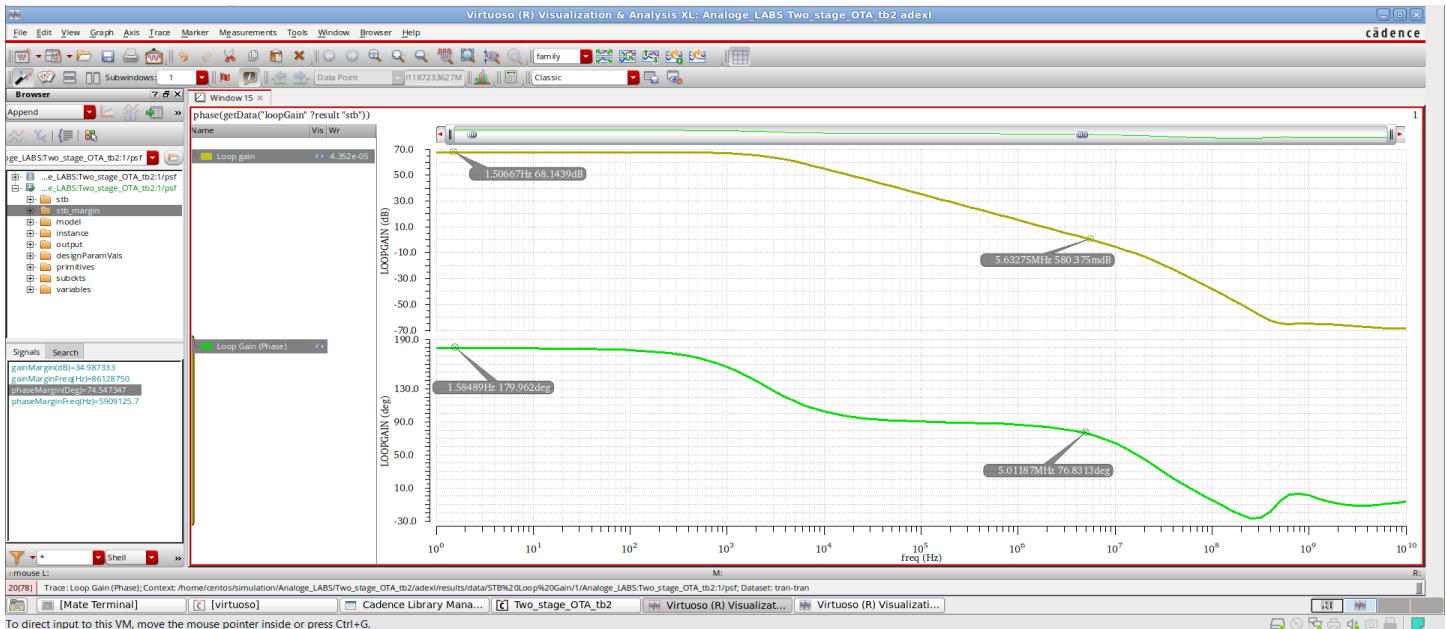


- Use $V_{ICM} = VDD/3$.
- Are the DC voltages at the input terminals of the op-amp exactly equal? Why?
- Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?
- ✓ Yes V_{out1} almost equal the open loop value , there is very small deference due to the error between V_{INN} & V_{INP} , $\Delta V_{out} = 680.4\text{mV} - 680\text{mV} = .4\text{mV}$.

- Is the current (and gm) in the input pair exactly equal? Why?
- ✓ No , due to the very small error signal there is small difference of the Current and gm.
- ✓ $\Delta ID = 6.25 - 6.249 = .01 \mu A = 10 \text{nA}$.

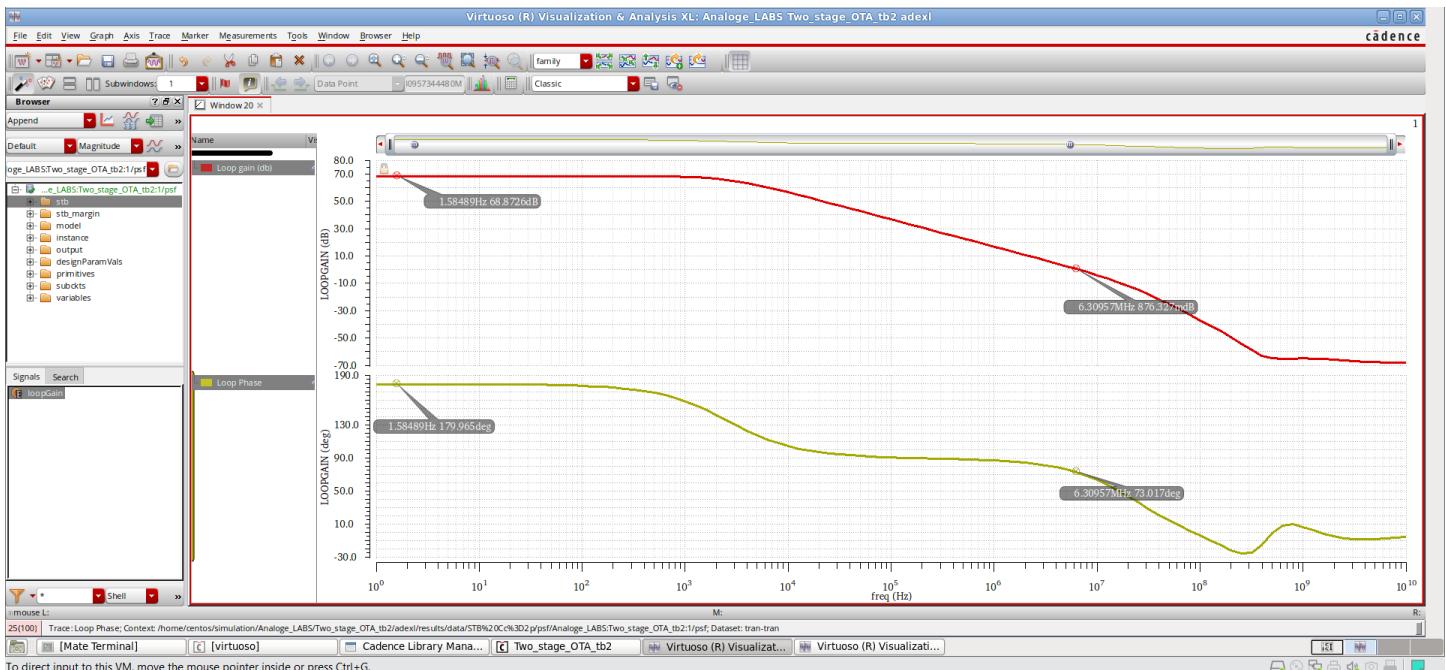
2) Loop gain:

- Use STB analysis (1Hz:10Gz, logarithmic, 10 points/decade) in unity gain buffer configuration.
- Use $V_{ICM} = V_{DD}/3$.
- Plot loop gain in dB and phase vs frequency.



Test	Output	Nominal	Spec	Weight	Pass/Fail
Analogue_LAB5:Two_stage OTA_tb2:1	Ao	2.573k			
Analogue_LAB5:Two_stage OTA_tb2:1	Ao_db	68.21			
Analogue_LAB5:Two_stage OTA_tb2:1	Bw	2.37k			
Analogue_LAB5:Two_stage OTA_tb2:1	FU	5.969M			
Analogue_LAB5:Two_stage OTA_tb2:1	GBW	6.112M			
Analogue_LAB5:Two_stage OTA_tb2:1	PM	74.55			

Loop gain when $C_C=2\text{pF}$.



Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Two_stage_OTA_tb2:1	Ao	2.777k			
Analoge_LABS:Two_stage_OTA_tb2:1	Ao_db	68.87			
Analoge_LABS:Two_stage_OTA_tb2:1	BW	2.611k			
Analoge_LABS:Two_stage_OTA_tb2:1	FU	7.015M			
Analoge_LABS:Two_stage_OTA_tb2:1	GBW	7.269M			
Analoge_LABS:Two_stage_OTA_tb2:1	PM	71.44			

Note that the PM still met the required PM spec.

- Compare DC gain, fu, and GBW with those obtained from open-loop simulation.

	Open Loop	Close Loop
Avd	2.566K =68.18db	2.777K =68.87db
BW	2.964KHz	2.611KHz
GBW	7.623MHz	7.015MHz
Fu	7.386MHz	7.269MHz

Comment:

- ✓ As $\beta=1$ then the Loop gain almost equal the open loop gain.
- Report PM. Compare with hand calculations.
- ✓ As $\frac{Wp2}{Wu} = \frac{GM2*Cc}{GM1*CL} = \frac{797.7u*2P}{100.1*5P} = 3.19$, then $PM \approx 72$ deg.

	Hand Analysis	Simulation
PM	72 deg	71.44 deg

Comment:

As $PM < 76.3$ deg ($Q=0.5$) , then the system is under damped system so that we will see overshoot in the step response.

- Compare simulation results with hand calculations in a table.
- ✓ $\beta=1$
- ✓ $LG = \beta A_{ol} = A1 * A2 = \frac{gm1,2}{gds1,2 + gds3,4} * \frac{gm6}{gds6 + gds7} = 2.584KV/V = 68.25db$.
- ✓ $BW = \frac{1}{2\pi Cc * (1+A2) * (ro2||ro4)} = 3.005KHz$.
- ✓ $GBW = Fu = 7.7549MHz$.

	Hand Analysis	Simulation
DC LG	2.584KV/V =68.25db	2.777K =68.87db
BW	3.005KHz	2.611KHz
GBW	7.7549MHz	7.015MHz

3) Slew rate:

- Apply a step input with the following parameters (delay = 1us, initial value = CMIR-low + 50mV, final value = CMIR-high – 50mV, rise time = 1ns, period = 1s, width = 1s). Note that we want a single step input, which is why we selected very large period and width for the pulse.
- Run transient analysis (stop = 5us and step = 0.1ns).
- Report Vin and Vout overlaid.



- Report the slew rate.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Two_stage OTA_tb2:1	Slew rate	4.301M			

Note that the slew rate is less than the required , so that we will reduce Cc to increase the SR , but this will reduce the phase margin , let Cc=2pF.



Test	Output	Nominal	Spec	Weight	Pass/Fail
Analoge_LABS:Two_stage_OTA_tb2:1	Slew rate	5.23M			

Now the PM and SR specs are met.

- Compare simulation results with hand calculations in a table.

✓ $SR = \frac{IB1}{Cc} = \frac{12.5u}{2p} = 6.25V/\mu S$, this result is less than the simulated value as we not take into account the self-capacitances of the mosfets.

	Hand Analysis	Simulation
SR	6.25V/us	5.23V/uS

4) Settling time:

- Apply a small signal step input with the following parameters (delay = 1us, initial value = VDD/3, final value = VDD/3 + 5mV, rise time = 1ns, period = 1s, width = 1s). Note that we want a single step input, which is why we selected very large period and width for the pulse. Note that we apply a small signal pulse (5mV step) to measure the small signal settling time.



- Calculate the output rise time from simulation.
- Compare simulation results with hand calculations in a table4.

$$\checkmark \text{ Trise} = 2.2\tau = \frac{2.2}{Wu} = \frac{2.2}{2\pi * 7.015 \text{MHz}} = 49.91 \text{nS.}$$

	Hand Analysis	Simulation
Trise	49.91ns	31.71ns

- Do you see any ringing? Why?
 - Yes , there is small overshoot , that is as the system is underdamped ($\text{PM}<76 \text{ deg}$ or $\text{Q}>.5$).