

Spartan6_DSP48A1

Project_1

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Sheet ID: 16

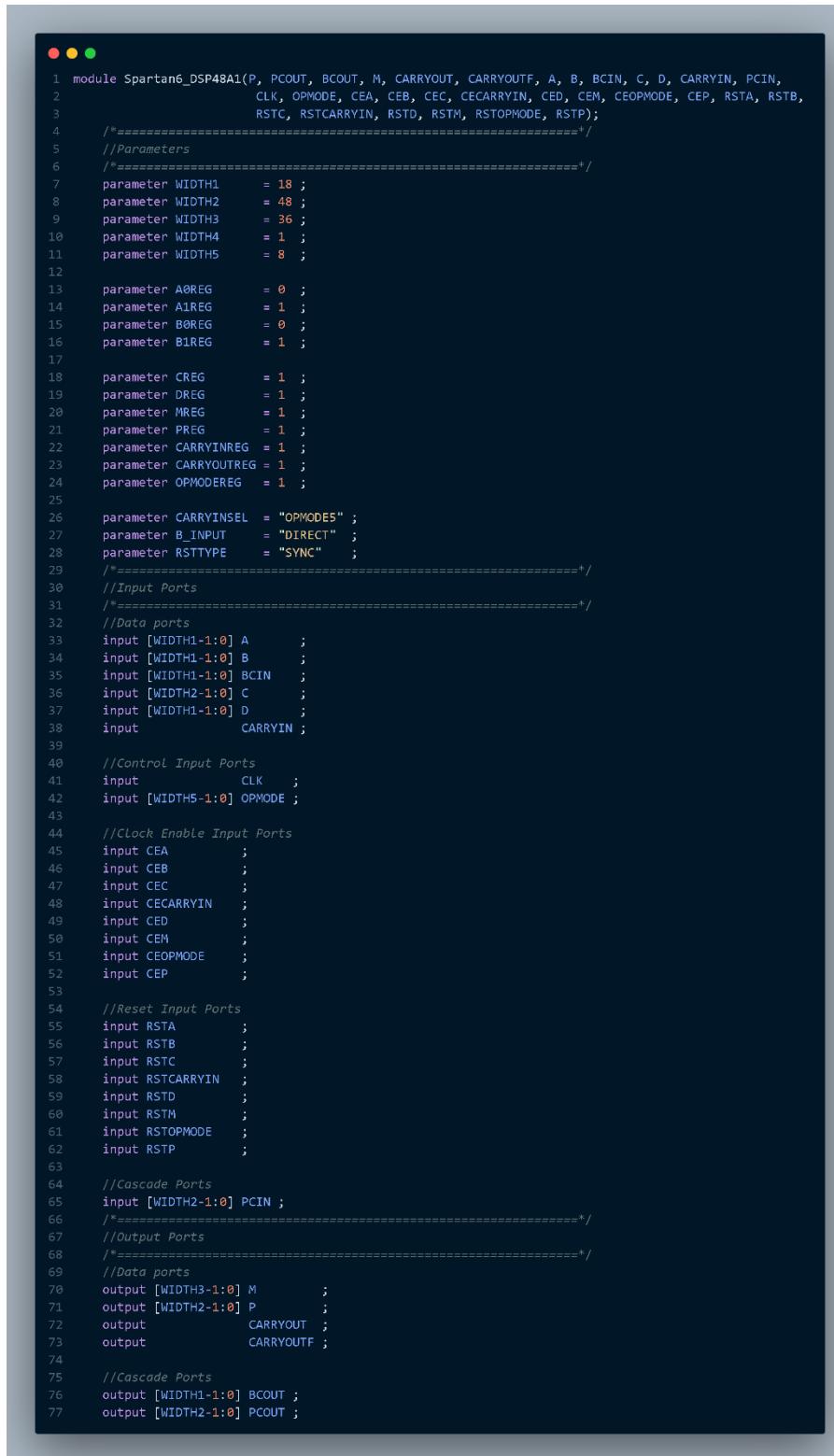
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1. RTL code

Spartan6_DSP48A1



```
1 module Spartan6_DSP48A1(P, PCOUT, BCOUT, M, CARRYOUT, CARRYOUTF, A, B, BCIN, C, D, CARRYIN, PCIN,
2                         CLK, OPMODE, CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, RSTA, RSTB,
3                         RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP);
4 /*=====
5 //Parameters
6 =====*/
7 parameter WIDTH1      = 18 ;
8 parameter WIDTH2      = 48 ;
9 parameter WIDTH3      = 36 ;
10 parameter WIDTH4      = 1 ;
11 parameter WIDTH5      = 8 ;
12
13 parameter A0REG       = 0 ;
14 parameter A1REG       = 1 ;
15 parameter B0REG       = 0 ;
16 parameter B1REG       = 1 ;
17
18 parameter CREG        = 1 ;
19 parameter DREG        = 1 ;
20 parameter MREG        = 1 ;
21 parameter PREG        = 1 ;
22 parameter CARRYINREG = 1 ;
23 parameter CARRYOUTREG = 1 ;
24 parameter OPMODEREG   = 1 ;
25
26 parameter CARRYINSEL  = "OPMODES" ;
27 parameter B_INPUT      = "DIRECT" ;
28 parameter RSTTYPE      = "SYNC" ;
29 /*=====
30 //Input Ports
31 =====*/
32 //Data ports
33 input [WIDTH1-1:0] A      ;
34 input [WIDTH1-1:0] B      ;
35 input [WIDTH1-1:0] BCIN   ;
36 input [WIDTH2-1:0] C      ;
37 input [WIDTH1-1:0] D      ;
38 input                CARRYIN ;
39
40 //Control Input Ports
41 input                CLK    ;
42 input [WIDTH5-1:0] OPMODE ;
43
44 //Clock Enable Input Ports
45 input CEA           ;
46 input CEB           ;
47 input CEC           ;
48 input CECARRYIN    ;
49 input CED           ;
50 input CEM           ;
51 input CEOPMODE     ;
52 input CEP           ;
53
54 //Reset Input Ports
55 input RSTA          ;
56 input RSTB          ;
57 input RSTC          ;
58 input RSTCARRYIN   ;
59 input RSTD          ;
60 input RSTM          ;
61 input RSTOPMODE    ;
62 input RSTP          ;
63
64 //Cascade Ports
65 input [WIDTH2-1:0] PCIN ;
66 /*=====
67 //Output Ports
68 =====*/
69 //Data ports
70 output [WIDTH3-1:0] M      ;
71 output [WIDTH2-1:0] P      ;
72 output                CARRYOUT ;
73 output                CARRYOUTF ;
74
75 //Cascade Ports
76 output [WIDTH1-1:0] BCOUT ;
77 output [WIDTH2-1:0] PCOUT ;
```

```

1  /*=====
2  //input pre stage
3  =====*/
4  wire [WIDTH1-1:0] D_reg ;
5  wire [WIDTH1-1:0] A0_reg ;
6  wire [WIDTH1-1:0] B0_reg ;
7  wire [WIDTH1-1:0] BOUT ;
8  wire [WIDTH2-1:0] C_reg ;
9  wire [WIDTH5-1:0] OPMODE_reg ;
10
11 mux_b_bcin #(.B_INPUT(B_INPUT)) mux_B (BOUT, B, BCIN);
12
13 mux_reg_18bits_parameter #( .Reg_state(B0REG), .rst_state(RSTTYPE), .width_reg(WIDTH1))
14 B0_RegM (.out_mux_reg(B0_reg), .in(B), .clk(CLK), .clKE(CEB), .rst(RSTB));
15
16 mux_reg_18bits_parameter #( .Reg_state(A0REG), .rst_state(RSTTYPE), .width_reg(WIDTH1))
17 A0_RegM (.out_mux_reg(A0_reg), .in(A), .clk(CLK), .clKE(CEA), .rst(RSTA));
18
19 mux_reg_18bits_parameter #( .Reg_state(DREG), .rst_state(RSTTYPE), .width_reg(WIDTH1))
20 D_RegM (.out_mux_reg(D_reg), .in(D), .clk(CLK), .clKE(CED), .rst(RSTD));
21
22 mux_reg_18bits_parameter #( .Reg_state(CREG), .rst_state(RSTTYPE), .width_reg(WIDTH2))
23 C_RegM (.out_mux_reg(C_reg), .in(C), .clk(CLK), .clKE(CEC), .rst(RSTC));
24
25 mux_reg_18bits_parameter #( .Reg_state(OPMODEREG), .rst_state(RSTTYPE), .width_reg(WIDTH5))
26 OPMODE_RegM (.out_mux_reg(OPMODE_reg), .in(OPMODE), .clk(CLK), .clKE(CEOPMODE), .rst(RSTOPMODE));
27
28 //pre operator stage
29
30 wire [WIDTH1-1:0] pre_operator ;
31 wire [WIDTH1-1:0] B1_reg ;
32 wire [WIDTH1-1:0] A1_reg ;
33
34 mux_pre_add_sub #(.width_add_sub(WIDTH1))
35 pre_add_sub (.out(pre_operator), .ini(D_reg), .in2(B0_reg), .OPMODE_pre(OPMODE_reg[8]), .OPMODE_mux(OPMODE_reg[4]));
36
37 mux_reg_18bits_parameter #( .Reg_state(B1REG), .rst_state(RSTTYPE), .width_reg(WIDTH1))
38 B1_RegM (.out_mux_reg(B1_reg), .in(pre_operator), .clk(CLK), .clKE(CEB), .rst(RSTB));
39
40 mux_reg_18bits_parameter #( .Reg_state(A1REG), .rst_state(RSTTYPE), .width_reg(WIDTH1))
41 A1_RegM (.out_mux_reg(A1_reg), .in(A0_reg), .clk(CLK), .clKE(CEA), .rst(RSTA));
42
43 //Multiplication stage
44
45 wire [WIDTH3-1:0] M_pre_reg ;
46
47 assign BCOUT = B1_reg;
48
49 multiplier #(.width_mult_in(WIDTH1))
50 multi1 (.out(M_pre_reg), .ini(B1_reg), .in2(A1_reg));
51
52 mux_reg_18bits_parameter #( .Reg_state(MREG), .rst_state(RSTTYPE), .width_reg(WIDTH3))
53 M_RegM (.out_mux_reg(M), .in(M_pre_reg), .clk(CLK), .clKE(CEM), .rst(RSTM));
54
55 //Carry In
56
57 wire cin ;
58 wire cin_reg ;
59
60 mux_carry_cascade_in #(.CARRY_IN_SEL(CARRYINSEL))
61 carry_cascade (.out(cin), .OPmode5(OPMODE_reg[5]), .carryIN(CARRYIN));
62
63 mux_reg_18bits_parameter #( .Reg_state(CARRYINREG), .rst_state(RSTTYPE), .width_reg(WIDTH4))
64 CYI (.out_mux_reg(cin_reg), .in(cin), .clk(CLK), .clKE(CECARRYIN), .rst(RSTCARRYIN));
65
66 //X-Z multiplexers
67
68 wire [WIDTH2-1:0] x_out ;
69 wire [WIDTH2-1:0] z_out ;
70
71 mux_3to1_x_z
72 X_3to1_mux (.out(x_out), .in0({12'b0,M}), .in1(PCOUT), .in2({D_reg[11:0],A1_reg,B1_reg}), .opmode_2bits(OPMODE_reg[1:0]));
73
74 mux_3to1_x_z
75 Z_3to1_mux (.out(z_out), .in0(PCIN), .in1(PCOUT), .in2(C_reg), .opmode_2bits(OPMODE_reg[3:2]));
76
77 //post operator stage
78
79 wire [WIDTH2-1:0] post_operator ;
80 wire cout ;
81
82 mux_post_add_sub #(.width_add_sub(WIDTH2))
83 post_add_sub (.out(post_operator), .cout(cout), .ini(x_out), .in2(z_out), .cin(cin_reg), .OPMODE_post(OPMODE_reg[7]));
84
85 //Carry Out
86
87 mux_reg_18bits_parameter #( .Reg_state(CARRYOUTREG), .rst_state(RSTTYPE), .width_reg(WIDTH4))
88 CYO (.out_mux_reg(CARRYOUT), .in(cout), .clk(CLK), .clKE(CECARRYIN), .rst(RSTCARRYIN));
89 assign CARRYOUTF = CARRYOUT;
90
91 //P output
92
93 mux_reg_18bits_parameter #( .Reg_state(PREG), .rst_state(RSTTYPE), .width_reg(WIDTH2))
94 P_RegM (.out_mux_reg(P), .in(post_operator), .clk(CLK), .clKE(CEP), .rst(RSTP));
95 assign PCOUT = P;
96 endmodule

```

Multiplier

```
● ● ●  
1 module multiplier(out, in1, in2);  
2     parameter width_mult_in = 18;  
3     localparam width_mult_out = 2 * width_mult_in;  
4  
5     input [width_mult_in-1:0] in1;  
6     input [width_mult_in-1:0] in2;  
7  
8     output [width_mult_out-1:0] out;  
9  
10    assign out = in1 * in2;  
11 endmodule
```

mux_3to1_x_z

```
● ● ●
1 module mux_3to1_x_z(out, in0, in1, in2, opmode_2bits);
2     input [47:0] in0;
3     input [47:0] in1;
4     input [47:0] in2;
5     input [1:0] opmode_2bits;
6
7     output [47:0] out;
8
9     assign out = (opmode_2bits == 0)? 0:
10                  (opmode_2bits == 1)? in0:
11                  (opmode_2bits == 2)? in1:
12                  in2;
13 endmodule
```

mux_b_bcin

```
● ● ●  
1 module mux_b_bcin(BOUT, B, BCIN);  
2     parameter B_INPUT = "DIRECT";  
3  
4     input [17:0] BCIN;  
5     input [17:0] B;  
6  
7     output [17:0] BOUT;  
8  
9     assign BOUT = (B_INPUT == "DIRECT")? B : BCIN;  
10  
11 endmodule
```

mux_carry_cascade_in

```
● ● ●
1 module mux_carry_cascade_in(out, OPmode5, carryIN);
2   parameter CARRY_IN_SEL = "OPMODE5";
3
4   input carryIN ;
5   input OPmode5 ;
6
7   output out      ;
8
9   assign out = (CARRY_IN_SEL == "OPMODE5")? OPmode5: (CARRY_IN_SEL == "CARRYIN")? carryIN: 0;
10
11 endmodule
```

mux_post_add_sub

```
● ● ●
1 module mux_post_add_sub(out, cout, in1, in2, cin, OPMODE_post);
2   parameter width_add_sub = 48;
3
4   input [width_add_sub-1:0] in1;
5   input [width_add_sub-1:0] in2;
6   input cin ;
7   input OPMODE_post ;
8
9   output [width_add_sub-1:0] out;
10  output cout;
11
12  assign {cout,out} = (OPMODE_post == 0)? (in1 + in2 + cin) : (in2 - (in1 + cin));
13
14 endmodule
```

mux_pre_add_sub

```
● ● ●
1 module mux_pre_add_sub(out, in1, in2, OPMODE_pre, OPMODE_mux);
2     parameter width_add_sub = 18;
3
4     input [width_add_sub-1:0] in1;
5     input [width_add_sub-1:0] in2;
6     input OPMODE_pre ;
7     input OPMODE_mux ;
8
9     output [width_add_sub-1:0] out;
10
11    wire [width_add_sub-1:0] pre_out;
12
13    assign pre_out = (OPMODE_pre == 0)? (in1 + in2) : (in1 - in2);
14    assign out = (OPMODE_mux == 1)? pre_out : in2;
15 endmodule
```

mux_reg_18bits_parameter

```
● ● ●
1 module mux_reg_18bits_parameter(out_mux_reg, in, clk, clkE, rst);
2   parameter Reg_state = "1"      ;
3   parameter rst_state = "SYNC"   ;
4   parameter width_reg = 18     ;
5
6   input [width_reg - 1:0] in ;
7   input clk                  ;
8   input clkE                 ;
9   input rst                  ;
10
11  output [width_reg - 1:0] out_mux_reg ;
12
13 generate
14   if (rst_state == "SYNC") begin
15     mux_reg_18bits_sync #(Reg_state(Reg_state), .width_reg(width_reg))
16     mux_reg_18bits (.out_mux_reg(out_mux_reg), .in(in), .clk(clk), .clkE(clkE), .rst(rst));
17   end
18   else begin
19     mux_reg_18bits_async #(Reg_state(Reg_state), .width_reg(width_reg))
20     mux_reg_18bits (.out_mux_reg(out_mux_reg), .in(in), .clk(clk), .clkE(clkE), .rst(rst));
21   end
22 endgenerate
23 endmodule
```

mux_reg_18bits_async

```
● ● ●

1 module mux_reg_18bits_async(out_mux_reg, in, clk, clkE, rst);
2     parameter Reg_state = "1"      ;
3     parameter width_reg = 18      ;
4
5     input [width_reg - 1:0] in      ;
6     input clk                  ;
7     input clkE                 ;
8     input rst                  ;
9
10    output [width_reg - 1:0] out_mux_reg ;
11    reg [width_reg - 1:0] out_reg ;
12
13
14    assign out_mux_reg = (Reg_state == 1)? out_reg : in;
15
16    always @(posedge clk or posedge rst) begin
17        if(rst)begin
18            out_reg <= 0;
19        end
20        else if(clkE) begin
21            out_reg <= in;
22        end
23
24    end
25 endmodule
```

mux_reg_18bits_sync

```
● ● ●
1 module mux_reg_18bits_sync(out_mux_reg, in, clk, clkE, rst);
2     parameter Reg_state = "1"      ;
3     parameter width_reg = 18      ;
4
5     input [width_reg - 1:0] in ;
6     input clk                  ;
7     input clkE                 ;
8     input rst                  ;
9
10    output [width_reg - 1:0] out_mux_reg ;
11    reg [width_reg - 1:0] out_reg ;
12
13
14    assign out_mux_reg = (Reg_state == 1)? out_reg : in;
15
16    always @(posedge clk) begin
17        if(clkE)begin
18            if(rst)begin
19                out_reg <= 0;
20            end
21            else begin
22                out_reg <= in;
23            end
24        end
25    end
26 endmodule
```

2. Testbench code

```
● ● ●
1 module Spartan6_DSP48A1_tb();
2 //=====
3 //Parameters
4 //=====
5 // Parameters
6 parameter WIDTH1 = 18;
7 parameter WIDTH2 = 48;
8 parameter WIDTH3 = 36;
9 parameter WIDTH5 = 8;
10 //=====
11 //Input Ports
12 //=====
13 reg [WIDTH1-1:0] A, B, BCIN, D;
14 reg [WIDTH2-1:0] C, PCIN;
15 reg CARRYIN;
16 reg CLK;
17 reg [WIDTH5-1:0] OPMODE;
18 reg CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;
19 reg RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;
20 //=====
21 //Output Ports
22 //=====
23 wire [WIDTH3-1:0] M;
24 wire [WIDTH2-1:0] P, PCOUT;
25 wire [WIDTH1-1:0] BCOUT;
26 wire CARRYOUT, CARRYOUTF;
27 //=====
28 // Instantiate the DUT
29 //=====
30 Spartan6_DSP48A1 #(
31     .A0REG(0), .AIREG(1), .B0REG(0), .B1REG(1), .CREG(1), .DREG(1),
32     .IREG(1), .PREG(1), .CARRYINREG(1), .CARRYOUTREG(1), .OPMODEREG(1),
33     .CARRYINSEL("OPMODES"), .B_INPUT("DIRECT"), .RSTTYPE("SYNC")
34 ) dut (
35     .A(A), .B(B), .BCIN(BCIN), .C(C), .D(D), .CARRYIN(CARRYIN), .PCIN(PCIN),
36     .CLK(CLK), .OPMODE(OPMODE), .CEA(CEA), .CEB(CEB), .CEC(CEC),
37     .CECARRYIN(CECARRYIN), .CED(CED), .CEM(CEM), .CEOPMODE(CEOPMODE), .CEP(CEP),
38     .RSTA(RSTA), .RSTB(RSTB), .RSTC(RSTC), .RSTCARRYIN(RSTCARRYIN),
39     .RSTD(RSTD), .RSTM(RSTM), .RSTOPMODE(RSTOPMODE), .RSTP(RSTP),
40     .M(M), .P(P), .PCOUT(PCOUT), .BCOUT(BCOUT), .CARRYOUT(CARRYOUT), .CARRYOUTF(CARRYOUTF)
41 );
42 //=====
43 // Clock
44 //=====
45 initial begin
46     CLK = 0;
47     forever begin
48         #1 CLK = ~CLK;
49     end
50 end
51 //=====
52 // Stimulus Generation
53 initial begin
54     // Reset Test
55     //=====
56     // Reset Test
57     //=====
58     A = 0; B = 0; BCIN = 0; C = 0; D = 0; CARRYIN = 0; PCIN = 0; OPMODE = 0;
59     CEA = 0; CEB = 0; CEC = 0; CECARRYIN = 0; CED = 0; CEM = 0; CEOPMODE = 0; CEP = 0;
60     RSTA = 0; RSTB = 0; RSTC = 0; RSTCARRYIN = 0; RSTD = 0; RSTM = 0; RSTOPMODE = 0; RSTP = 0;
61     #5;
62     RSTA = 1; RSTB = 1; RSTC = 1; RSTCARRYIN = 1; RSTD = 1; RSTM = 1; RSTOPMODE = 1; RSTP = 1;
63     CEA = 1; CEB = 1; CEC = 1; CECARRYIN = 1; CED = 1; CEM = 1; CEOPMODE = 1; CEP = 1;
64     #3;
65     repeat(10)begin
66         A = $random; B = $random; BCIN = $random; C = $random; D = $random; CARRYIN = $random; PCIN = $random; OPMODE = $random;
67         CEA = $random; CEB = $random; CEC = $random; CECARRYIN = $random; CED = $random; CEM = $random; CEOPMODE = $random; CEP = $random;
68         @(negedge CLK);
69         if (M != 0 || P != 0 || PCOUT != 0 || BCOUT != 0 || CARRYOUT != 0 || CARRYOUTF != 0) begin
70             $display("Error in reset: M: %d, P: %d, PCOUT: %d, BCOUT: %d, CARRYOUT: %d, CARRYOUTF: %d"
71             , M, P, PCOUT, BCOUT, CARRYOUT, CARRYOUTF);
72             $stop;
73         end
74     end
75     RSTA = 0; RSTB = 0; RSTC = 0; RSTCARRYIN = 0; RSTD = 0; RSTM = 0; RSTOPMODE = 0; RSTP = 0;
76     CEA = 1; CEB = 1; CEC = 1; CECARRYIN = 1; CED = 1; CEM = 1; CEOPMODE = 1; CEP = 1;
77     #5;
```

```
1      /*=====
2      // DSP path 1
3      /*=====
4      OPMODE = 8'b11011101;
5      A = 20; B = 10; C = 350; D = 25;
6      BCIN = $random; PCIN = $random; CARRYIN = $random;
7      @(negedge CLK);
8      @(negedge CLK);
9      @(negedge CLK);
10     @(negedge CLK);
11     if(BCOUT !== 18'hf || M !== 36'h12c || P !== 48'h32 || PCOUT !== 48'h32 || CARRYOUT !== 0 || CARRYOUTF !== 0)begin
12         $display("Error in DSP path 1: BCOUT: %h, M: %h, P: %h, PCOUT: %h, CARRYOUT: %h, CARRYOUTF: %h"
13         , BCOUT, M, P, PCOUT, CARRYOUT, CARRYOUTF);
14         $stop;
15     end
16     #5;
17     /*=====
18     // DSP path 2
19     /*=====
20     OPMODE = 8'b000010000;
21     A = 20; B = 10; C = 350; D = 25;
22     BCIN = $random; PCIN = $random; CARRYIN = $random;
23     @(negedge CLK);
24     @(negedge CLK);
25     @(negedge CLK);
26     if(BCOUT !== 18'h23 || M !== 36'h2bc || P !== 48'h0 || PCOUT !== 48'h0 || CARRYOUT !== 0 || CARRYOUTF !== 0)begin
27         $display("Error in DSP path 2: BCOUT: %h, M: %h, P: %h, PCOUT: %h, CARRYOUT: %h, CARRYOUTF: %h"
28         , BCOUT, M, P, PCOUT, CARRYOUT, CARRYOUTF);
29         $stop;
30     end
31     #5;
32     /*=====
33     // DSP path 3
34     /*=====
35     OPMODE = 8'b00001010;
36     A = 20; B = 10; C = 350; D = 25;
37     BCIN = $random; PCIN = $random; CARRYIN = $random;
38     @(negedge CLK);
39     @(negedge CLK);
40     @(negedge CLK);
41     if(BCOUT !== 18'ha || M !== 36'hc8 || P !== PCOUT || CARRYOUT !== CARRYOUTF)begin
42         $display("Error in DSP path 3: BCOUT: %h, M: %h, P: %h, PCOUT: %h, CARRYOUT: %h, CARRYOUTF: %h"
43         , BCOUT, M, P, PCOUT, CARRYOUT, CARRYOUTF);
44         $stop;
45     end
46     #5;
47     /*=====
48     // DSP path 4
49     /*=====
50     OPMODE = 8'b10100111;
51     A = 5; B = 6; C = 350; D = 25; PCIN = 3000;
52     BCIN = $random; CARRYIN = $random;
53     @(negedge CLK);
54     @(negedge CLK);
55     @(negedge CLK);
56     if(BCOUT !== 18'h6 || M !== 36'h1e || P !== 48'hfe6ffffec0bb1 || PCOUT !== 48'hfe6ffffec0bb1 || CARRYOUT !== 1 || CARRYOUTF !== 1)begin
57         $display("Error in DSP path 4: BCOUT: %h, M: %h, P: %h, PCOUT: %h, CARRYOUT: %h, CARRYOUTF: %h"
58         , BCOUT, M, P, PCOUT, CARRYOUT, CARRYOUTF);
59         $stop;
60     end
61     $display("Test Done");
62     $finish;
63   end
64 endmodule
```

3. Do file

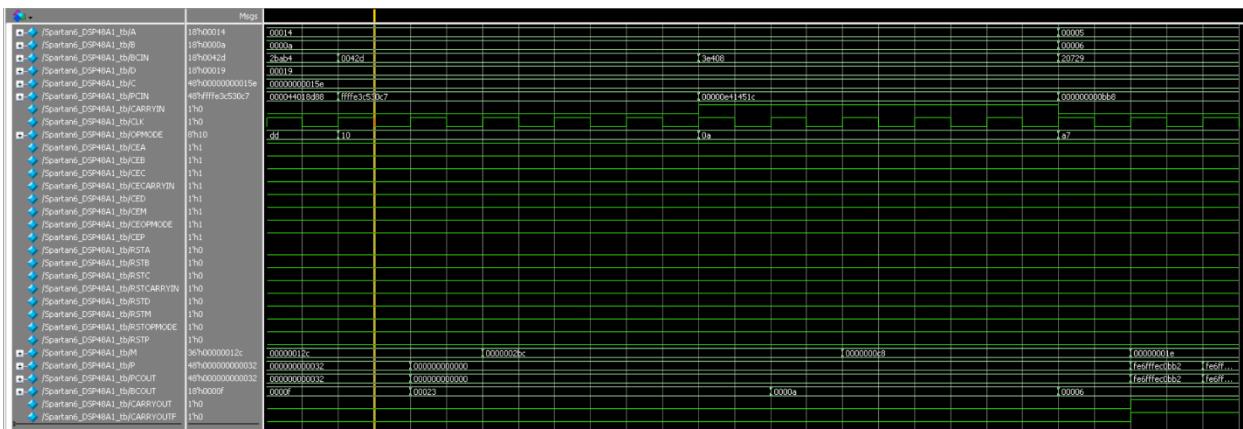
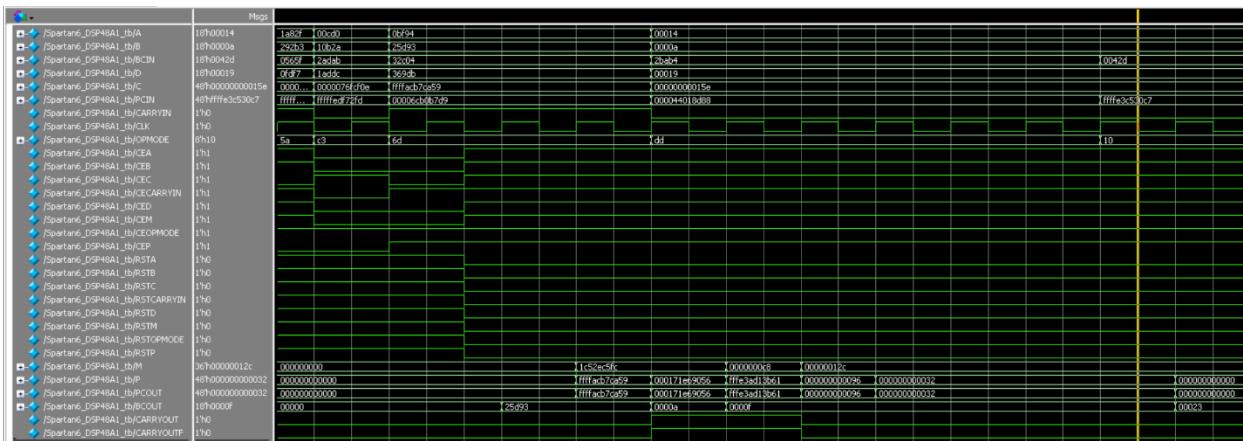
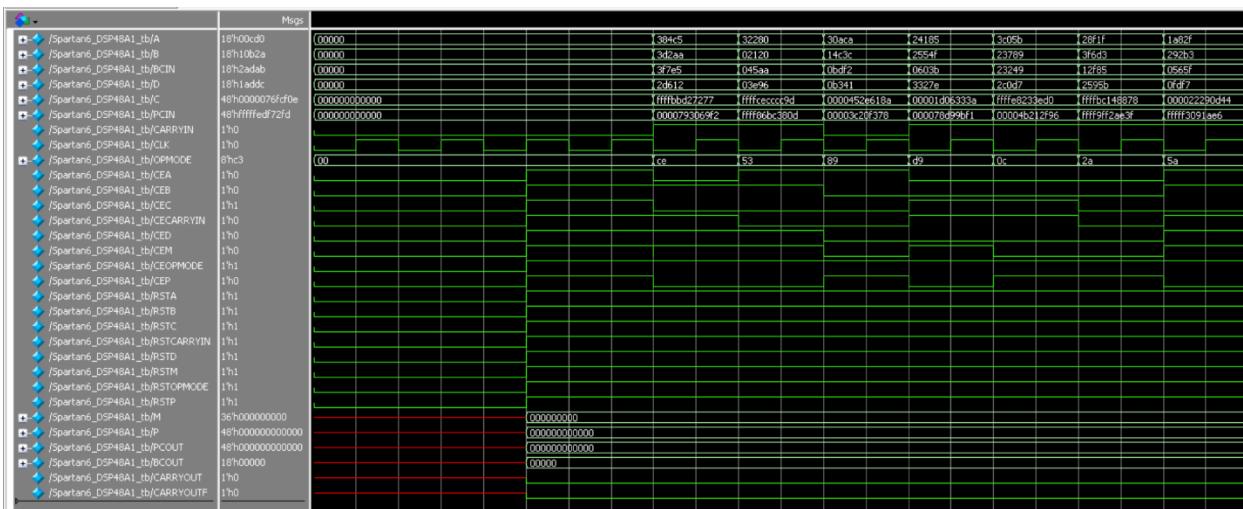
```
1 vlib work
2 vlog -work work Spartan6_DSP48A1.v mux_reg_18bits_async.v mux_reg_18bits_sync.v mux_reg_18bits_parameter.v mux_pre_add_sub.v mux_post_add_sub.v mux_cascade_in.v mux_b_bcin.v mux_3tol_x_z.v multiplier.v Spartan6_DSP48A1_tb.v
3 vsim -voptargs+=acc work.Spartan6_DSP48A1_tb
4 add wave *
5 run -all
6 #quit -sim
7
```

4. QuestaSim Snippets

Messages

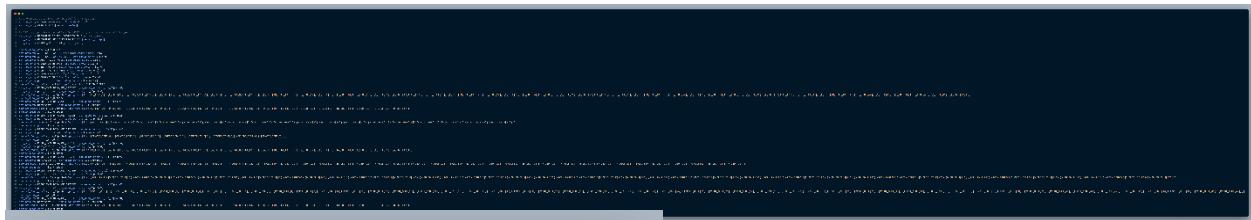
```
#-----#
# vsim -voptargs="+acc" work.Spartan6_DSP48A1_tb
# Start time: 03:16:18 on Jul 28,2025
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading work.Spartan6_DSP48A1_tb(fast)
# Loading work.Spartan6_DSP48A1(fast)
# Loading work.mux_b_bcin(fast)
# Loading work.mux_reg_18bits_parameter(fast)
# Loading work.mux_reg_18bits_sync(fast)
# Loading work.mux_reg_18bits_parameter(fast_1)
# Loading work.mux_reg_18bits_sync(fast_1)
# Loading work.mux_reg_18bits_parameter(fast_2)
# Loading work.mux_reg_18bits_sync(fast_2)
# Loading work.mux_reg_18bits_parameter(fast_3)
# Loading work.mux_reg_18bits_sync(fast_3)
# Loading work.mux_pre_add_sub(fast)
# Loading work.multiplier(fast)
# Loading work.mux_reg_18bits_parameter(fast_4)
# Loading work.mux_reg_18bits_sync(fast_4)
# Loading work.mux_cascade_in(fast)
# Loading work.mux_reg_18bits_parameter(fast_5)
# Loading work.mux_reg_18bits_sync(fast_5)
# Loading work.mux_3tol_x_z(fast)
# Loading work.mux_post_add_sub(fast)
# Test Done
# ** Note: $finish    : Spartan6_DSP48A1_tb.v(140)
#      Time: 68 ns Iteration: 1 Instance: /Spartan6_DSP48A1_tb
..
```

Waveform



5. Constraint File

```
6  # Clock signal
7  set_property -dict { PACKAGE_PIN W5  IOSTANDARD LVCMOS33 } [get_ports CLK]
8  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
```



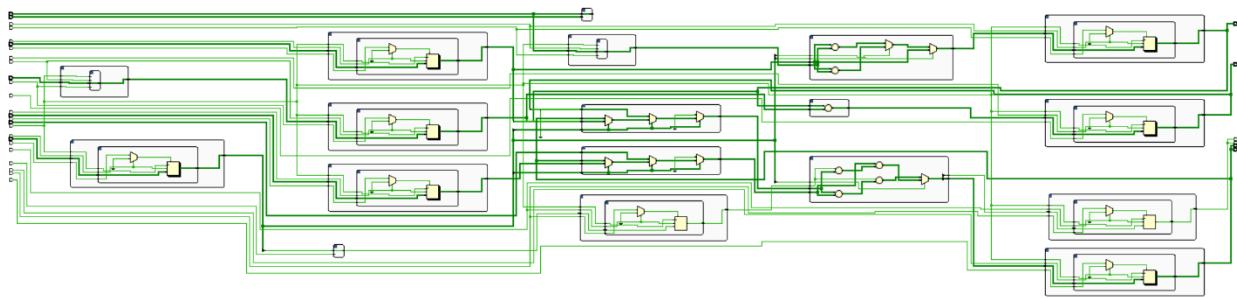
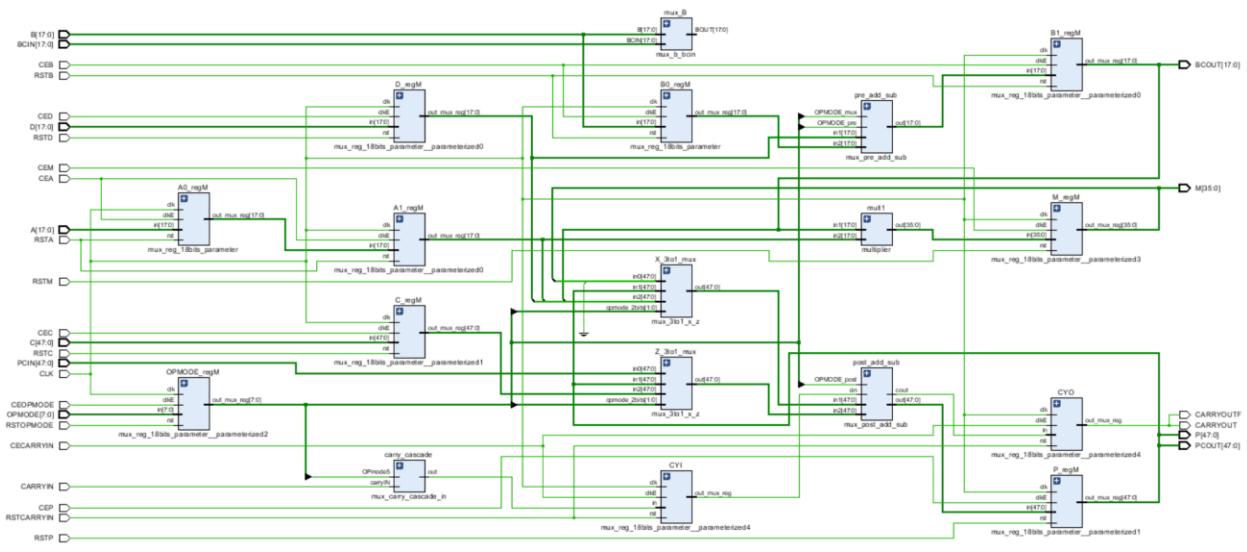
```
1  set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
2  set_property port_width 1 [get_debug_ports u_ila_0/probe11]
3  connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
4  create_debug_port u_ila_0 probe
5  set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
6  set_property port_width 1 [get_debug_ports u_ila_0/probe12]
7  connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
8  create_debug_port u_ila_0 probe
9  set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
10 set_property port_width 1 [get_debug_ports u_ila_0/probe13]
11 connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
12 create_debug_port u_ila_0 probe
13 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
14 set_property port_width 1 [get_debug_ports u_ila_0/probe14]
15 connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
16 create_debug_port u_ila_0 probe
17 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
18 set_property port_width 1 [get_debug_ports u_ila_0/probe15]
19 connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
20 create_debug_port u_ila_0 probe
21 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
22 set_property port_width 1 [get_debug_ports u_ila_0/probe16]
23 connect_debug_port u_ila_0/probe16 [get_nets [list CEOPMODE_IBUF]]
24 create_debug_port u_ila_0 probe
25 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
26 set_property port_width 1 [get_debug_ports u_ila_0/probe17]
27 connect_debug_port u_ila_0/probe17 [get_nets [list CEP_IBUF]]
28 create_debug_port u_ila_0 probe
29 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
30 set_property port_width 1 [get_debug_ports u_ila_0/probe18]
31 connect_debug_port u_ila_0/probe18 [get_nets [list CLK_IBUF]]
32 create_debug_port u_ila_0 probe
33 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
34 set_property port_width 1 [get_debug_ports u_ila_0/probe19]
35 connect_debug_port u_ila_0/probe19 [get_nets [list RSTA_IBUF]]
36 create_debug_port u_ila_0 probe
37 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
38 set_property port_width 1 [get_debug_ports u_ila_0/probe20]
39 connect_debug_port u_ila_0/probe20 [get_nets [list RSTB_IBUF]]
40 create_debug_port u_ila_0 probe
41 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
42 set_property port_width 1 [get_debug_ports u_ila_0/probe21]
43 connect_debug_port u_ila_0/probe21 [get_nets [list RSTC_IBUF]]
44 create_debug_port u_ila_0 probe
45 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
46 set_property port_width 1 [get_debug_ports u_ila_0/probe22]
47 connect_debug_port u_ila_0/probe22 [get_nets [list RSTCARRYIN_IBUF]]
48 create_debug_port u_ila_0 probe
49 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
50 set_property port_width 1 [get_debug_ports u_ila_0/probe23]
51 connect_debug_port u_ila_0/probe23 [get_nets [list RSTD_IBUF]]
52 create_debug_port u_ila_0 probe
53 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
54 set_property port_width 1 [get_debug_ports u_ila_0/probe24]
55 connect_debug_port u_ila_0/probe24 [get_nets [list RSTM_IBUF]]
56 create_debug_port u_ila_0 probe
57 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
58 set_property port_width 1 [get_debug_ports u_ila_0/probe25]
59 connect_debug_port u_ila_0/probe25 [get_nets [list RSTOPMODE_IBUF]]
60 create_debug_port u_ila_0 probe
61 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
62 set_property port_width 1 [get_debug_ports u_ila_0/probe26]
63 connect_debug_port u_ila_0/probe26 [get_nets [list RSTP_IBUF]]
64 set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
65 set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
66 set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
67 connect_debug_port dbg_hub/clk [get_nets CLK_IBUF_BUFG]
68
```

6. Elaboration

Message Tab

- ▼ Vivado Commands (3 infos)
 - ▼ General Messages (3 infos)
 - ⓘ [IP_Flow 19-234] Refreshing IP repositories
 - ⓘ [IP_Flow 19-1704] No user IP repositories specified
 - ⓘ [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Prg/Vivado/Vivado/2018.2/data/ip'.
- ▼ Elaborated Design (2 infos)
 - ▼ General Messages (2 infos)
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Schematic



7. Synthesis

Messages tab

Synthesis (42 warnings, 56 infos)

- Common 17-349 Got license for feature 'Synthesis' and/or device xc7a200t
- [Synth 8-6157] synthesizing module 'Spartan6_DSP48A1' [[Spartan6_DSP48A1.v1](#)] (18 more like this)
- [Synth 8-6155] done synthesizing module 'mux_b_bcin'(#1) [[mux_b_bcin.v1](#)] (18 more like this)
- [Synth 8-3331] design mux_carry_cascade_in has unconnected port carryIN (40 more like this)
- [Device 21-403] Loading part xc7a200tffg1156-3
- [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/other/Courses/Kareem_waseem_Digital-Design/Projects/Project_1/Synthesis/constraint/Constraints_basys3 - Copy.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [XILISpartan6_DSP48A1_propImpl.xdc]
- Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [[mux_pre_add_sub.v1](#)] (1 more like this)
- [Synth 8-5842] Cannot pack DSP OPMode registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [[multiplier.v1](#)]
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 207 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital-Design/Projects/Project_1/Synthesis/p1/project_1/runs/synth_1/Spartan6_DSP48A1.dcp has been generated.
- [runcl-4] Executing: report_utilization -file Spartan6_DSP48A1_utilization_synth.rpt -pb Spartan6_DSP48A1_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Mon Jul 28 03:50:39 2025..

Synthesized Design (6 infos)

- [Netlist 29-17] Analyzing 207 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

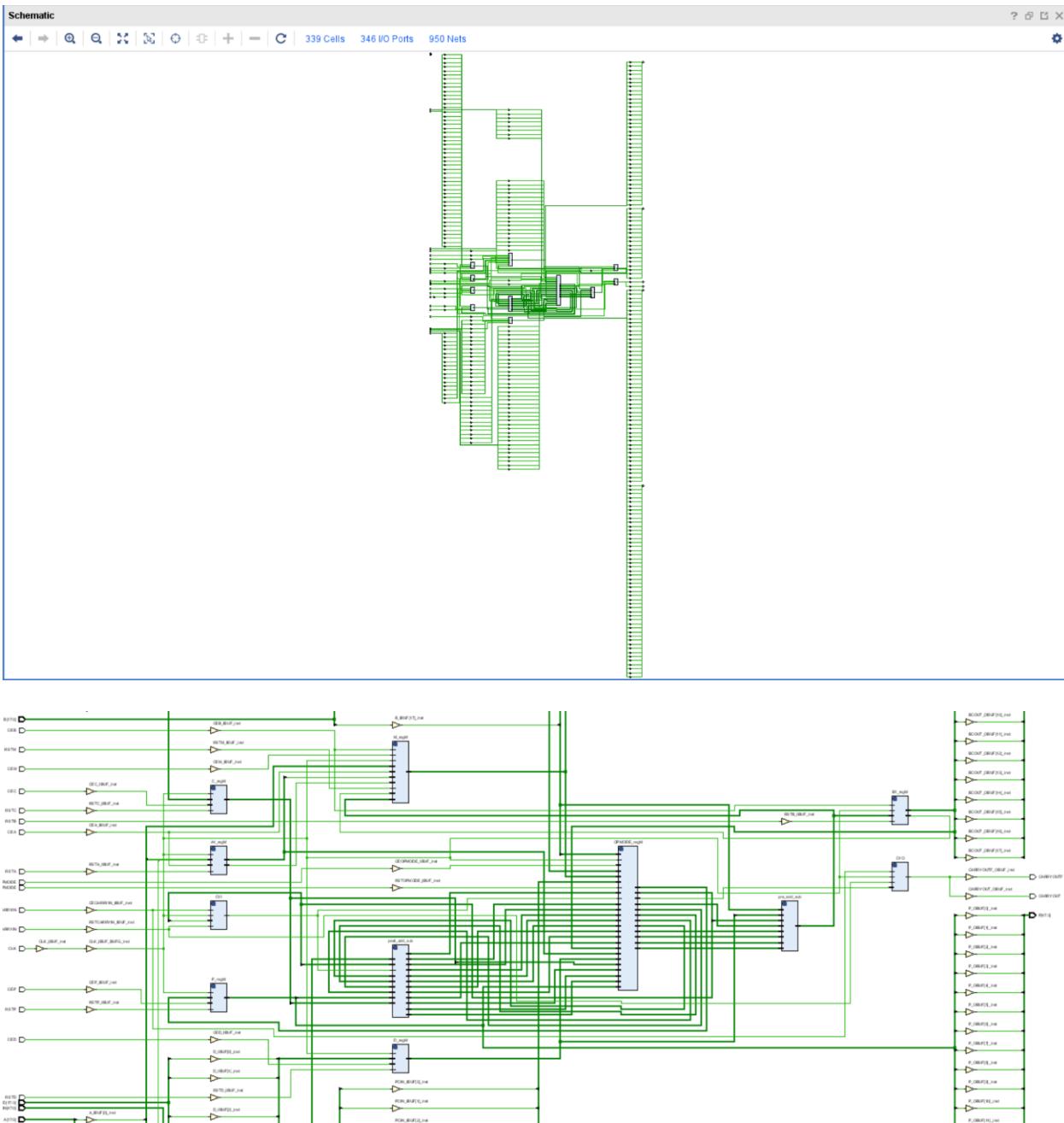
Utilization report

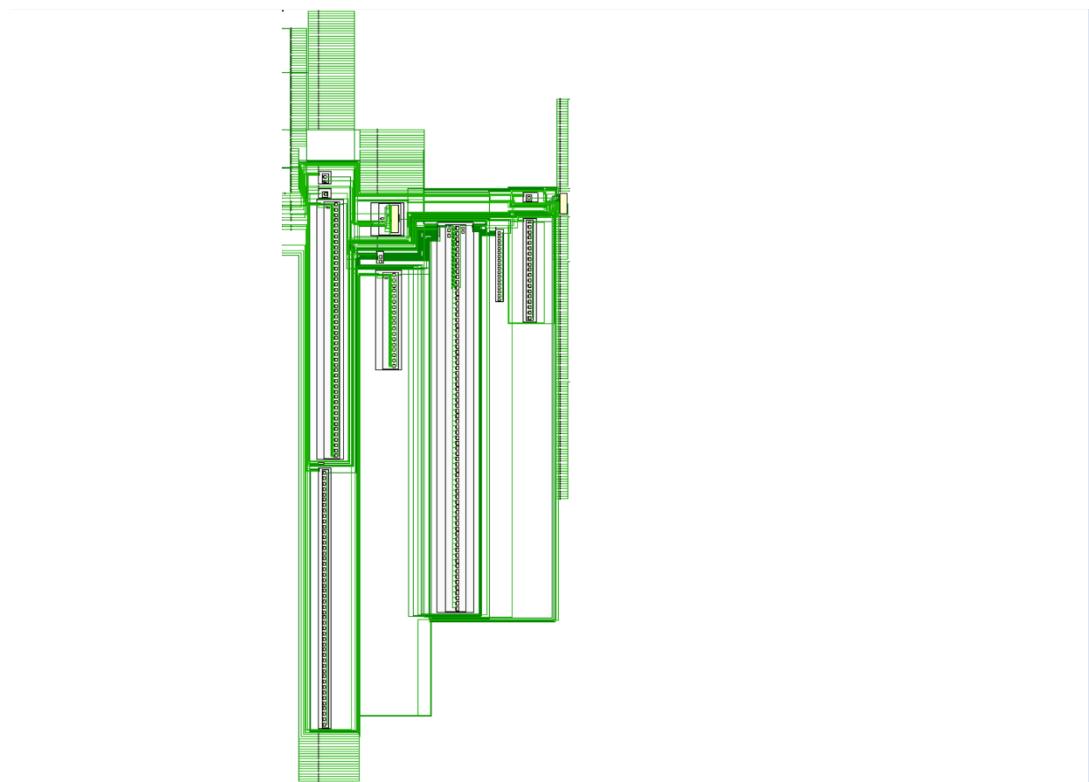
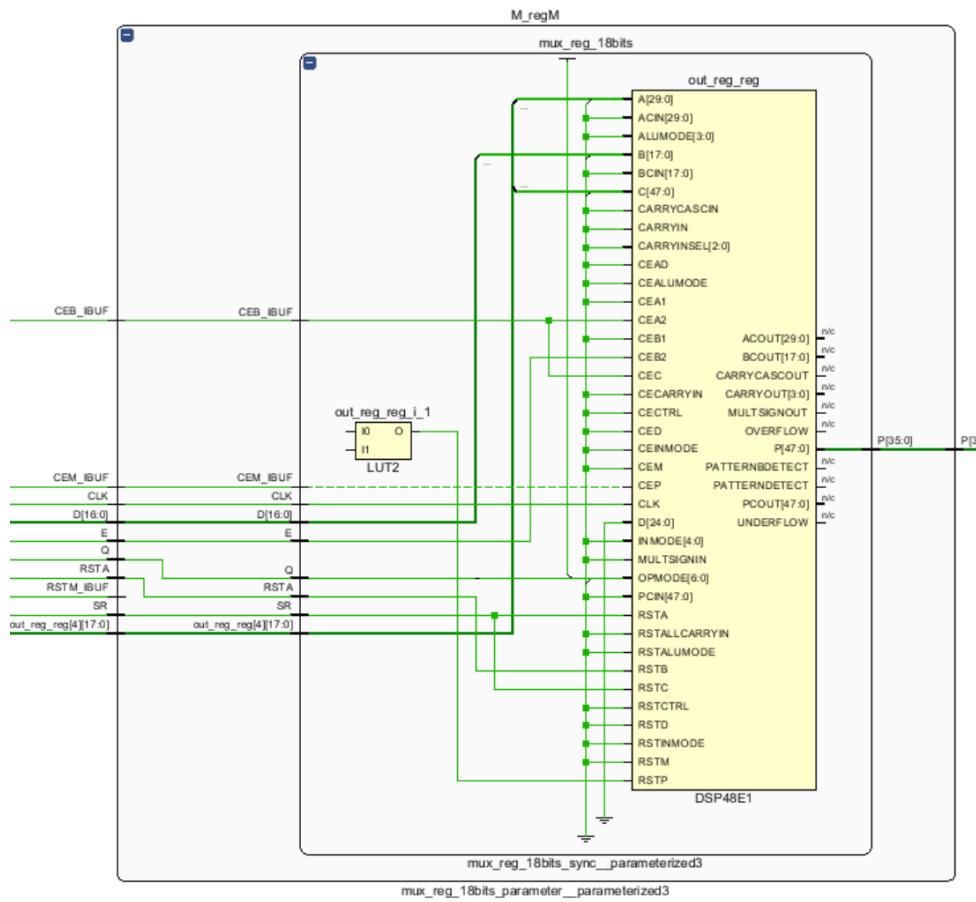
Hierarchy						
	Name	Slice LUTs (134600)	Slice Registers (269200)	DSP s (740)	Bonded IOB (500)	BUFGCTRL (32)
Summary	N Spartan6_DSP48A1	226	160	1	327	1
Slice Logic						
Slice LUTs (<1%)	A1_regM (mux_reg_18...	1	18	0	0	0
LUT as Logic (<1%)	B1_regM (mux_reg_18...	1	18	0	0	0
Slice Registers (<1%)	C1_regM (mux_reg_18b...	1	48	0	0	0
Register as Flip Flop (<1%)	CYI (mux_reg_18bits_...	1	1	0	0	0
Memory	CYO (mux_reg_18bits_...	1	1	0	0	0
DSP	D1_regM (mux_reg_18b...	1	18	0	0	0
DSPs (<1%)	E1_regM (mux_reg_18b...	1	0	1	0	0
DSP48E1 only	M1_regM (mux_reg_18b...	1	8	0	0	0
IO and GT Specific	OPMODE_regM (mux_...	187	0	0	0	0
Bonded IOB (65%)	P1_regM (mux_reg_18b...	1	48	0	0	0
IOB Master Pads	post_add_sub (mux_p...	48	0	0	0	0
Clocking	pre_add_sub (mux_pr...	19	0	0	0	0
BUFGCTRL (3%)						

timing report

Design Timing Summary						
General Information		Setup		Hold		
Timer Settings		Worst Negative Slack (WNS): 5.516 ns			Worst Hold Slack (WHS): 0.227 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Design Timing Summary		Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Clock Summary (1)		Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:
Check Timing (326)		Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:
Intra-Clock Paths	All user specified timing constraints are met.					
Inter-Clock Paths						
Other Path Groups						
User Ignored Paths						
Unconstrained Paths						

Schematic





8. Implementation

Message tab

The screenshot shows the 'Messages' tab in the Vivado IDE. The log is organized into sections corresponding to different phases of the implementation process:

- Implementation (2 warnings, 102 infos)**
 - Design Initialization (7 infos)**
 - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a200fg1156-3
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - Opt Design (35 infos)**
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
 - [Project 1-461] DRC finished with 0 Errors
 - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Prg/Vivado/Vivado/2018.2/data/ip'.
 - [Chipscope 16-329] Generating Script for core instance _dbg_hub (1 more like this)
 - [IP_Flow 19-3806] Processing IP xilinx.com:ip:xsdbm:3.0 for cell dbg_hub_CV. (1 more like this)
 - [Opt 31-49] Retargeted 0 cell(s).
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
 - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
 - [Opt 31-662] Phase BLIFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
 - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
 - [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
 - [Pwropt 34-9] Applying IDT optimizations ...
 - [Pwropt 34-10] Applying ODC optimizations ...
 - [Physopt 32-619] Estimated Timing Summary | WNS=4.870 | TNS=0.000 |
 - [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 8 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.
 - [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-138] The checkpoint 'D:/other/Courses/Kareem_waseem_Digital-Design/Projects/Project_1/Synthesis/p1/project_1/project_1_runs/impl_1/Spartan6_DSP48A1_opt.dcp' has been generated.
 - [runctd-4] Executing : report_drc -file Spartan6_DSP48A1_drc_opted.rpt -pb Spartan6_DSP48A1_drc_opted.pb -rpx Spartan6_DSP48A1_drc_opted.rpx
 - [IP_Flow 19-1839] IP Catalog is up to date.
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Corehdl 2-168] The results of DRC are in file Spartan6_DSP48A1_drc_opted.rpt.
 - Place Design (24 infos)**
 - [Chipscope 16-240] Debug cores have already been implemented
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
 - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
 - [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - [Physopt 32-65] No nets found for high-fanout optimization.
 - [Physopt 32-232] Optimized 0 net. Created 0 new instance.
 - [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
 - [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
 - [Place 30-746] Post Placement Timing Summary WNS=5.171. For the most accurate timing information please run report_timing.
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-138] The checkpoint 'D:/other/Courses/Kareem_waseem_Digital-Design/Projects/Project_1/Synthesis/p1/project_1/project_1_runs/impl_1/Spartan6_DSP48A1_placed.dcp' has been generated.
 - [runctd-4] Executing : report_io -file Spartan6_DSP48A1_io_placed.rpt (2 more like this)
 - Route Design (2 warnings, 36 infos)**
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
 - DRC (1 warning)**
 - Pin Planning (1 warning)**
 - [DRC CFGIVS-7] CONFIG_VOLTAGE with Config Bank VCCO: The CONFIG_MODE property of current_design specifies a configuration mode (SPILx4) that uses pins in bank 14. I/O standards used in this bank have a voltage requirement of 1.80. However, the CONFIG_VOLTAGE for current_design is set to 3.3. Ensure that your configuration voltage is compatible with the I/O standards in banks used by your configuration mode. Refer to device configuration user guide for more information. Pins used by config mode: V28 (IO_L1P_T0_D00_MOSI_14), V29 (IO_L1N_T0_D01_DIN_14), V26 (IO_L2P_T0_D02_14), V27 (IO_L2N_T0_D03_14), W26 (IO_L3P_T0_DQ0_PUDC_B_14), and Y27 (IO_L6P_T0_FCS_B_14)

ⓘ [Vivado_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings
 ⓘ [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
 ⓘ [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
 > ⓘ [Route 35-416] Intermediate Timing Summary | WNS=5.186 | TNS=0.000 | WHS=-1.513 | THS=-332.761| (3 more like this)
 ⓘ [Route 35-57] Estimated Timing Summary | WNS=3.117 | TNS=0.000 | WHS=0.057 | THS=0.000 |
 ⓘ [Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.
 ⓘ [Route 35-16] Router Completed Successfully
 ⓘ [Common 17-83] Releasing license: Implementation
 ⓘ [Timing 38-480] Writing timing data to binary archive.
 ⓘ [Common 17-1381] The checkpoint 'D:/other/Courses/Kareem_waseem_Digital-Design/Projects/Project_1/Synthesis/p1/project_1/runs/impl_1/Spartan6_DSP48A1_routed.dcp' has been generated.
 ⓘ [IP_Flow 19-1839] IP Catalog is up to date
 > ⓘ [DRC 23-27] Running DRC with 2 threads (1 more like this)
 ⓘ [Corefd 2-168] The results of DRC are in file Spartan6_DSP48A1_drc_routed.rpt.
 > ⓘ [runtdc-4] Executing : report_drc -file Spartan6_DSP48A1_drc_routed.rpt -pb Spartan6_DSP48A1_drc_routed.pb -rpx Spartan6_DSP48A1_drc_routed.rpx (7 more like this)
 > ⓘ [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 ⓘ [DRC 23-133] Running Methodology with 2 threads
 ⓘ [Corefd 2-1520] The results of Report Methodology are in file Spartan6_DSP48A1_methodology_drc_routed.rpt.
 ⓘ [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
 ⓘ [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
 > ⓘ [Timing 38-91] UpdateTimingParams: Speed grade: -3, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
 > ⓘ [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)

ⓘ Implemented Design (1 warning, 9 infos)

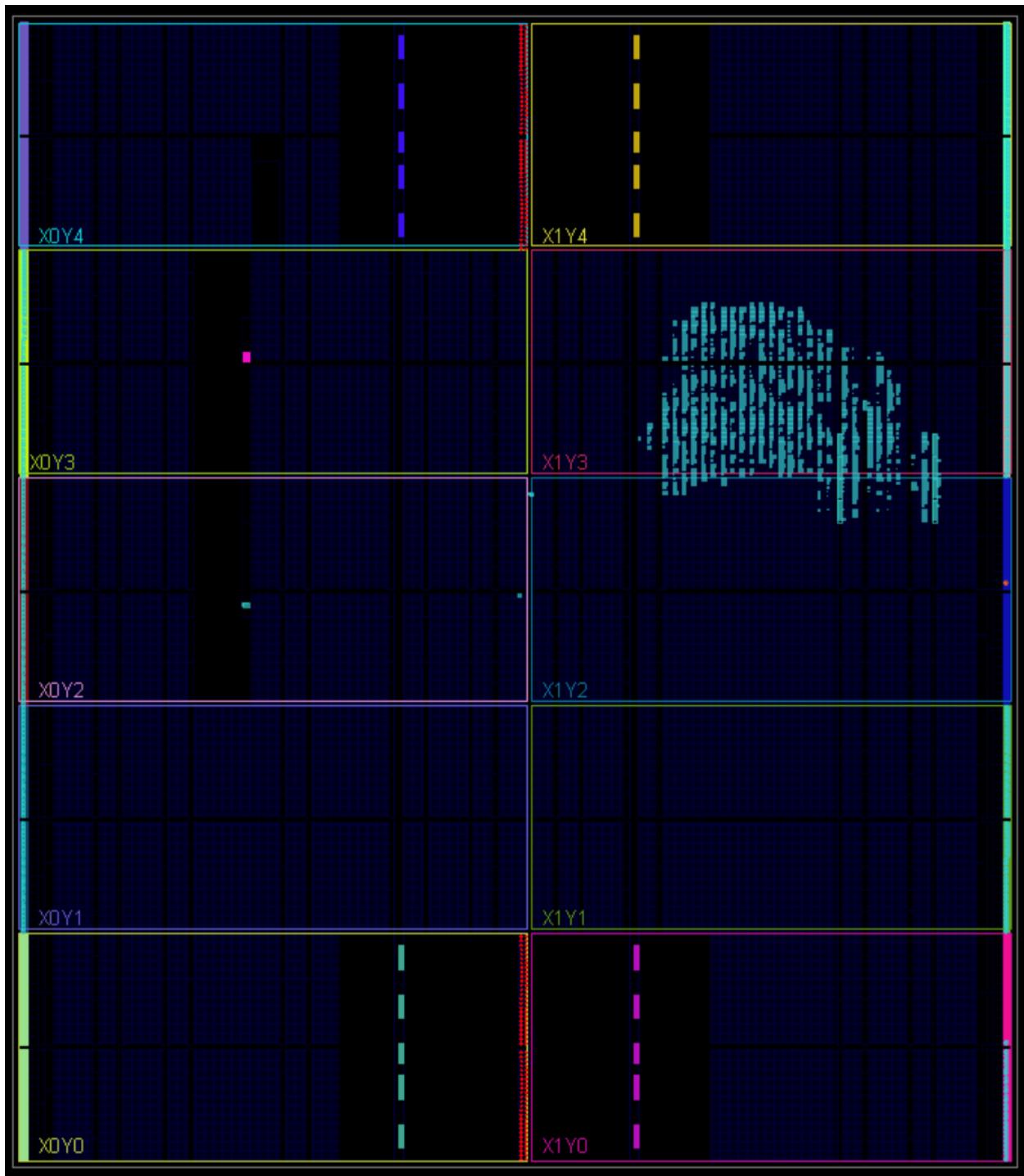
ⓘ General Messages (1 warning, 9 infos)

- ⓘ [Netlist 29-17] Analyzing 892 Unisim elements for replacement
- ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
- ⓘ [Project 1-570] Preparing netlist for logic optimization
- ⓘ [Timing 38-478] Restoring timing data from binary archive.
- ⓘ [Timing 38-479] Binary timing data restore complete.
- ⓘ [Project 1-856] Restoring constraints from binary archive.
- ⓘ [Project 1-853] Binary constraint restore complete.
- ⓘ [Project 1-111] Unisim Transformation Summary:
A total of 262 instances were transformed.
CFGlut5 => CFGlut5 (SRLC32E, SRL16E): 256 instances
RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances
- ⓘ [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.

Utilization report

Timing report

Device Snippet



9. Linting

a) Lint snippet

Questa Lint 2021.1 (J:\gn\Projects\Project_1\Lint\code\lint.db)

File Edit View Lint Checks Window Help

Details

```

1 module mux_reg_18bits_sync(out_mux_reg, in, clk, clkE, rst);
2   parameter Reg_state = "1";
3   parameter width_reg = 18;
4   parameter width_reg - 1:0 in;
5   parameter width_reg - 1:0 out_mux_reg;
6   parameter width_reg - 1:0 out_reg;
7   parameter width_reg - 1:0 out_mux_reg;
8   parameter width_reg - 1:0 out_reg;
9   parameter width_reg - 1:0 out_mux_reg;
10  parameter width_reg - 1:0 out_reg;
11  parameter width_reg - 1:0 out_mux_reg;
12  parameter width_reg - 1:0 out_reg;
13  parameter width_reg - 1:0 out_mux_reg;
14  assign out_mux_reg = (Reg_state == 1)? out_reg : in;
15  always @ (posedge clk) begin
16    if(clkE)begin
17      if(rst)begin
18        out_reg <= 0;
19      end
20      else begin
21        out_reg <= in;
22      end
23    end
24  end
25 endmodule

```

Lint Summary

Name	Count
Open/uninspected	9
Info	9
condition_const	3
parameter_name_duplicate	4
line_char_large	2

Flow Navi... De... De... mux_b_bcin.v mux_reg_18bits_parameter.v mux_post_add_sub.v mux_reg_18bits_sync.v Drivers Lint Summary Schematic 1

Lint Checks

Filter: Type here

Severity	Status	Check	Alias	Message	Module
Info		condition_const		Condition expression is a constant. Module mux_b_bcin, File D:/other/Courses/Kareem_waseem_Digital-Design/Projects/Project_1/Lint/code/mux...	mux_b_bcin
Info		condition_const		Condition expression is a constant. Module mux_carry_cascade_in, File D:/other/Courses/Kareem_waseem_Digital-Design/Projects/Project_1/Lint...	mux_carry_cascade_in
Info		condition_const		Condition expression is a constant. Module mux_carry_cascade_out, File D:/other/Courses/Kareem_waseem_Digital-Design/Projects/Project_1/Lint...	mux_carry_cascade_out
Info		parameter_name_duplicate		Same parameter name is used in more than one module. Parameter width, Total count 2, First module: Module mux_post_add_sub, File...	mux_post_add_sub
Info		parameter_name_duplicate		Same parameter name is used in more than one module. Parameter width, Total count 2, First module: Module mux_reg_18bits_parameter, File...	mux_reg_18bits_parameter
Info		parameter_name_duplicate		Same parameter name is used in more than one module. Parameter width, Total count 2, First module: Module mux_reg_18bits_parameter, File...	mux_reg_18bits_parameter
Info		parameter_name_duplicate		Same parameter name is used in more than one module. Parameter width, Total count 2, First module: Module mux_reg_18bits_parameter, File...	mux_reg_18bits_parameter
Info		line_char_large		Line has more characters than the specified limit. Current Count 115, Specified Limit 110, File D:/other/Courses/Kareem_waseem_Digital-Design/P...	none
Info		line_char_large		Line has more characters than the specified limit. Current Count 117, Specified Limit 110, File D:/other/Courses/Kareem_waseem_Digital-Design/P...	none

Transcript Message Viewer Lint Checks Design Metrics Design Information Status Desktop 2 Dashboard ...eem_waseem_Digital-Design\Projects\Project_1\Lint\code\mux_reg_18bits_sync.v [Spartan6_DSP48A1.A0_regM.genblk1.mux_reg_18bits]

b) Lint Schematic

