

```

≡ decoder3to8.v > ...
1  ✓ module decoder3to8 (
2      input en,
3      input [2:0] in,
4      output reg [7:0] out
5  );
6
7  ✓ always @(*) begin
8  ✓      if (en) begin
9          out = 8'b0;
10
11  ✓          case (in)
12              3'b000: out[0]=1'b1;
13              3'b001: out[1]=1'b1;
14              3'b010: out[2]=1'b1;
15              3'b011: out[3]=1'b1;
16              3'b100: out[4]=1'b1;
17              3'b101: out[5]=1'b1;
18              3'b110: out[6]=1'b1;
19              3'b111: out[7]=1'b1;
20              default: out=8'd0;
21          endcase
22      end
23  ✓      else begin
24          out = 8'b11111111;
25      end
26  end
27
28  endmodule

```

Figure 1 design

```

≡ tb.v
1  module decoder_tb;
2  wire [7:0] out;
3  reg [2:0] in;
4  reg en;
5  integer i;
6  decoder3to8 dut(en, in, out);
7
8  initial begin
9      $monitor( "en=%b, in=%b, out=%b ", en, in, out);
10     for ( i=0; i<16; i=i+1)
11         begin
12             {en,in} = i;
13             #1;
14         end
15     end
16 endmodule

```

Figure 2 testbench

```

PS D:\Engineering\External learning\Courses\IC Design\Chipions\Assignments> iverilog -o decoder .\decoder3to8.v .\tb.v
PS D:\Engineering\External learning\Courses\IC Design\Chipions\Assignments> vvp .\decoder
● en=0, in=000, out=11111111
en=0, in=001, out=11111111
en=0, in=010, out=11111111
en=0, in=011, out=11111111
en=0, in=100, out=11111111
en=0, in=101, out=11111111
en=0, in=110, out=11111111
en=0, in=111, out=11111111
en=1, in=000, out=00000001
en=1, in=001, out=00000010
en=1, in=010, out=00000100
en=1, in=011, out=00001000
en=1, in=100, out=00010000
en=1, in=101, out=00100000
en=1, in=110, out=01000000
○ en=1, in=111, out=10000000

```

Figure 3 output

The screenshot shows the EasyEDA interface with two panels: 'testbench.v' on the left and 'design.v' on the right. Below these panels is a log window showing the simulation results.

testbench.v (SV/Verilog Testbench):

```

1 // Code your testbench here
2 // or browse Examples
3 module decoder_tb;
4 wire [7:0] out;
5 reg [2:0] in;
6 reg en;
7 integer i;
8 decoder3to8 dut(en, in, out);
9
10 initial begin
11   $monitor("en=%b, in=%b, out=%b ", en, in, out);
12   for (i=0; i<16; i=i+1)
13     begin
14       {en,in} = i;
15       #1;
16     end
17 end
18 endmodule

```

design.v (SV/Verilog Design):

```

1 // Code your design here
2 module decoder3to8 (
3   input en,
4   input [2:0] in,
5   output reg [7:0] out
6 );
7
8 always @(*) begin
9   if (en) begin
10     out = 8'b0;
11
12     case (in)
13       3'b000: out[0]=1'b1;
14       3'b001: out[1]=1'b1;
15       3'b010: out[2]=1'b1;
16       3'b011: out[3]=1'b1;
17       3'b100: out[4]=1'b1;
18       3'b101: out[5]=1'b1;
19       3'b110: out[6]=1'b1;
20       3'b111: out[7]=1'b1;
21       default: out=8'd0;
22     endcase
23   end
24   else begin
25     out = 8'b11111111;
26   end
27 end
28 endmodule

```

Log Window:

```

[2023-04-17 15:40:03 EDT] iverilog '-wall' design.v testbench.v && unbuffer vvp a.out
en=0, in=000, out=11111111
en=0, in=001, out=11111111
en=0, in=010, out=11111111
en=0, in=011, out=11111111
en=0, in=100, out=11111111
en=0, in=101, out=11111111
en=0, in=110, out=11111111
en=0, in=111, out=11111111
en=1, in=000, out=00000001
en=1, in=001, out=00000010
en=1, in=010, out=00000100
en=1, in=011, out=00001000
en=1, in=100, out=00010000
en=1, in=101, out=00100000
en=1, in=110, out=01000000
en=1, in=111, out=10000000
Done

```

Figure 4 EasyEDA

EasyEDA link: <https://www.edaplayground.com/x/KXTx>