SPI_PROJECT

Ahmed Osama Fathy
Abdelrahman Essam Ismail

- ***Slave_Code:***

```
module SPI (clk,rst_n,MOSI,MISO,SS_n,rx_data,rx_valid,tx_data,tx_valid);
parameter IDLE=3'b000;
parameter CHK_CMD=3'b001;
parameter WRITE=3'b010;
parameter READ_ADDRESS=3'b011;
parameter READ_DATA=3'b100;
input MOSI,SS_n,clk,rst_n;
 output reg rx_valid;
output reg [9:0] rx_data;
input [7:0] tx_data;
input tx_valid;
reg  rd_address_first;

output reg MISO;

reg[3:0] count_1;
reg [3:0]count_2;
reg [3:0] count_3;
(* fsm_encoding = "gray" *)
reg [2:0] ns,cs;

always@(cs,MOSI,SS_n)
begin
case (cs)
    IDLE:begin
        if(!SS_n)
        ns=CHK_CMD;
        else
        ns= IDLE;

    end

    CHK_CMD:begin
        if(SS_n==0)
        begin
        if(MOSI==0)
        ns=WRITE;
        else
        if(rd_address_first==0)
        begin
        ns=READ_ADDRESS;

        end
        else
        begin
        ns=READ_DATA;

```

```
            end


            end
            else
            ns= IDLE;


        end

        WRITE:begin
            if(SS_n)
            ns= IDLE;
            else
            begin
            if(count_1 <10)
            ns= WRITE;

            end

        end

        READ_ADDRESS:begin

            if(SS_n)
            ns=IDLE;
            else
            begin
                if(count_2 < 10)
                ns=READ_ADDRESS;
        end
        end
        READ_DATA: begin

             if(SS_n)
            ns=IDLE;
            else
            begin
                if(count_3 < 8)
                ns=READ_DATA;
        end
        end

        default: ns= IDLE;
    endcase
    end

    always@(posedge clk,negedge rst_n)
    begin
      if(!rst_n)
```

```
   cs<=IDLE;
else
cs<= ns;

end

always@(posedge clk,negedge rst_n)
begin
if(!rst_n)
begin
  rx_data<=0;
  rx_valid<=0;
  count_1<=0;
   count_2<=0;
  rd_address_first<=0;
  count_3<=0;
MISO<=0;

end
else
case(cs)
IDLE:begin
  rx_valid<=0;
  count_1<=0;
 count_2<=0;
  count_3<=0;
end

CHK_CMD:begin
    rx_valid<=0;
    count_1<=0;
   count_2<=0;
    count_3<=0;

end

WRITE: begin
    if(count_1<10)
    begin
        rx_data<={rx_data[8:0],MOSI};
        count_1<=count_1+1;
    end
        else
        rx_valid<=1;

    end

READ_ADDRESS: begin
 rd_address_first<=1;
    if(count_2<10)
    begin
        rx_data<={rx_data[8:0],MOSI };
       count_2<=count_2+1;
    end
        else
        rx_valid<=1;

    end
    READ_DATA: begin
    rd_address_first<=0;
    if(count_2<10)
    begin
        rx_data<={rx_data[8:0],MOSI };
       count_2<=count_2+1;
    end
        else
        begin
        rx_valid<=1;
        if(count_3 < 8 )
        begin
            if(tx_valid==1)
            begin
            MISO <= tx_data[7-count_3];
            count_3<=count_3+1;
            end

        end
        end

    end
    default:begin
  rx_valid<=0;
  count_1<=0;
 count_2<=0;
  count_3<=7;
end
    endcase
end

endmodule


```

- ***RAM_Code:***

```
module RAM_pr2(clk,rst_n,din,rx_valid,dout,tx_valid);
parameter MEM_DEPTH = 256;
parameter ADDR_SIZE = 8;
input [9:0] din;
input rx_valid,clk,rst_n;
output reg[7:0] dout;
output reg tx_valid;
reg [ADDR_SIZE-1:0] wr_address;
reg [ADDR_SIZE-1:0] mem_1 [MEM_DEPTH-1:0];

always @(posedge clk,negedge rst_n) begin
    if(!rst_n)
    begin
    dout<=0;
    tx_valid<=0;
    end
    else
    begin
    if(rx_valid==1)
    begin
    case (din[9:8])
    2'b00: begin
      wr_address<= din[7:0];
      tx_valid<=0;
    end

    2'b01: begin
        mem_1[wr_address]<= din[7:0];
        tx_valid<=0;
    end
    2'b10:begin
         wr_address<= din[7:0];
         tx_valid<=0;
    end
    2'b11: begin
        dout<= mem_1[wr_address];
        tx_valid<=1;
    end
     default: wr_address<= din[7:0];
    endcase
    end
end
end
endmodule

```

- ***Master_Code:***

```
module Master(SS_n,MOSI,MISO,clk,rst_n);
input MOSI,SS_n,clk,rst_n;
 output MISO;
 wire rx_valid;
wire [9:0] rx_data;
wire [7:0] tx_data;
wire tx_valid;
 SPI   s1 (clk,rst_n,MOSI,MISO,SS_n,rx_data,rx_valid,tx_data,tx_valid);
RAM_pr2  R1(clk,rst_n,rx_data,rx_valid,tx_data,tx_valid);
endmodule

```

- ***TB_Code:***

```
module master_slave();
reg MOSI,SS_n,clk,rst_n;
 wire MISO;
Master M1(SS_n,MOSI,MISO,clk,rst_n);
initial begin
    clk=1;
forever

   #1 clk=~clk;
end

initial begin
    rst_n=0;
    #5;
 rst_n=1;
//giving write address
SS_n=0;
@(negedge clk);
MOSI=0;
@(negedge clk);


repeat(2)

  @(negedge clk) MOSI=0;




repeat(8)

   @(negedge clk) MOSI=1;
#5;
SS_n=1;
```

```
#10;
// store data in ram at the address given before

SS_n=0;
@(negedge clk);
MOSI=0;
@(negedge clk);




  @(negedge clk) MOSI=0;
@(negedge clk) MOSI =1;




repeat(8)

   @(negedge clk) MOSI=$random;
#5;
SS_n=1;
#10;
// giving address to read data from it
rst_n=1;
SS_n=0;
@(negedge clk);
MOSI=1;
@(negedge clk);




  @(negedge clk) MOSI=1;
@(negedge clk) MOSI =0;




repeat(8)

   @(negedge clk) MOSI=1;
#5;
SS_n=1;
#10;
// Read data from the address given before  inside the RAM
rst_n=1;
SS_n=0;
@(negedge clk);
MOSI=1;
```

```
@(negedge clk);




  @(negedge clk) MOSI=1;
@(negedge clk) MOSI =1;




repeat(8)

   @(negedge clk) MOSI=0;
#24;
SS_n=1;
#10;
//  giving new write address
SS_n=0;
@(negedge clk);
MOSI=0;
@(negedge clk);


repeat(2)

  @(negedge clk) MOSI=0;




repeat(7)

   @(negedge clk) MOSI=1;

   @(negedge clk) MOSI=0;

#5;
SS_n=1;
#10;


 // write new data in the given address inside RAM
 SS_n=0;
@(negedge clk);
MOSI=0;
@(negedge clk);



```

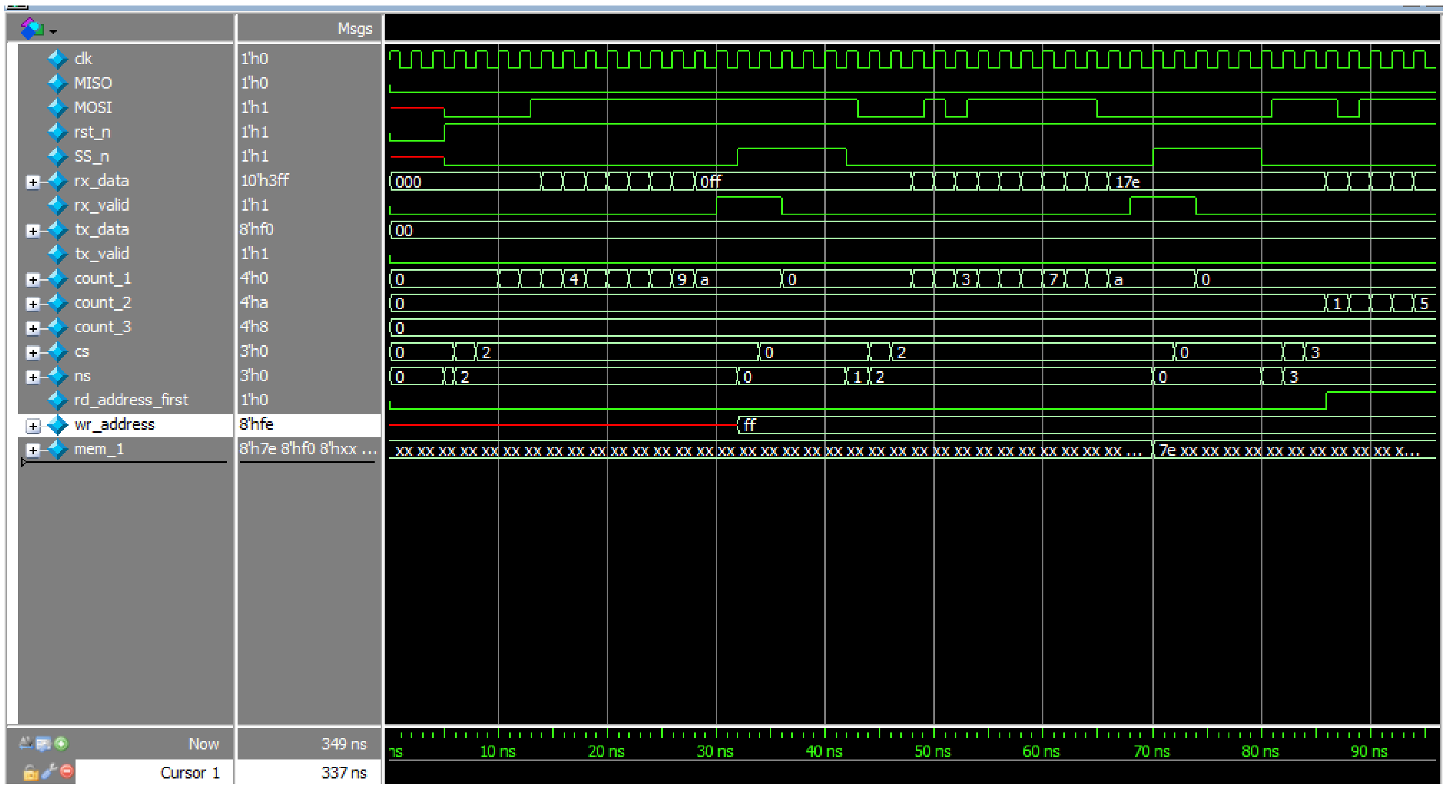
```
•
•     @(negedge clk) MOSI=0;
•     @(negedge clk) MOSI=1;
•
•
•
•
•   repeat(4)
•
•      @(negedge clk) MOSI=1;
•
•      repeat(4)
•      @(negedge clk) MOSI=0;
•
•
•   #5;
•   SS_n=1;
•   #10;
•   //  taking read address
•   SS_n=0;
•   @(negedge clk);
•   MOSI=1;
•   @(negedge clk);
•
•
•
•
•     @(negedge clk) MOSI=1;
•     @(negedge clk) MOSI=0;
•
•
•
•
•   repeat(7)
•
•      @(negedge clk) MOSI=1;
•
•      @(negedge clk) MOSI=0;
•
•   #5;
•   SS_n=1;
•   #10;
•   //read data from memory
•   SS_n=0;
•   @(negedge clk);
•   MOSI=1;
•   @(negedge clk);
•
•
•   repeat(2)
```

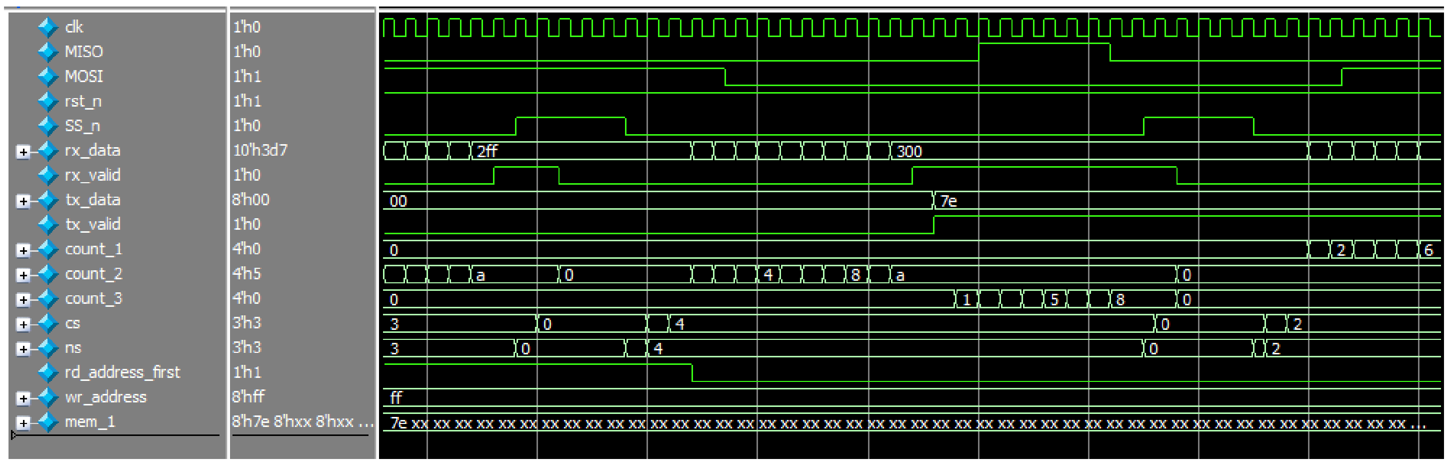
```
    @(negedge clk) MOSI=1;




  repeat(8)

     @(negedge clk) MOSI=1;

  #24;
  SS_n=1;
  #10;
  SS_n=0;
  #2;
  SS_n=1;
  #2;


     $stop;


  end
  endmodule
```

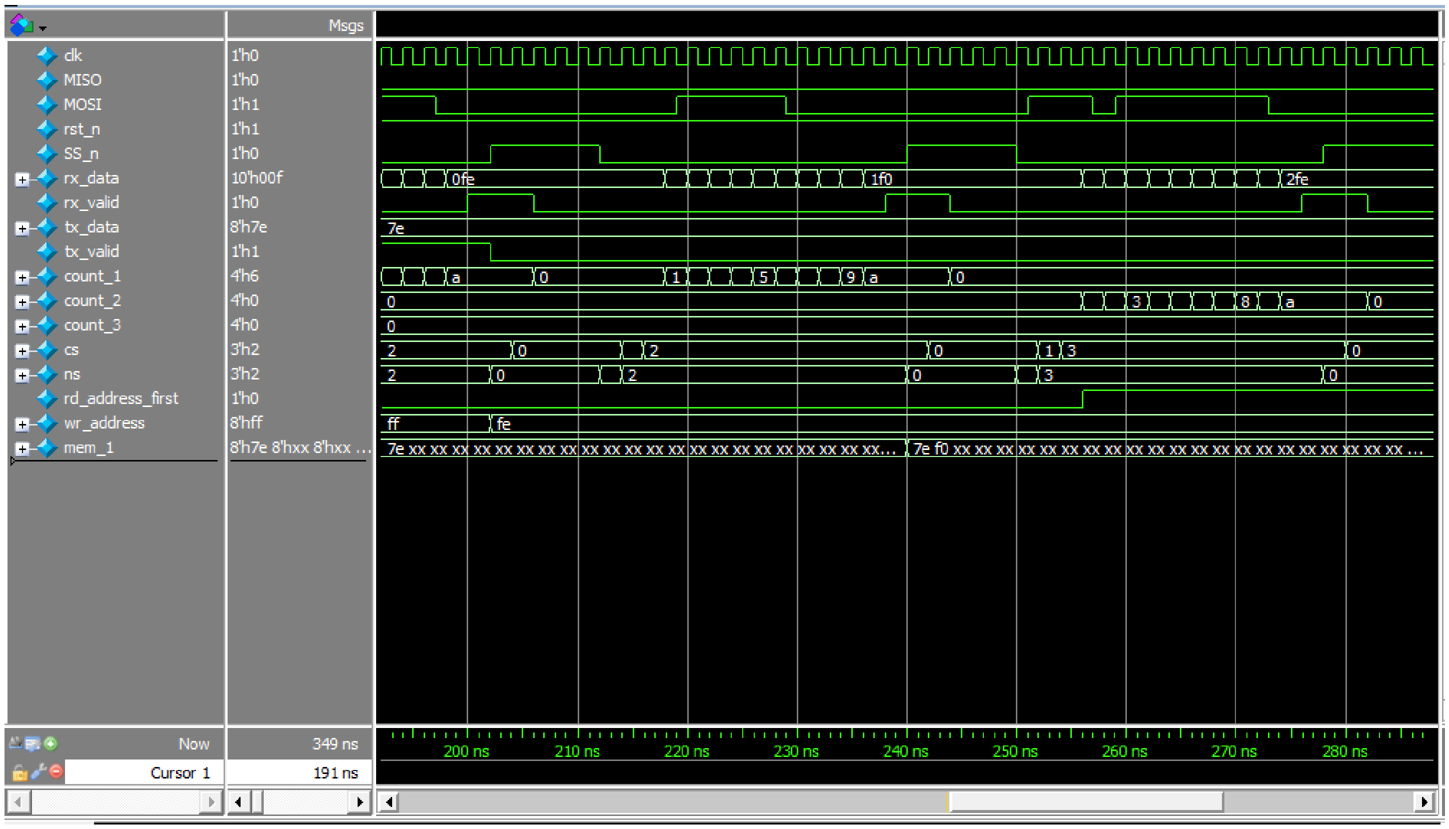
- ***DO_File:***

```
vlib work
vlog SPI.v Master.v master_slave_tb.v RAM_pr2.v
vsim -voptargs=+acc master_slave
add wave -position insertpoint  \
sim:/master_slave/clk \
sim:/master_slave/MISO \
sim:/master_slave/MOSI \
sim:/master_slave/rst_n \
sim:/master_slave/SS_n \
sim:/master_slave/M1/rx_data \
sim:/master_slave/M1/rx_valid \
sim:/master_slave/M1/tx_data \
sim:/master_slave/M1/tx_valid \
sim:/master_slave/M1/s1/count_1 \
sim:/master_slave/M1/s1/count_2 \
sim:/master_slave/M1/s1/count_3 \
sim:/master_slave/M1/s1/cs \
sim:/master_slave/M1/s1/ns \
sim:/master_slave/M1/R1/mem_1
run -all
```

- ***Snippets_of_waveform:***

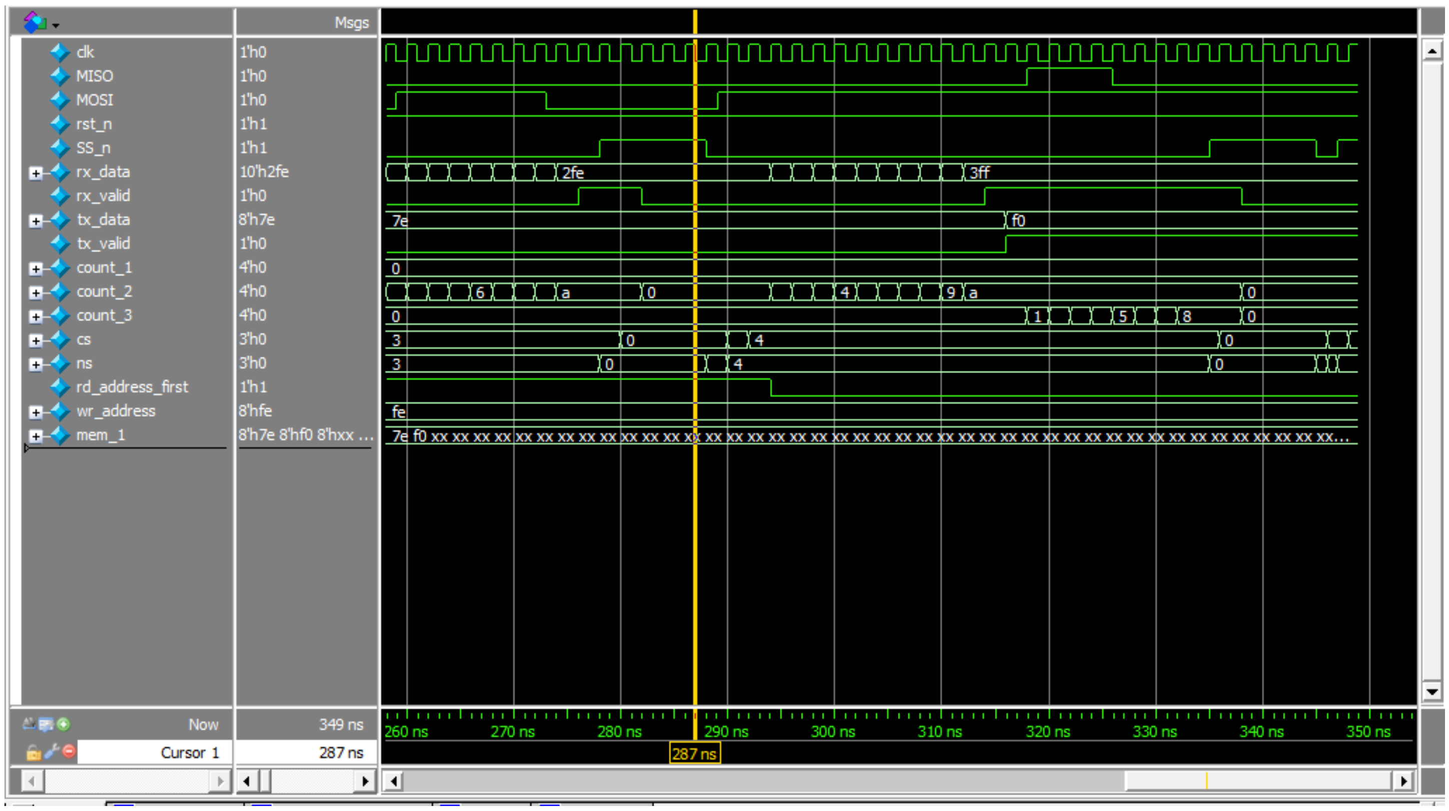






```
                    Msgs
clk                 1'h0
MISO                1'h0
MOSI                1'h1
rst_n               1'h1
SS_n                1'h0
rx_data             10'h00f
rx_valid            1'h0
tx_data             8'h7e
tx_valid            1'h1
count_1             4'h6
count_2             4'h0
count_3             4'h0
cs                  3'h2
ns                  3'h2
rd_address_first    1'h0
wr_address          8'hff
mem_1               8'h7e 8'hxx 8'hxx ...

Now                 349 ns
Cursor 1            191 ns
```

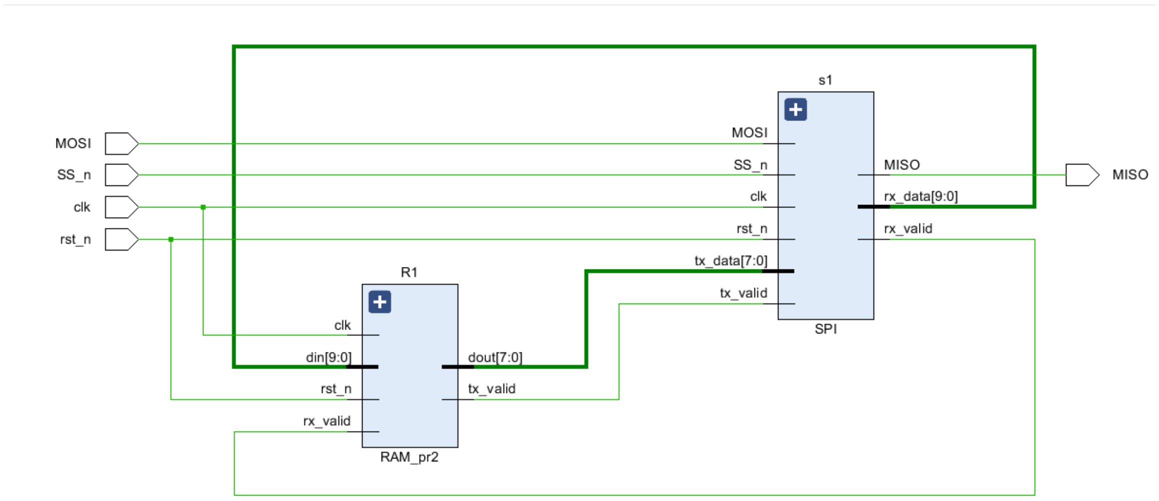
0fe
1f0
2fe
7e
a
0
1
5
9
3
8
2
fe
ff
7e xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx...
7e f0 xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx ...
200 ns
210 ns
220 ns
230 ns
240 ns
250 ns
260 ns
270 ns
280 ns

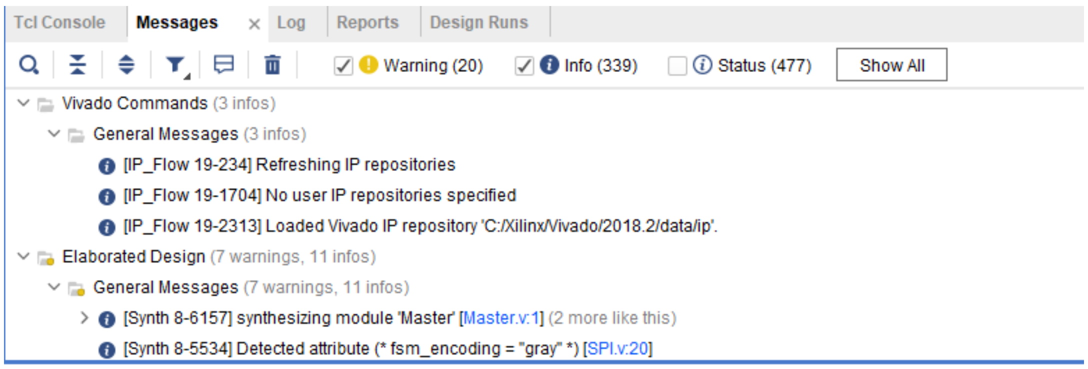


```
                    Msgs
clk                 1'h0
MISO                1'h0
MOSI                1'h0
rst_n               1'h1
SS_n                1'h1
rx_data             10'h2fe
rx_valid            1'h0
tx_data             8'h7e
tx_valid            1'h0
count_1             4'h0
count_2             4'h0
count_3             4'h0
cs                  3'h0
ns                  3'h0
rd_address_first    1'h1
wr_address          8'hfe
mem_1               8'h7e 8'hf0 8'hxx ...

Now                 349 ns
Cursor 1            287 ns
```

2fe
3ff
7e
f0
0
6
a
4
9
1
5
8
3
fe
7e f0 xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx...
260 ns
270 ns
280 ns
290 ns
300 ns
310 ns
320 ns
330 ns
340 ns
350 ns
287 ns

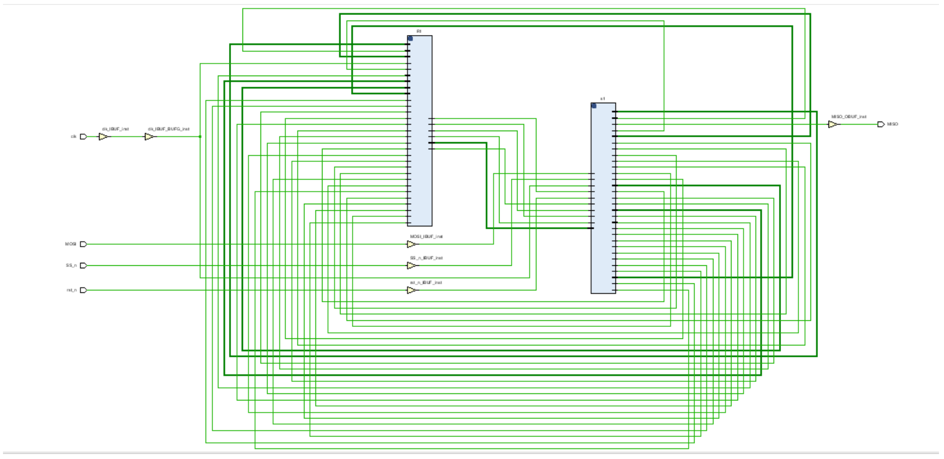
- ***Vivado:***
  - *Gray_Encoding*
  - ***Elaboration_with_no_errors***

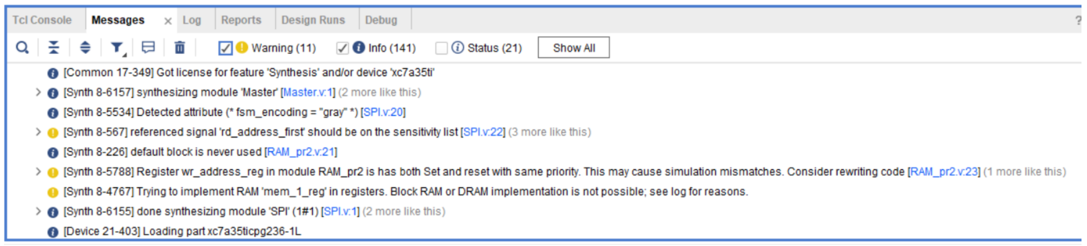




Vivado Commands (3 infos)
General Messages (3 infos)
[IP_Flow 19-234] Refreshing IP repositories
[IP_Flow 19-1704] No user IP repositories specified
[IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Elaborated Design (7 warnings, 11 infos)
General Messages (7 warnings, 11 infos)
[Synth 8-6157] synthesizing module 'Master' [Master.v:1] (2 more like this)
[Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPI.v:20]

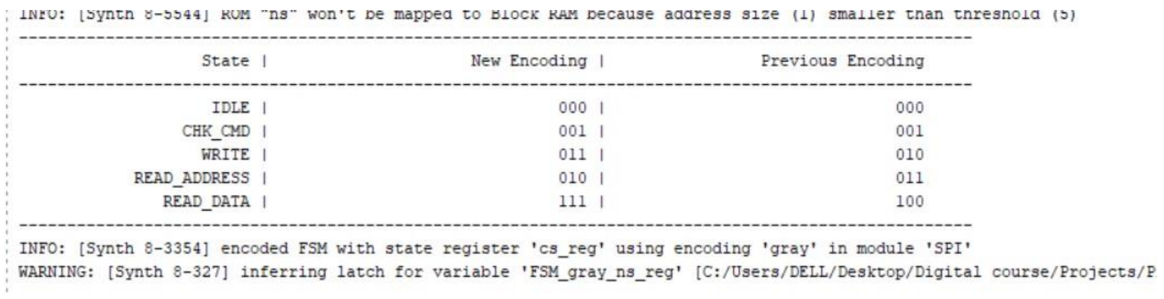
- ***Synthesis_schematic_with_no_errors***





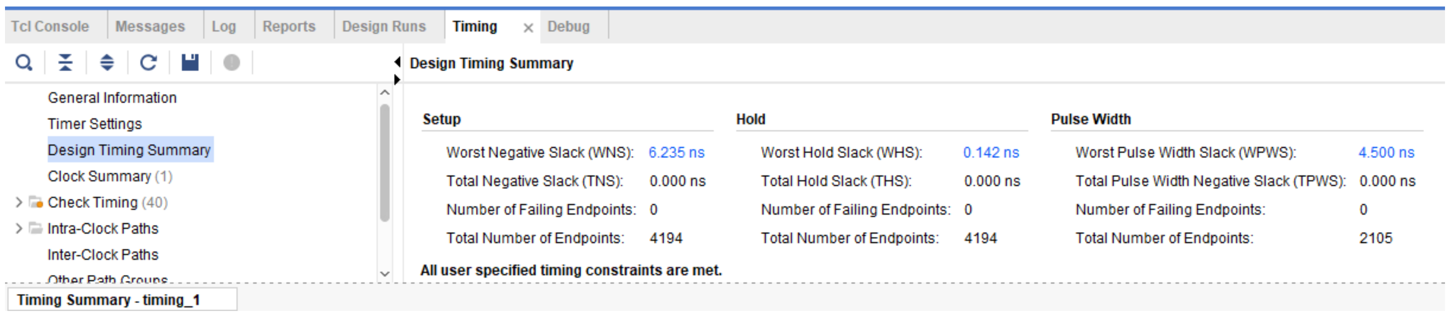
[Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
[Synth 8-6157] synthesizing module 'Master' [Master.v:1] (2 more like this)
[Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPI.v:20]
[Synth 8-567] referenced signal 'rd_address_first' should be on the sensitivity list [SPI.v:22] (3 more like this)
[Synth 8-226] default block is never used [RAM_pr2.v:21]
[Synth 8-5788] Register wr_address_reg in module RAM_pr2 is has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code [RAM_pr2.v:23] (1 more like this)
[Synth 8-4767] Trying to implement RAM 'mem_1_reg' in registers. Block RAM or DRAM implementation is not possible; see log for reasons.
[Synth 8-6155] done synthesizing module 'SPI' (1#1) [SPI.v:1] (2 more like this)
[Device 21-403] Loading part xc7a35ticpg236-1L

- ***Synthesis_Report***



```
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |                 Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                               000
                 CHK_CMD |                              001 |                               001
                   WRITE |                              011 |                               010
            READ_ADDRESS |                              010 |                               011
               READ_DATA |                              111 |                               100
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [C:/Users/DELL/Desktop/Digital course/Projects/P
```

- ***Synthesis_time_report***

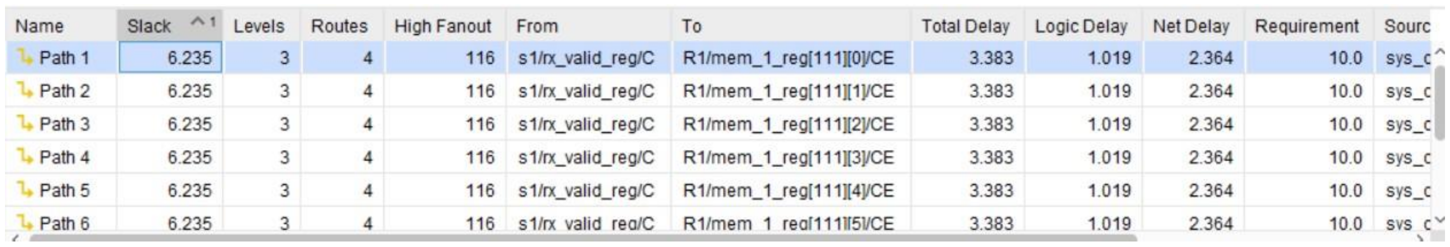


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.235 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4194	Total Number of Endpoints:	4194	Total Number of Endpoints:	2105

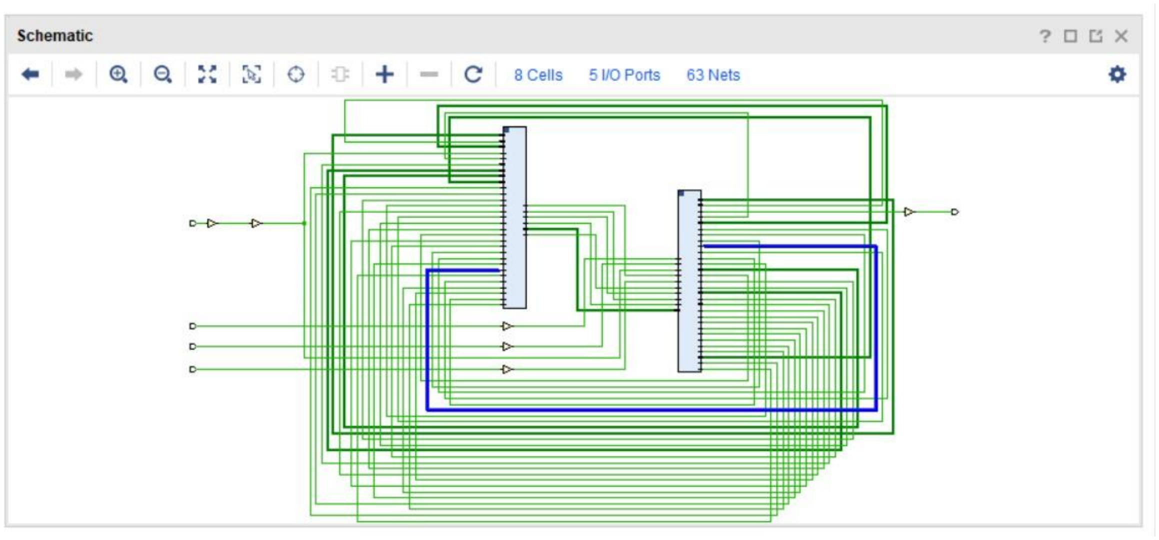
All user specified timing constraints are met.

Timing Summary - timing_1

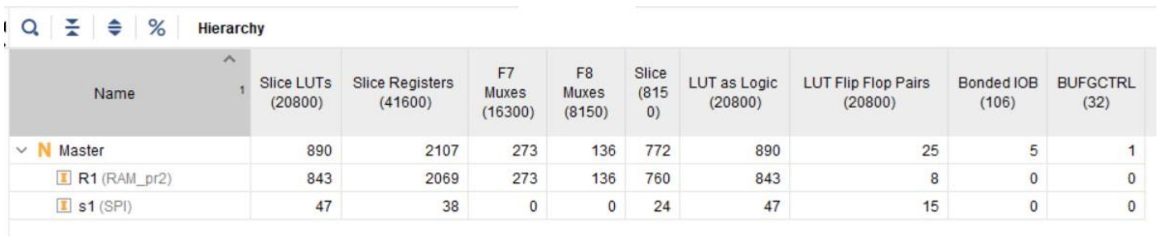


Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Sourc
Path 1	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][0]/CE	3.383	1.019	2.364	10.0	sys_c
Path 2	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][1]/CE	3.383	1.019	2.364	10.0	sys_c
Path 3	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][2]/CE	3.383	1.019	2.364	10.0	sys_c
Path 4	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][3]/CE	3.383	1.019	2.364	10.0	sys_c
Path 5	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][4]/CE	3.383	1.019	2.364	10.0	sys_c
Path 6	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][5]/CE	3.383	1.019	2.364	10.0	sys_c

- ***Critical_Path***

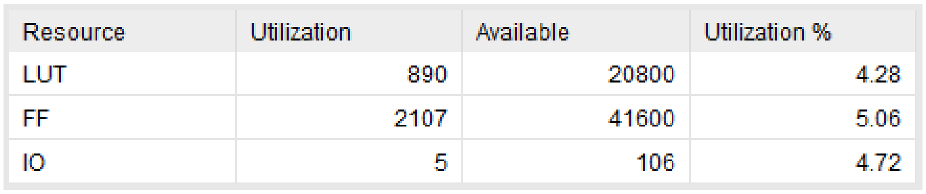


- ***Report_utilization_after_implementation***

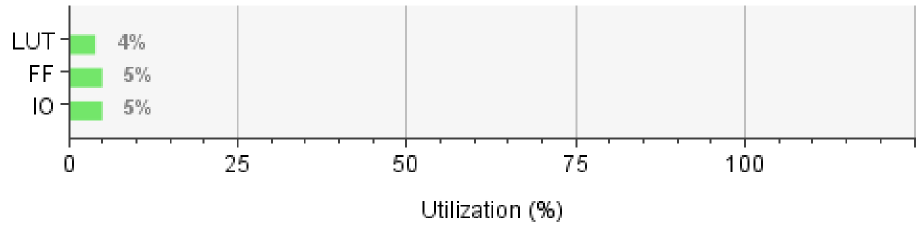


Hierarchy

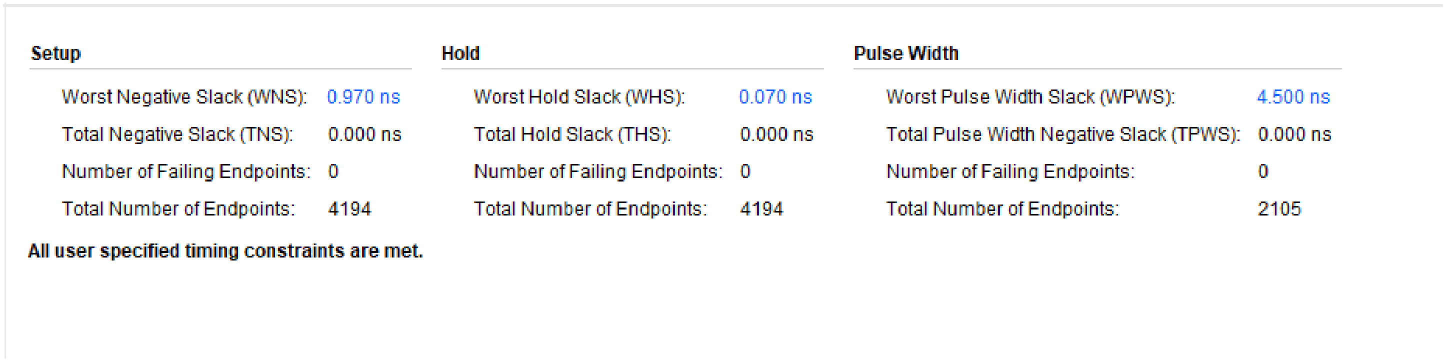
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
N Master	890	2107	273	136	772	890	25	5	1
R1 (RAM_pr2)	843	2069	273	136	760	843	8	0	0
s1 (SPI)	47	38	0	0	24	47	15	0	0



Resource	Utilization	Available	Utilization %
LUT	890	20800	4.28
FF	2107	41600	5.06
IO	5	106	4.72



- ***implementation_time_report***



Setup

Worst Negative Slack (WNS):	0.970 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	4194

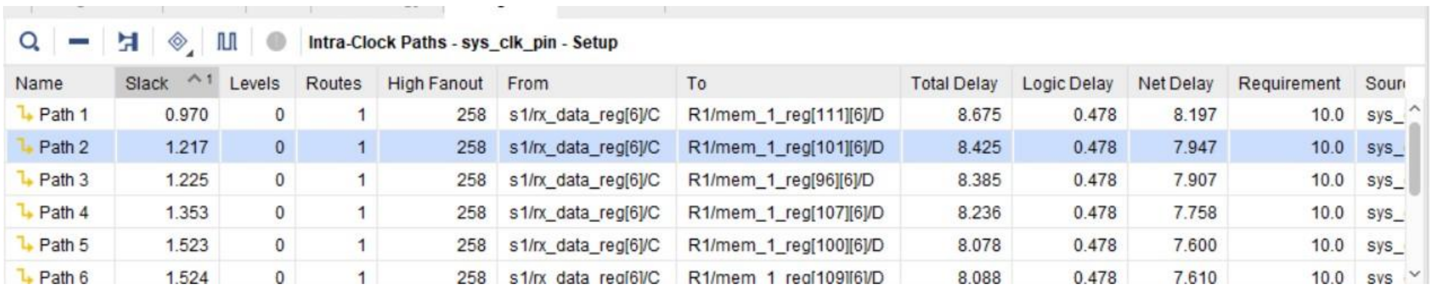
Hold

Worst Hold Slack (WHS):	0.070 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	4194

Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	2105

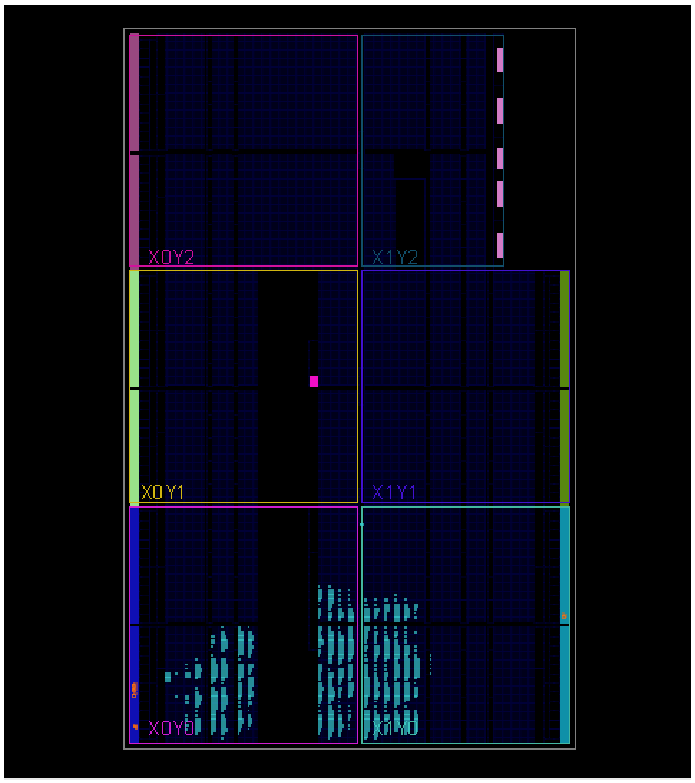
All user specified timing constraints are met.

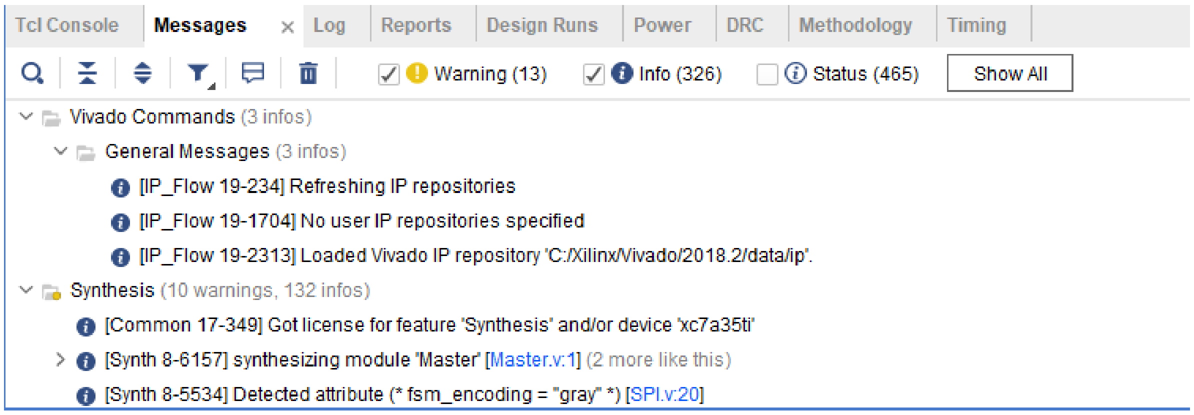


Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Sour
Path 1	0.970	0	1	258	s1/rx_data_reg[6]/C	R1/mem_1_reg[111][6]/D	8.675	0.478	8.197	10.0	sys_
Path 2	1.217	0	1	258	s1/rx_data_reg[6]/C	R1/mem_1_reg[101][6]/D	8.425	0.478	7.947	10.0	sys_
Path 3	1.225	0	1	258	s1/rx_data_reg[6]/C	R1/mem_1_reg[96][6]/D	8.385	0.478	7.907	10.0	sys_
Path 4	1.353	0	1	258	s1/rx_data_reg[6]/C	R1/mem_1_reg[107][6]/D	8.236	0.478	7.758	10.0	sys_
Path 5	1.523	0	1	258	s1/rx_data_reg[6]/C	R1/mem_1_reg[100][6]/D	8.078	0.478	7.600	10.0	sys_
Path 6	1.524	0	1	258	s1/rx_data_reg[6]/C	R1/mem_1_reg[109][6]/D	8.088	0.478	7.610	10.0	sys_

- ***Device_implementation_with_no_errors***

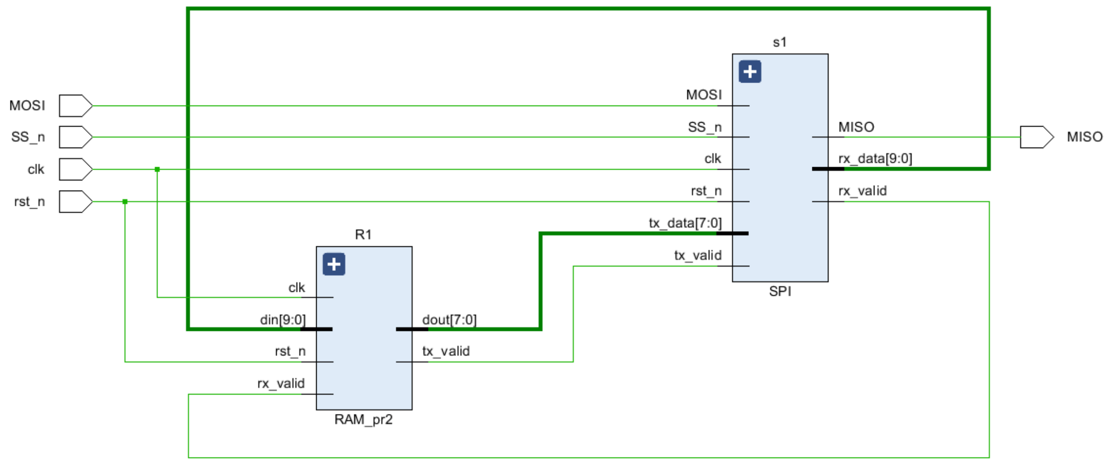


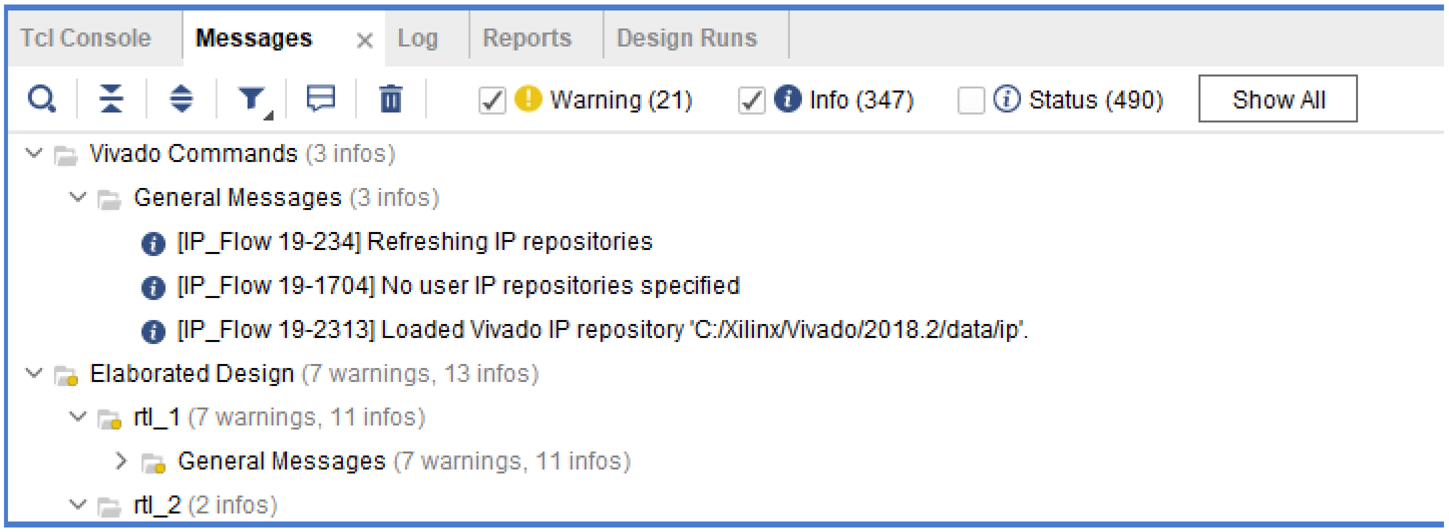


[✓] Warning (13) [✓] Info (326) [ ] Status (465)

```
Vivado Commands (3 infos)
    General Messages (3 infos)
        [IP_Flow 19-234] Refreshing IP repositories
        [IP_Flow 19-1704] No user IP repositories specified
        [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Synthesis (10 warnings, 132 infos)
    [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
    [Synth 8-6157] synthesizing module 'Master' [Master.v:1] (2 more like this)
    [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPI.v:20]
```

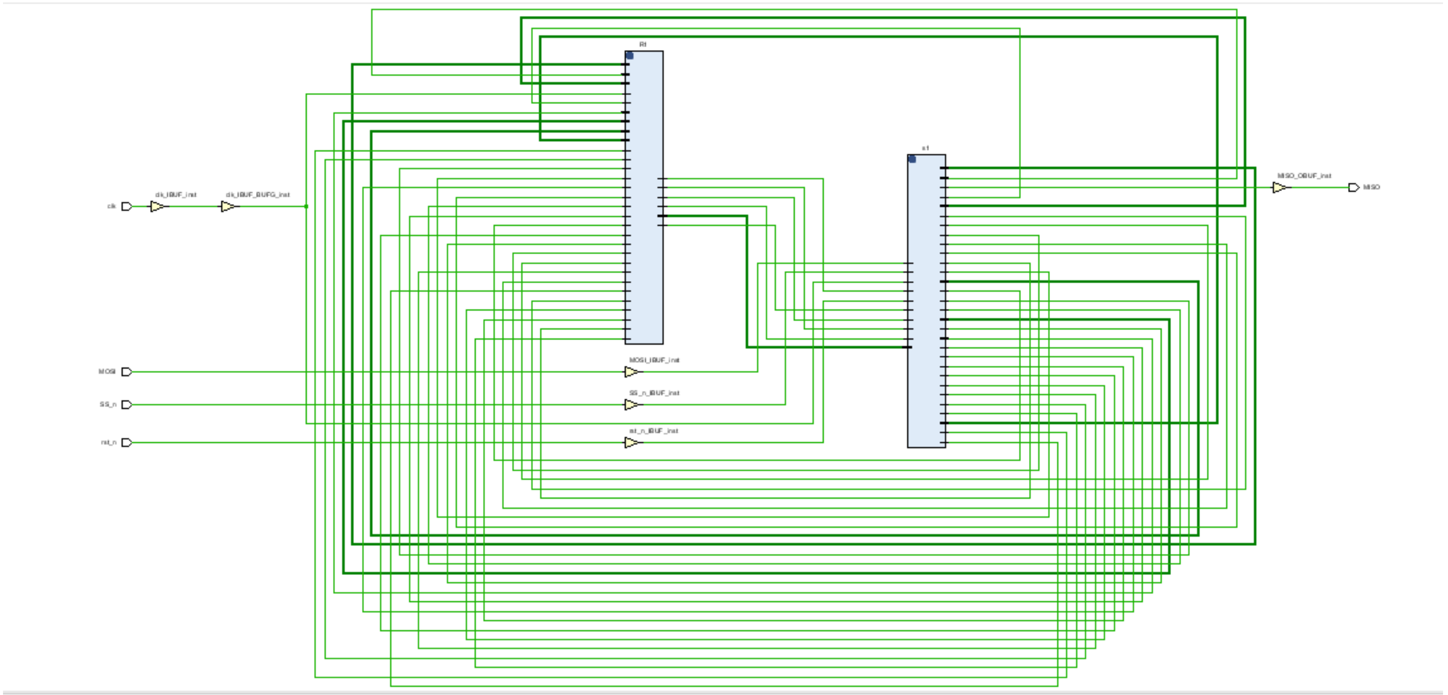
- *One_hot_encoding*
- ***Elaboration_with_no_errors***

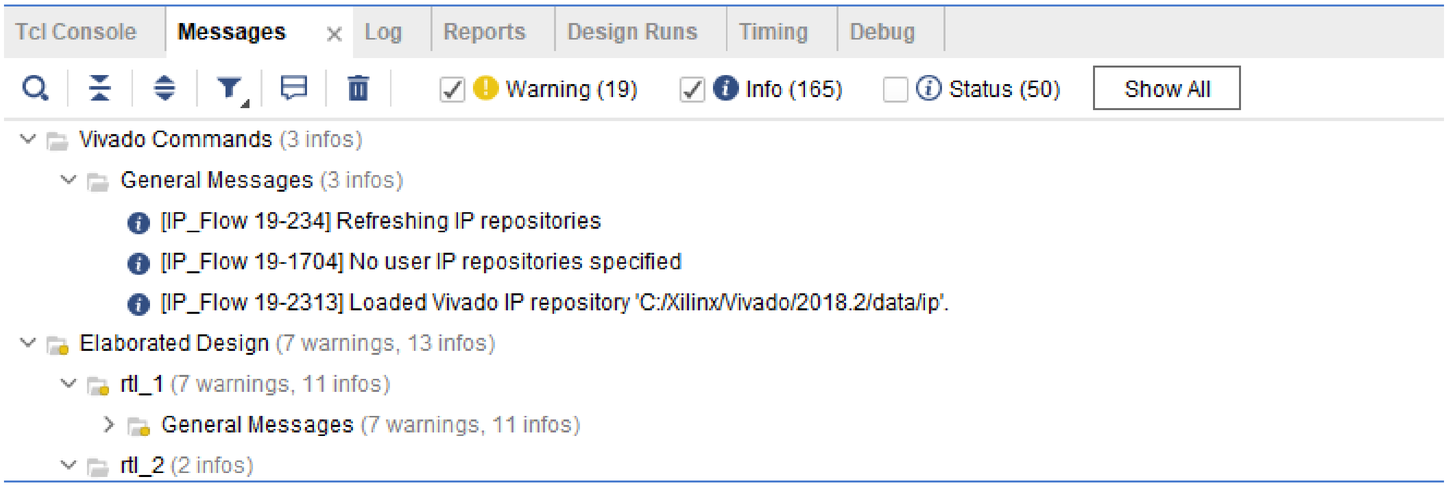




```
Vivado Commands (3 infos)
    General Messages (3 infos)
        [IP_Flow 19-234] Refreshing IP repositories
        [IP_Flow 19-1704] No user IP repositories specified
        [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Elaborated Design (7 warnings, 13 infos)
    rtl_1 (7 warnings, 11 infos)
        General Messages (7 warnings, 11 infos)
    rtl_2 (2 infos)
```

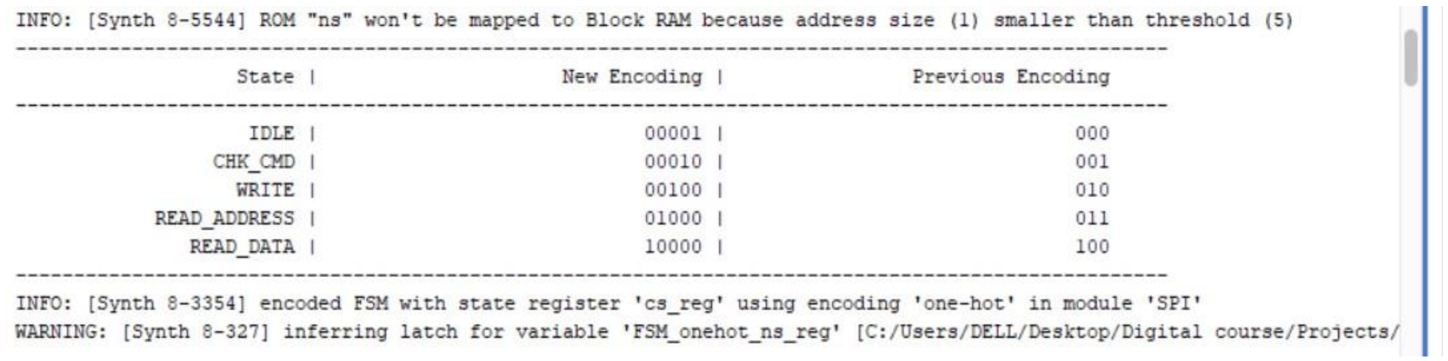
- ***Synthesis_schematic_with_no_errors***





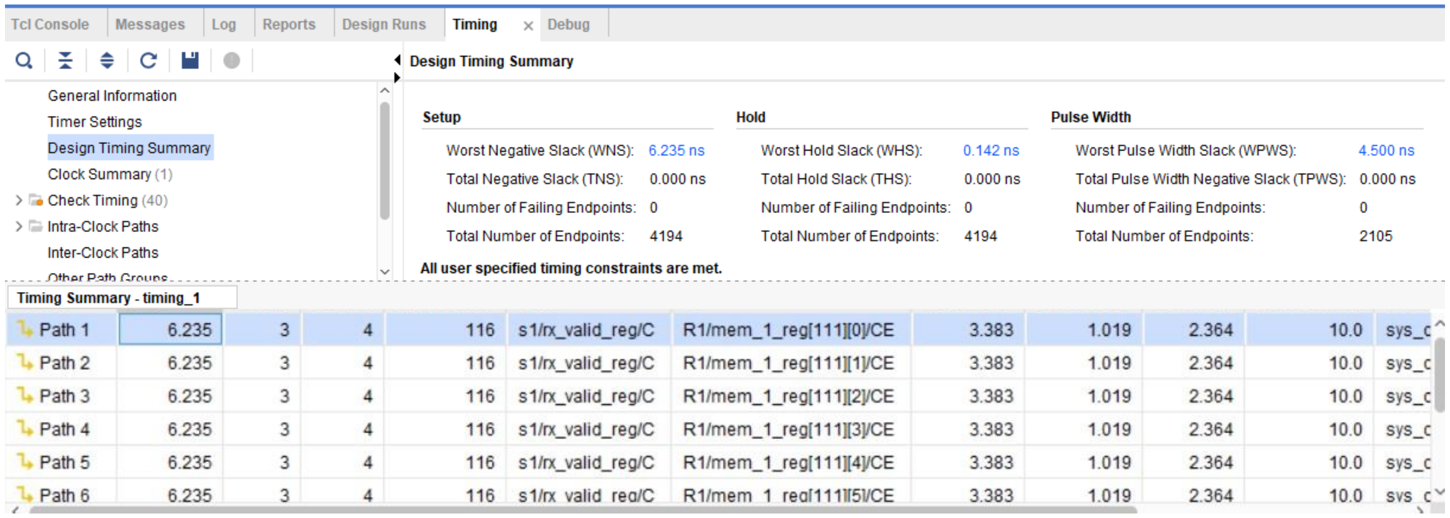
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Elaborated Design (7 warnings, 13 infos)
  rtl_1 (7 warnings, 11 infos)
    General Messages (7 warnings, 11 infos)
  rtl_2 (2 infos)

- ***Synthesis_Report***



```
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |                Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                            00001 |                              000
                 CHK_CMD |                            00010 |                              001
                   WRITE |                            00100 |                              010
            READ_ADDRESS |                            01000 |                              011
               READ_DATA |                            10000 |                              100
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [C:/Users/DELL/Desktop/Digital course/Projects/
```

- ***Synthesis_time_report***



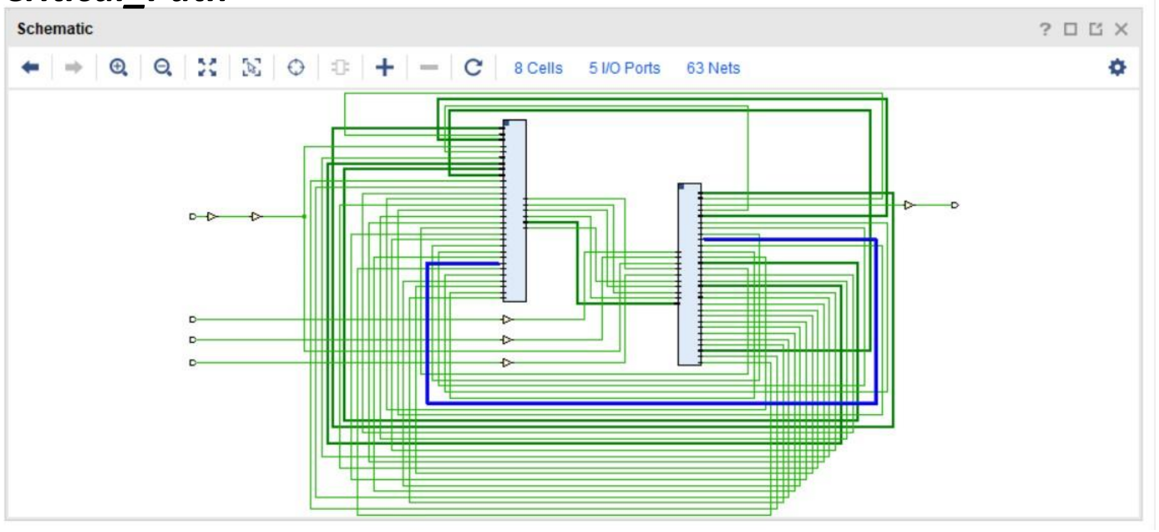
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.235 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4194	Total Number of Endpoints:	4194	Total Number of Endpoints:	2105

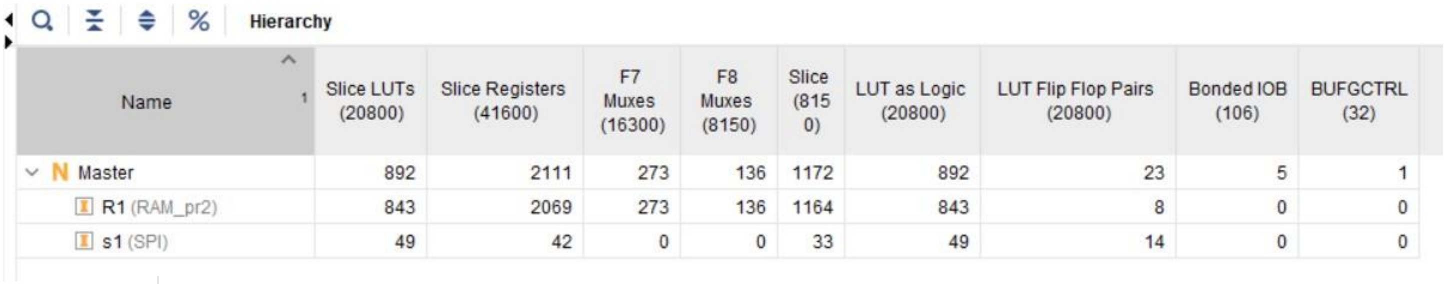
All user specified timing constraints are met.

Path 1	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][0]/CE	3.383	1.019	2.364	10.0	sys_c
Path 2	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][1]/CE	3.383	1.019	2.364	10.0	sys_c
Path 3	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][2]/CE	3.383	1.019	2.364	10.0	sys_c
Path 4	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][3]/CE	3.383	1.019	2.364	10.0	sys_c
Path 5	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][4]/CE	3.383	1.019	2.364	10.0	sys_c
Path 6	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][5]/CE	3.383	1.019	2.364	10.0	sys_c

- ***Critical_Path***

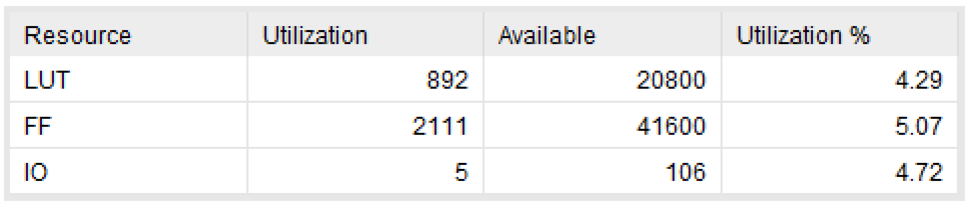


- ***Report_utilization_after_implementation***

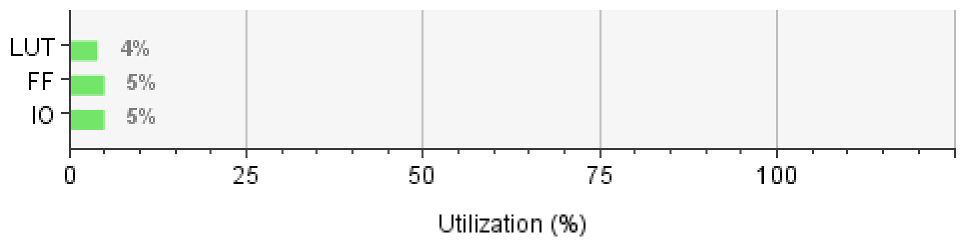


Hierarchy

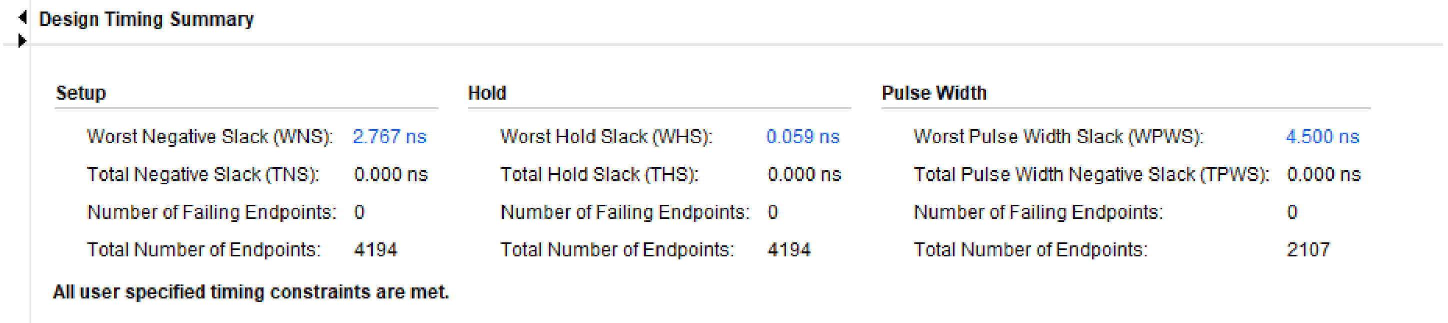
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
Master	892	2111	273	136	1172	892	23	5	1
R1 (RAM_pr2)	843	2069	273	136	1164	843	8	0	0
s1 (SPI)	49	42	0	0	33	49	14	0	0



Resource	Utilization	Available	Utilization %
LUT	892	20800	4.29
FF	2111	41600	5.07
IO	5	106	4.72



- ***implementation_time_report***



Design Timing Summary

Setup

Worst Negative Slack (WNS):	2.767 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	4194

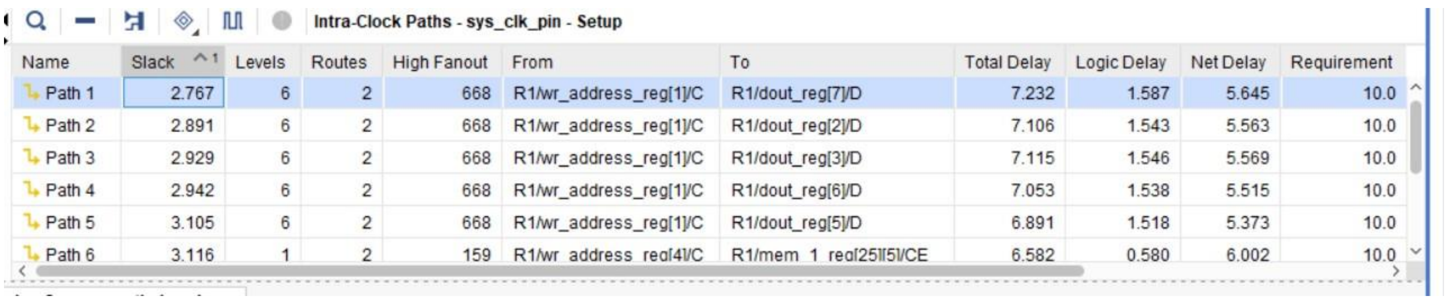
Hold

Worst Hold Slack (WHS):	0.059 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	4194

Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	2107

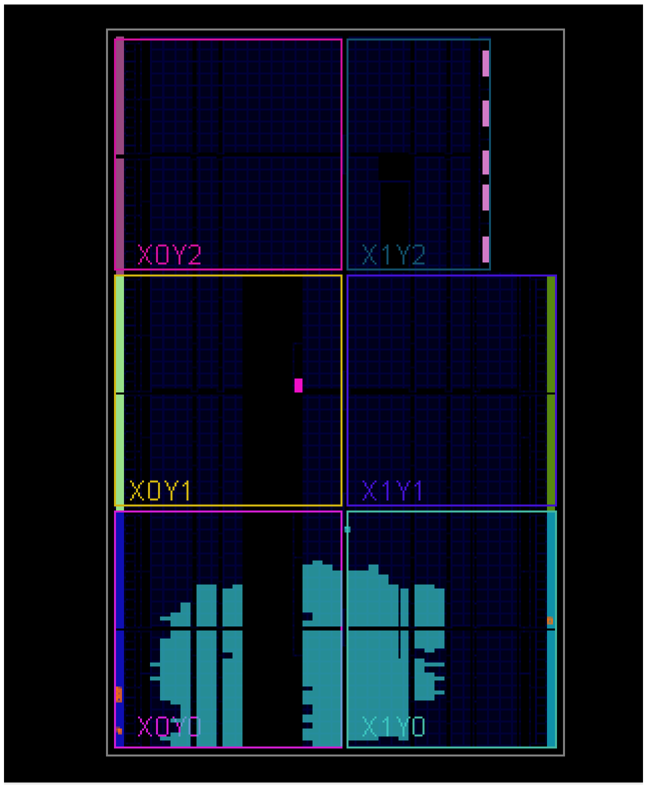
All user specified timing constraints are met.

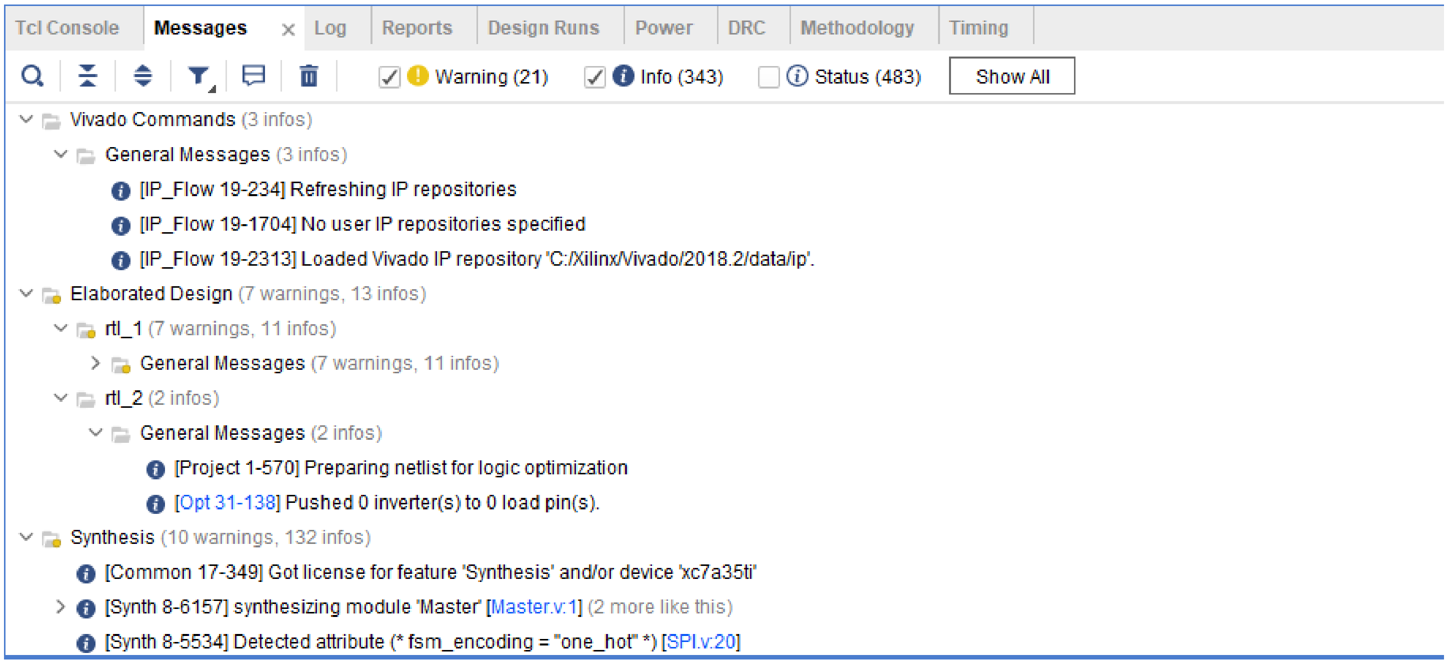


Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	2.767	6	2	668	R1/wr_address_reg[1]/C	R1/dout_reg[7]/D	7.232	1.587	5.645	10.0
Path 2	2.891	6	2	668	R1/wr_address_reg[1]/C	R1/dout_reg[2]/D	7.106	1.543	5.563	10.0
Path 3	2.929	6	2	668	R1/wr_address_reg[1]/C	R1/dout_reg[3]/D	7.115	1.546	5.569	10.0
Path 4	2.942	6	2	668	R1/wr_address_reg[1]/C	R1/dout_reg[6]/D	7.053	1.538	5.515	10.0
Path 5	3.105	6	2	668	R1/wr_address_reg[1]/C	R1/dout_reg[5]/D	6.891	1.518	5.373	10.0
Path 6	3.116	1	2	159	R1/wr_address_reg[4]/C	R1/mem_1_reg[25][5]/CE	6.582	0.580	6.002	10.0

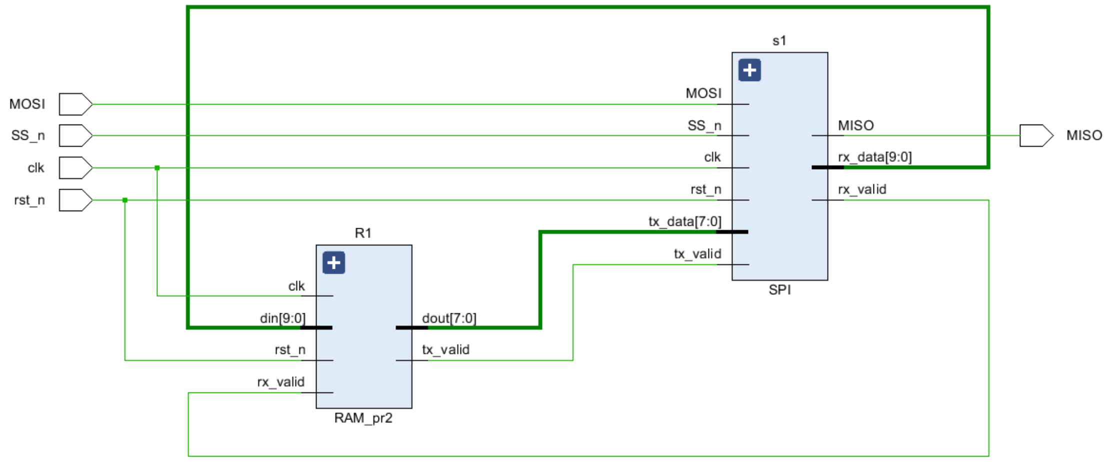
- ***Device_implementation_with_no_errors***

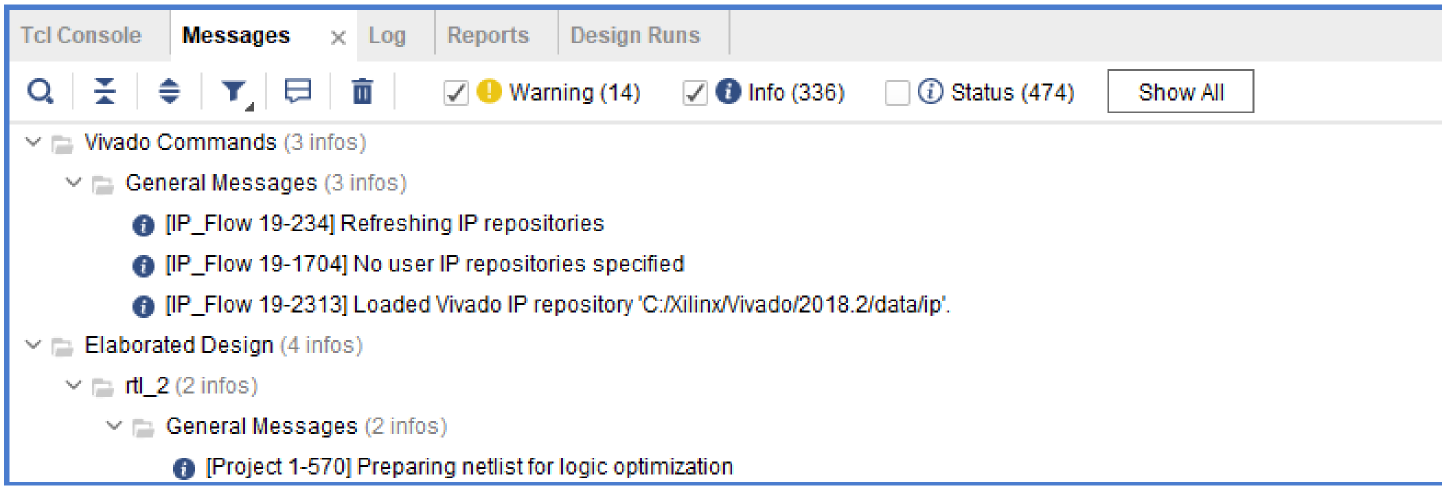




```
Vivado Commands (3 infos)
    General Messages (3 infos)
        [IP_Flow 19-234] Refreshing IP repositories
        [IP_Flow 19-1704] No user IP repositories specified
        [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Elaborated Design (7 warnings, 13 infos)
    rtl_1 (7 warnings, 11 infos)
        General Messages (7 warnings, 11 infos)
    rtl_2 (2 infos)
        General Messages (2 infos)
            [Project 1-570] Preparing netlist for logic optimization
            [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Synthesis (10 warnings, 132 infos)
    [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
    [Synth 8-6157] synthesizing module 'Master' [Master.v:1] (2 more like this)
    [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI.v:20]
```

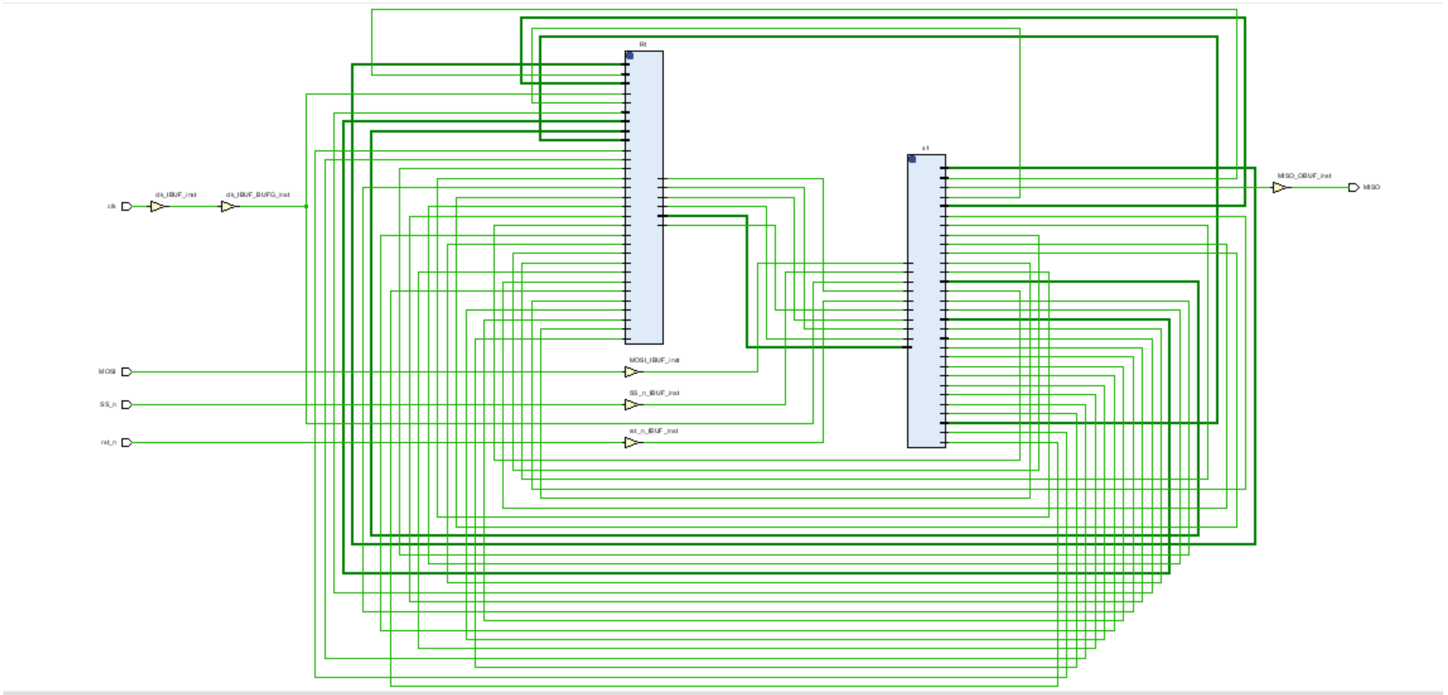
- *Sequential_encoding*
- ***Elaboration_with_no_errors***

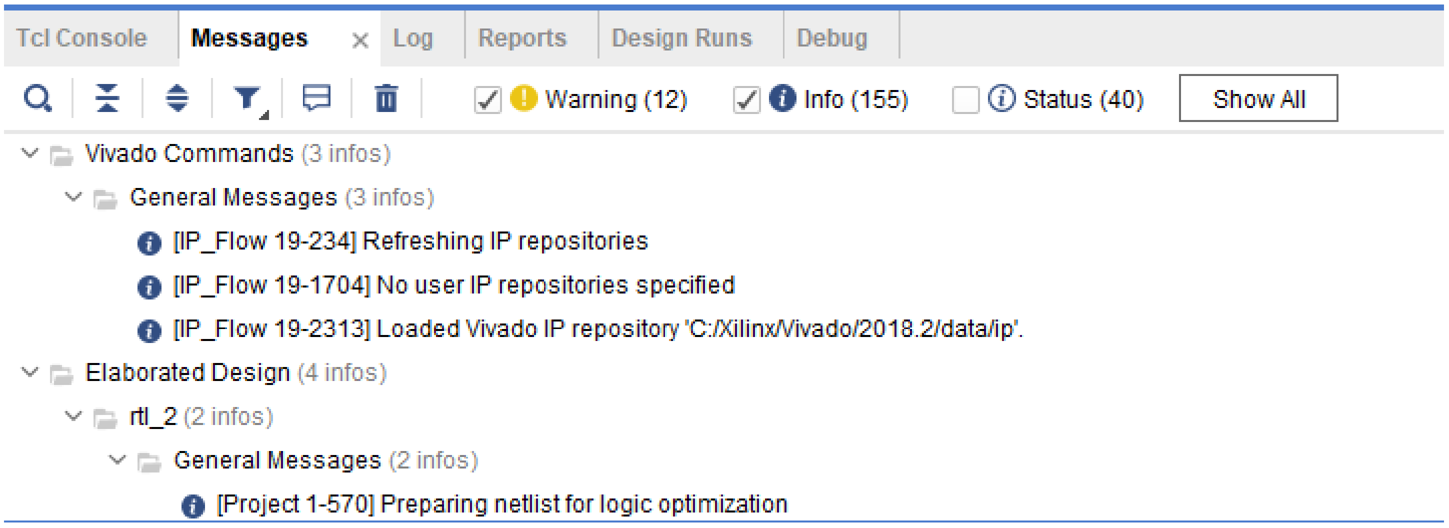




```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Elaborated Design (4 infos)
  rtl_2 (2 infos)
    General Messages (2 infos)
      [Project 1-570] Preparing netlist for logic optimization
```

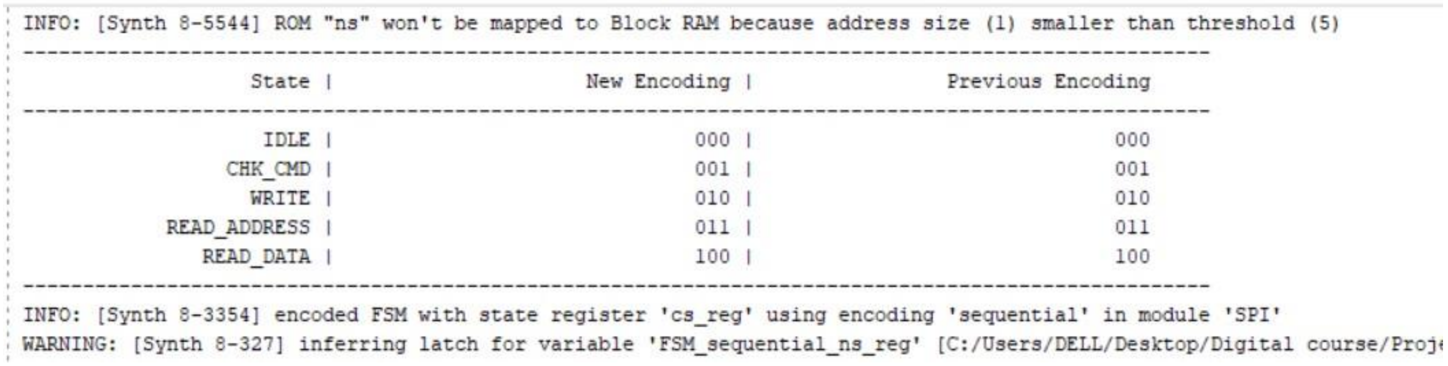
- ***Synthesis_schematic_with_no_errors***





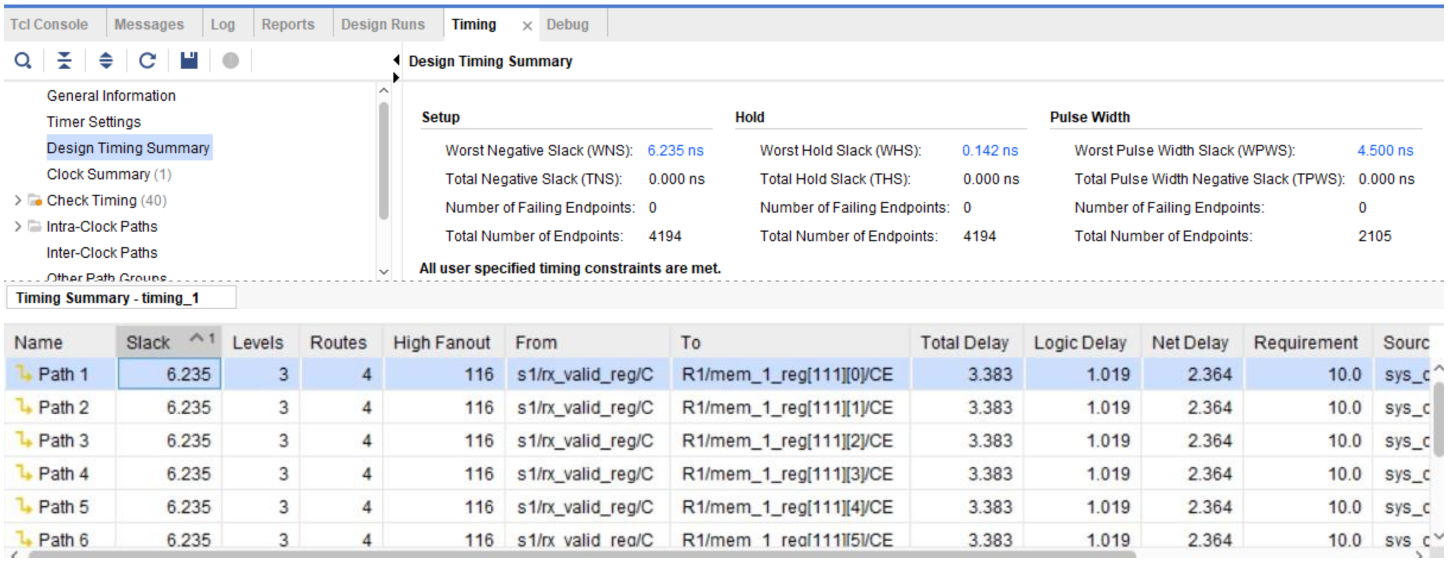
```
Vivado Commands (3 infos)
    General Messages (3 infos)
        [IP_Flow 19-234] Refreshing IP repositories
        [IP_Flow 19-1704] No user IP repositories specified
        [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Elaborated Design (4 infos)
    rtl_2 (2 infos)
        General Messages (2 infos)
            [Project 1-570] Preparing netlist for logic optimization
```

- ***Synthesis_Report***



```
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |                Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                              000
                 CHK_CMD |                              001 |                              001
                   WRITE |                              010 |                              010
            READ_ADDRESS |                              011 |                              011
               READ_DATA |                              100 |                              100
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_sequential_ns_reg' [C:/Users/DELL/Desktop/Digital course/Proj
```

- ***Synthesis_time_report***



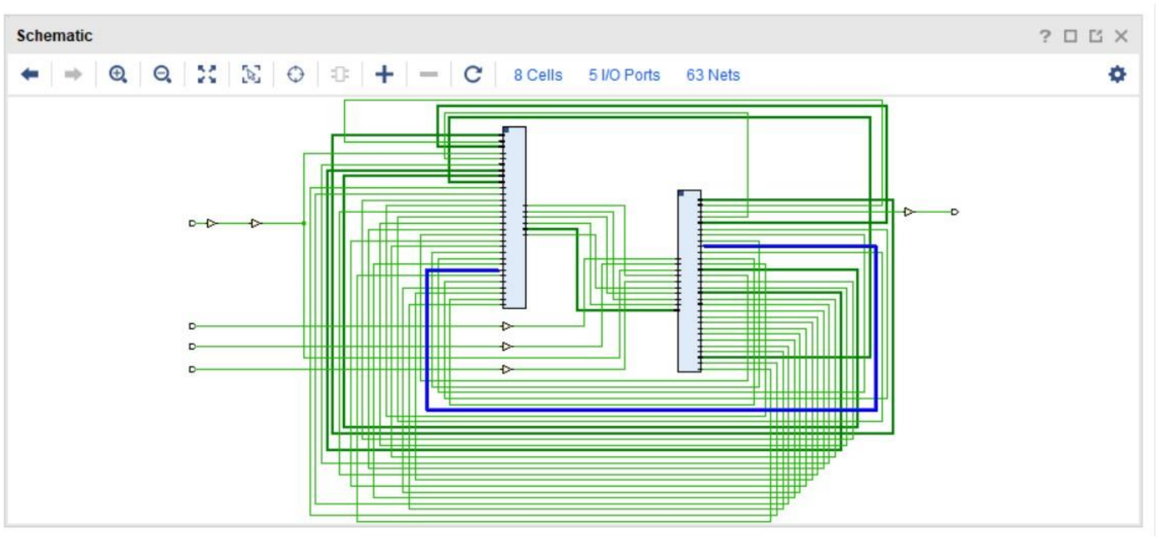
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.235 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4194	Total Number of Endpoints:	4194	Total Number of Endpoints:	2105

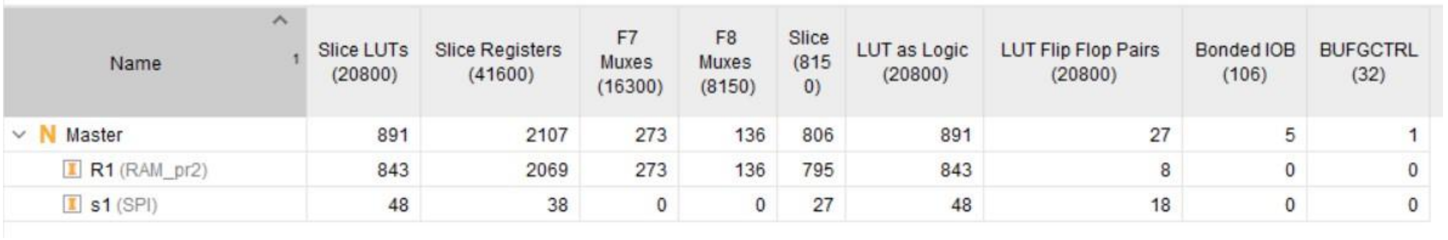
All user specified timing constraints are met.

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Sourc
Path 1	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][0]/CE	3.383	1.019	2.364	10.0	sys_c
Path 2	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][1]/CE	3.383	1.019	2.364	10.0	sys_c
Path 3	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][2]/CE	3.383	1.019	2.364	10.0	sys_c
Path 4	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][3]/CE	3.383	1.019	2.364	10.0	sys_c
Path 5	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][4]/CE	3.383	1.019	2.364	10.0	sys_c
Path 6	6.235	3	4	116	s1/rx_valid_reg/C	R1/mem_1_reg[111][5]/CE	3.383	1.019	2.364	10.0	sys_c

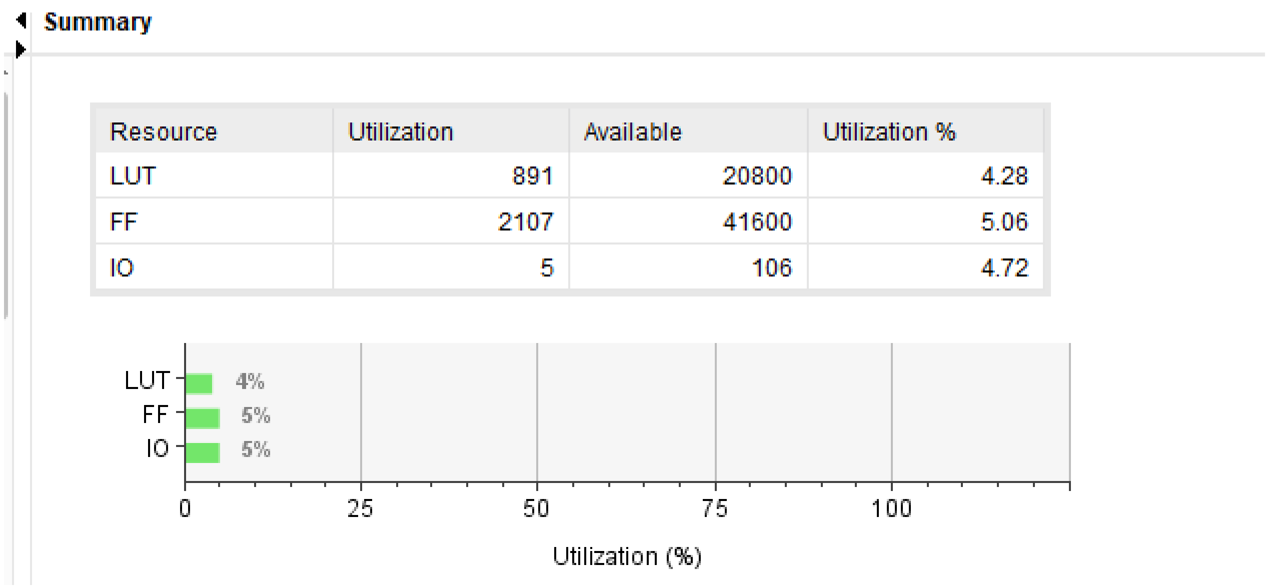
- ***Critical_Path***



- ***Report_utilization_after_implementation***



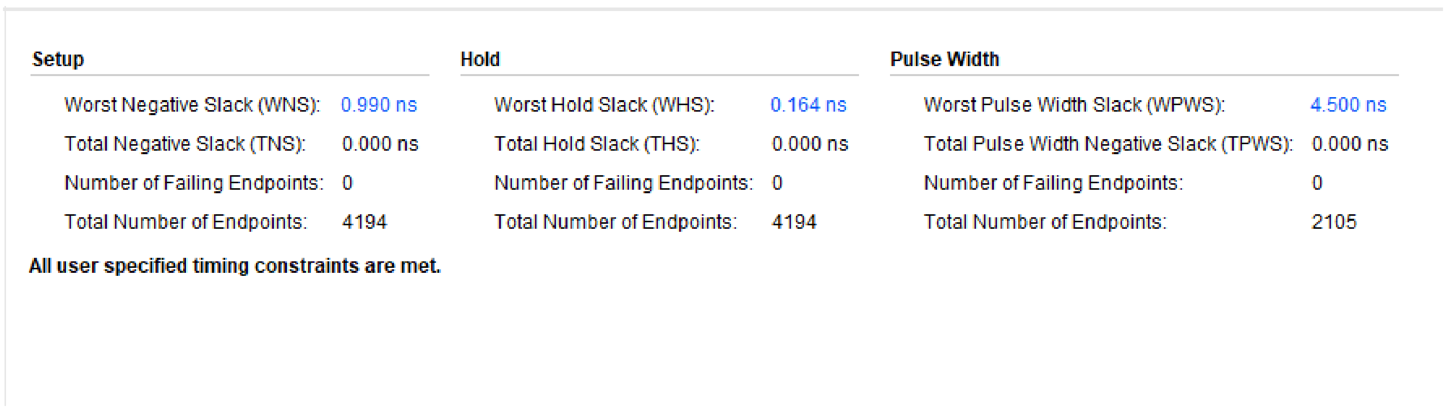
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
Master	891	2107	273	136	806	891	27	5	1
R1 (RAM_pr2)	843	2069	273	136	795	843	8	0	0
s1 (SPI)	48	38	0	0	27	48	18	0	0



Summary

Resource	Utilization	Available	Utilization %
LUT	891	20800	4.28
FF	2107	41600	5.06
IO	5	106	4.72

- ***implementation_time_report***



Setup

Worst Negative Slack (WNS):	0.990 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	4194

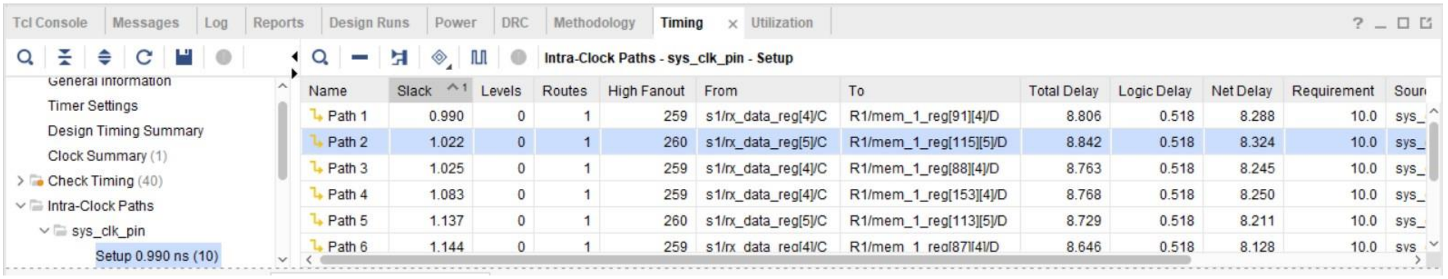
Hold

Worst Hold Slack (WHS):	0.164 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	4194

Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	2105

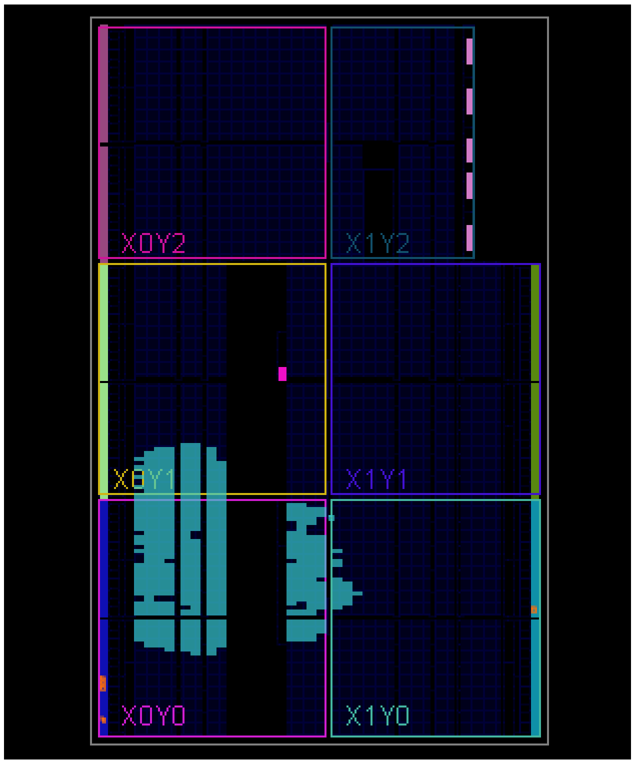
All user specified timing constraints are met.

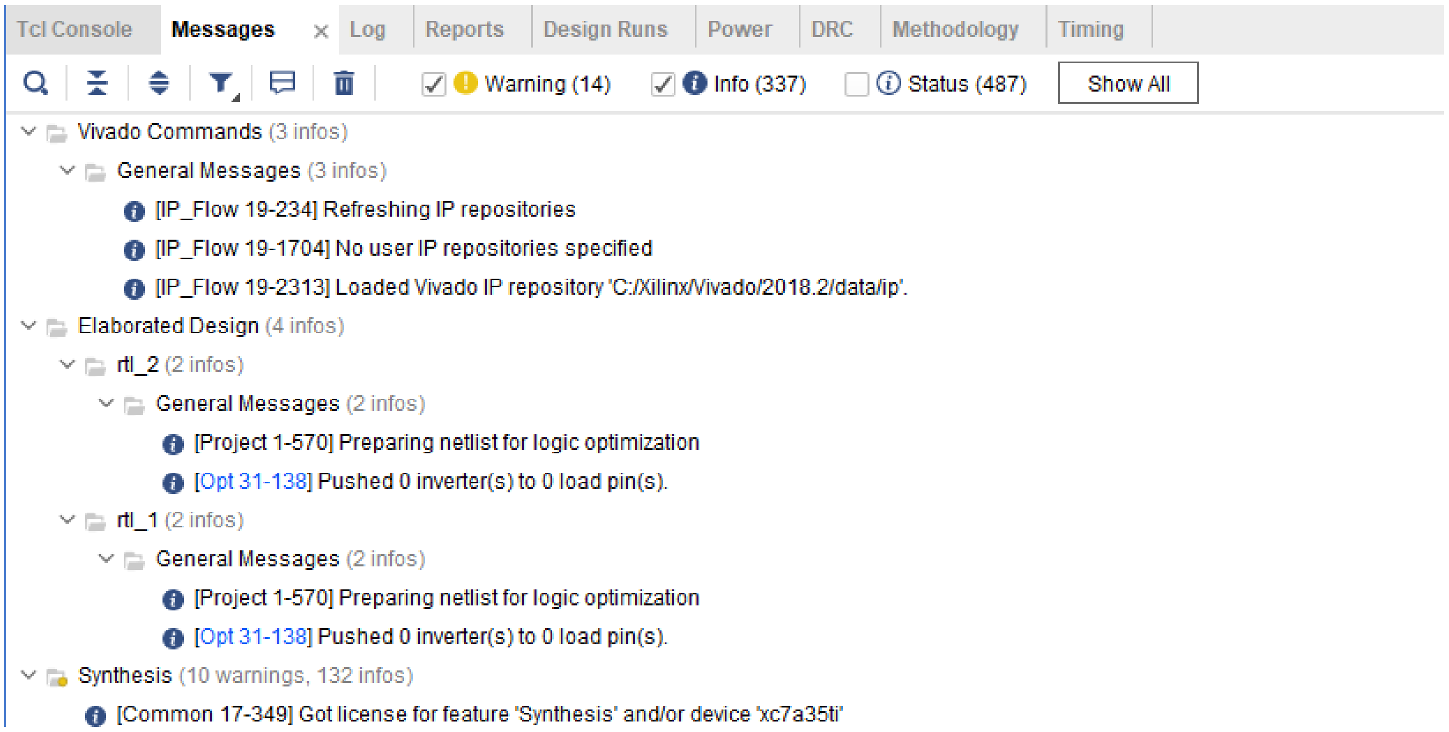


Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Sour
Path 1	0.990	0	1	259	s1/rx_data_reg[4]/C	R1/mem_1_reg[91][4]/D	8.806	0.518	8.288	10.0	sys_
Path 2	1.022	0	1	260	s1/rx_data_reg[5]/C	R1/mem_1_reg[115][5]/D	8.842	0.518	8.324	10.0	sys_
Path 3	1.025	0	1	259	s1/rx_data_reg[4]/C	R1/mem_1_reg[88][4]/D	8.763	0.518	8.245	10.0	sys_
Path 4	1.083	0	1	259	s1/rx_data_reg[4]/C	R1/mem_1_reg[153][4]/D	8.768	0.518	8.250	10.0	sys_
Path 5	1.137	0	1	260	s1/rx_data_reg[5]/C	R1/mem_1_reg[113][5]/D	8.729	0.518	8.211	10.0	sys_
Path 6	1.144	0	1	259	s1/rx_data_reg[4]/C	R1/mem_1_reg[87][4]/D	8.646	0.518	8.128	10.0	sys_

- ***Device_implementation_with_no_errors***





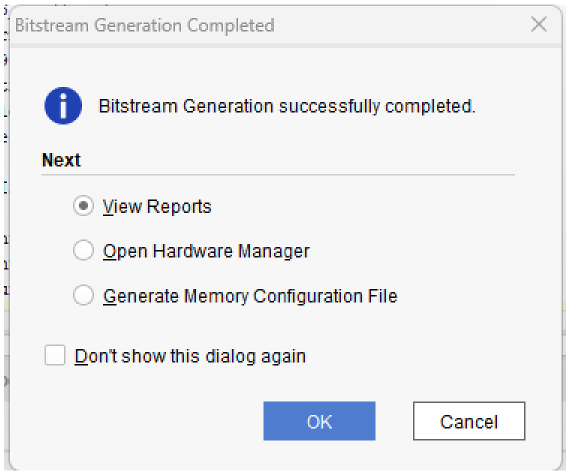
```
Vivado Commands (3 infos)
    General Messages (3 infos)
        [IP_Flow 19-234] Refreshing IP repositories
        [IP_Flow 19-1704] No user IP repositories specified
        [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Elaborated Design (4 infos)
    rtl_2 (2 infos)
        General Messages (2 infos)
            [Project 1-570] Preparing netlist for logic optimization
            [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    rtl_1 (2 infos)
        General Messages (2 infos)
            [Project 1-570] Preparing netlist for logic optimization
            [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Synthesis (10 warnings, 132 infos)
    [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
```

- ***Observation***

First

According to the setup time slack after implementation of each type of encoding we found that hot_one encoding has better setup time slack in the worst case(worst path) than that of gray and sequential encoding. So, we choose one_hot encoding then generate bit stream file .

- ***Generation of bit stream***


Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

- [✓ View Reports]
- Open Hardware Manager
- Generate Memory Configuration File

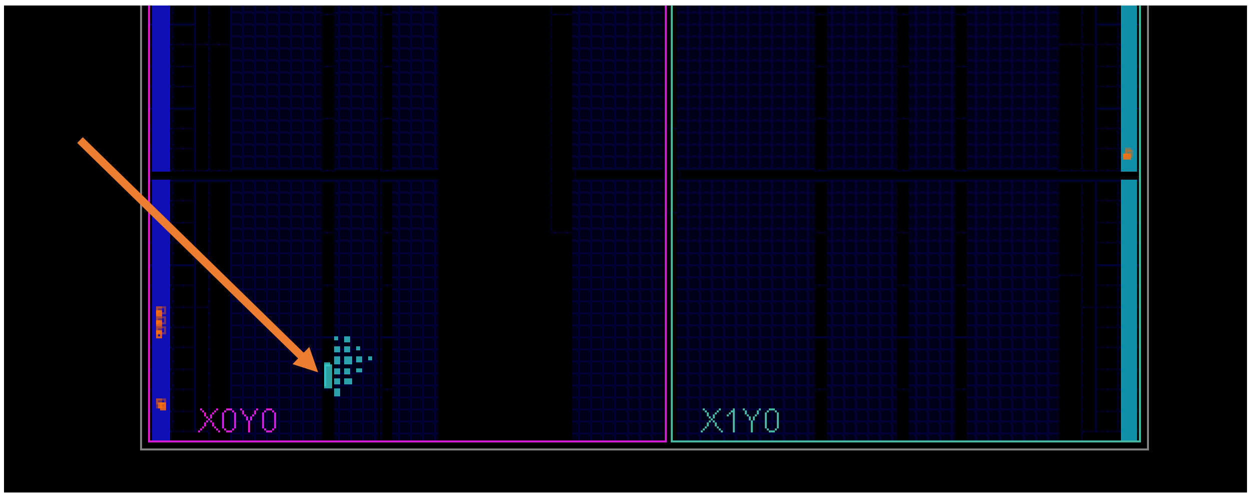
Don't show this dialog again

Second

we observe that no ram used in the implementation only many flipflops are used and that because of Asynchrouns reset is not supported in the FPGA KIT used.

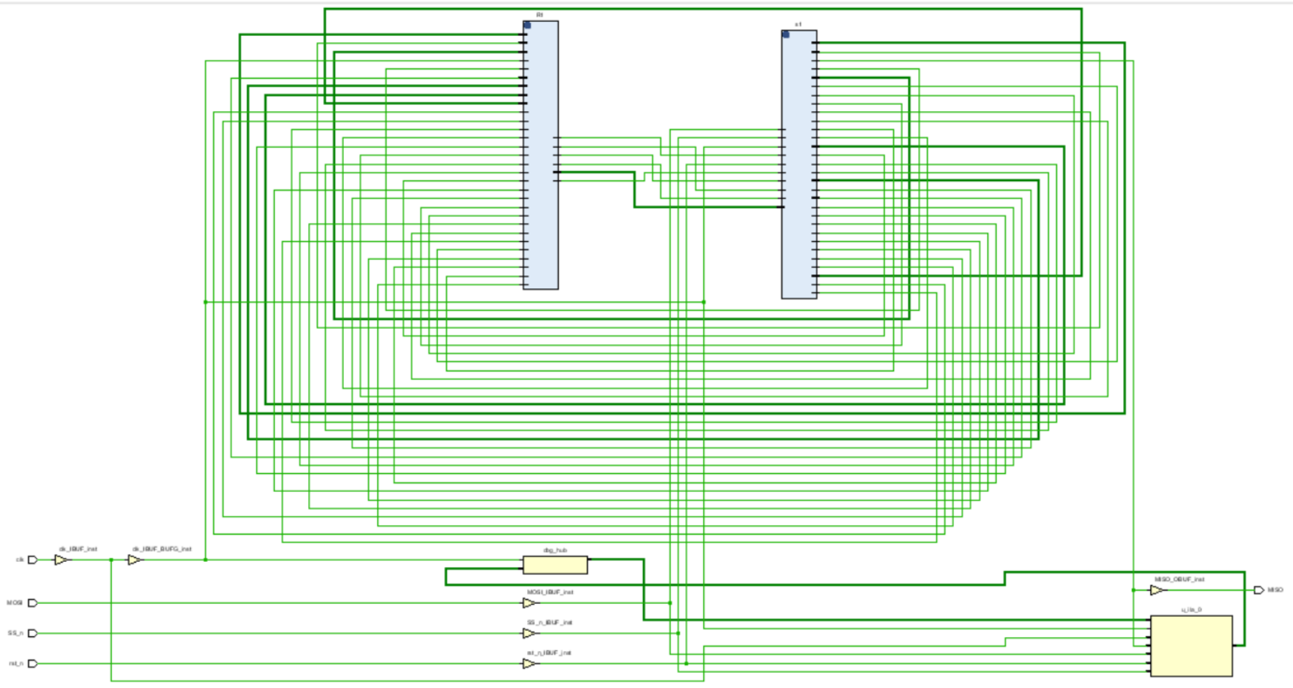
So, we make reset synchronized with clk to check that ram is used during implementation.

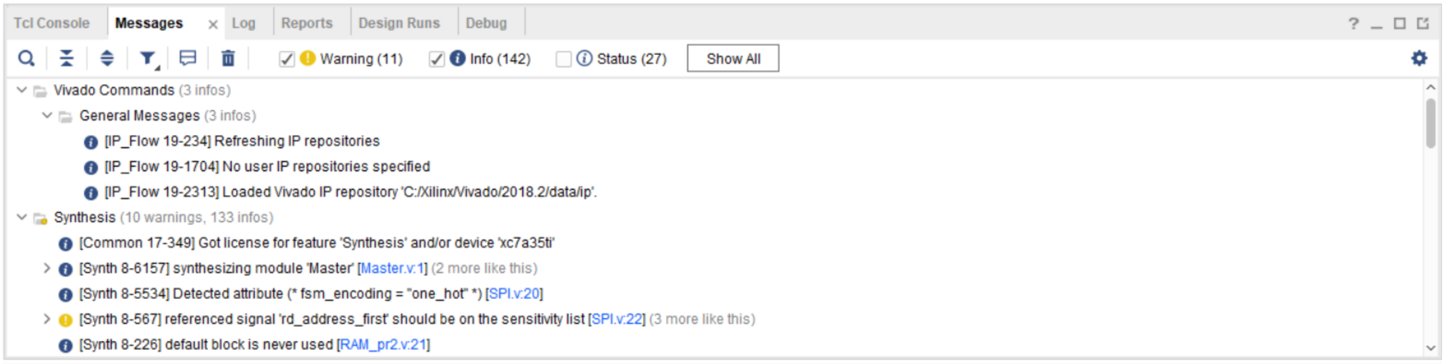
An arrow points to the ram used during implementation as shown below



Synthesis&Debug of one_hot_encoding after comparison

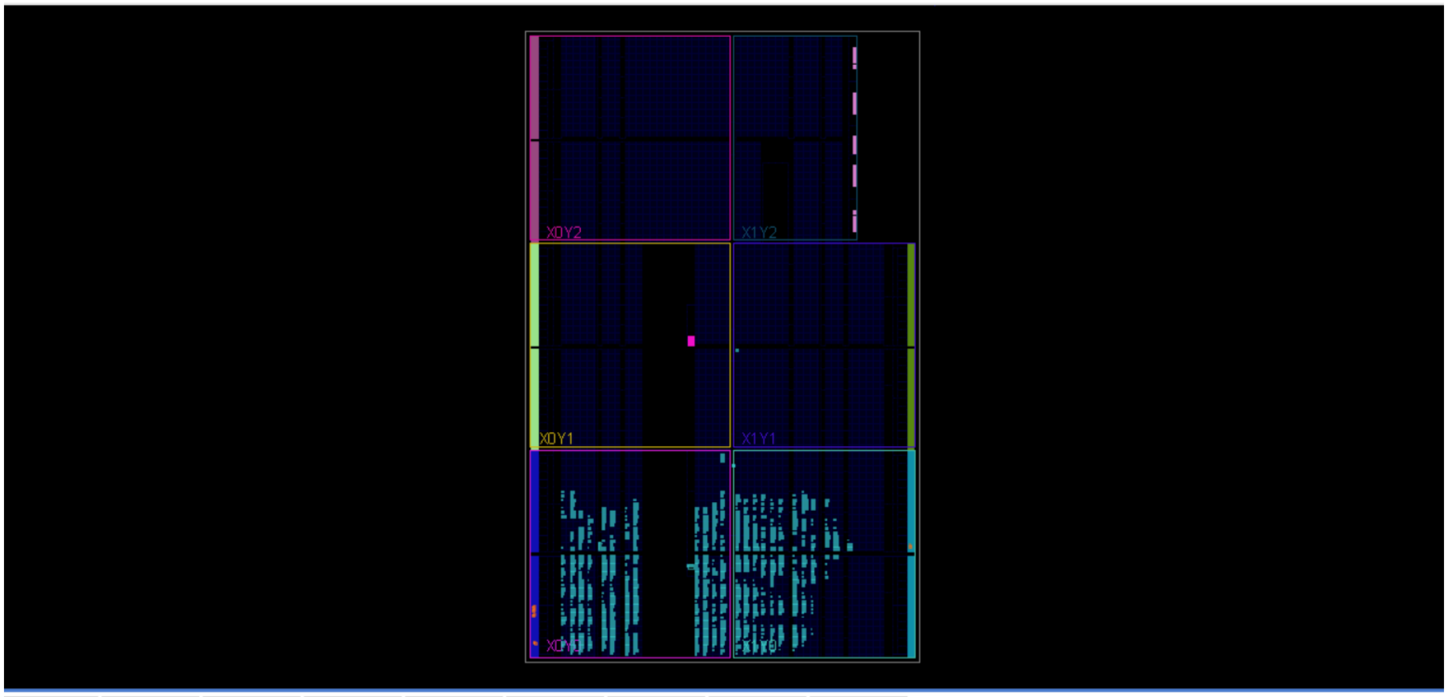
- ***Synthesis_schematic_with_debug_cores_no_errors***

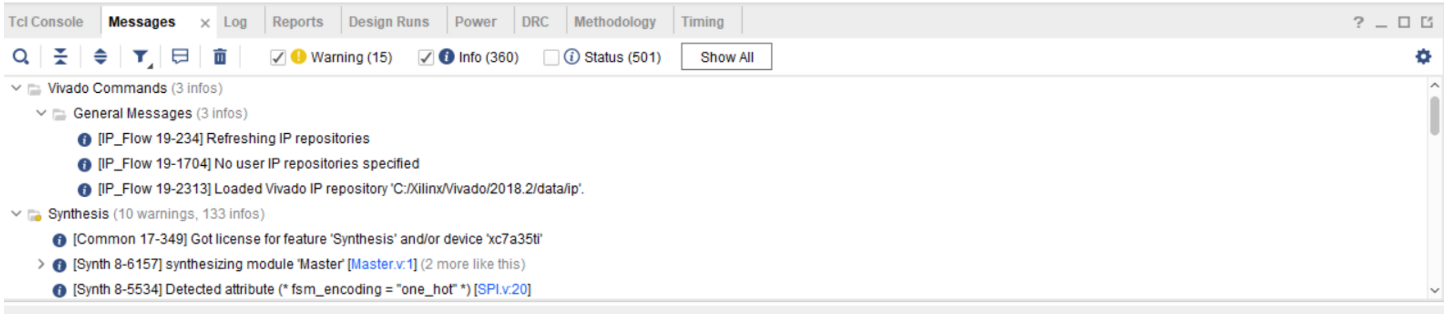




```
Vivado Commands (3 infos)
    General Messages (3 infos)
        [IP_Flow 19-234] Refreshing IP repositories
        [IP_Flow 19-1704] No user IP repositories specified
        [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Synthesis (10 warnings, 133 infos)
    [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
    [Synth 8-6157] synthesizing module 'Master' [Master.v:1] (2 more like this)
    [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI.v:20]
    [Synth 8-567] referenced signal 'rd_address_first' should be on the sensitivity list [SPI.v:22] (3 more like this)
    [Synth 8-226] default block is never used [RAM_pr2.v:21]
```

- ***Device_implementation_with_debug_cores_no_errors***





```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
Synthesis (10 warnings, 133 infos)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  [Synth 8-6157] synthesizing module 'Master' [Master.v:1] (2 more like this)
  [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI.v:20]
```