DSP_PROJECT

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- ***Code:***

```
module project_1
(A,B,D,C,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA
,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
parameter A0REG=0;
parameter A1REG=1;
parameter B0REG=0;
parameter B1REG=1;
parameter CREG=1;
parameter MREG=1;
parameter DREG=1;
parameter PREG=1;
parameter CARRYINREG=1;
parameter CARRYOUTREG=1;
parameter OPMODEREG=1;
parameter CARRINYSEL="OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE ="SYNC";

input
CLK,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEP,CEC,CED,CEM,CARRYIN,
CECARRYIN,CEOPMODE;
input [17:0]A,B,D,BCIN;
input [7:0] OPMODE;
input [47:0]C,PCIN;
output [17:0] BCOUT;
output  [47:0] PCOUT,P;
output  CARRYOUT,CARRYOUTF;
output  [35:0] M;

wire [17:0] B_MUX;
wire[17:0] A_REG;
wire[17:0] B_REG;
wire[17:0] D_REG;
wire [47:0] C_REG;
wire [7:0] OPMODE_REG;
wire [17:0] result_REG;
wire [17:0] A_REG2;
wire [35:0] multiply_REG;
wire CARRY_IN_MUX;
wire CARRYIN_REG;
reg [17:0] add_sub;
reg [17:0] result;
reg[35:0] multiply;
reg[47:0] X;
reg [47:0]Z;
reg [47:0] add_sub_2;
reg cout;
assign B_MUX= (B_INPUT == "DIRECT")? B: (B_INPUT == "CASCADE")? BCIN:0;
```

```
assign  CARRY_IN_MUX= (CARRINYSEL=="OPMODE5")? OPMODE_REG[5]:
(CARRINYSEL=="CARRYIN")?CARRYIN:1'b0;
ff #(.width(18),.DREG(A0REG),.RSTTYPE(RSTTYPE)) A0( CLK,CEA ,RSTA,A,A_REG);
ff #(.width(18),.DREG(B0REG),.RSTTYPE(RSTTYPE)) B0( CLK,CEB ,RSTB,B_MUX,B_REG);
ff #(.width(48),.DREG(CREG),.RSTTYPE(RSTTYPE)) C_ff ( CLK,CEC ,RSTC,C,C_REG);
ff #(.width(18),.DREG(DREG),.RSTTYPE(RSTTYPE)) D_ff( CLK,CED ,RSTD,D,D_REG);
ff #(.width(8),.DREG(OPMODEREG),.RSTTYPE(RSTTYPE)) OPMODE_ff ( CLK,CEOPMODE
,RSTOPMODE,OPMODE,OPMODE_REG);
ff #(.width(18),.DREG(B1REG),.RSTTYPE(RSTTYPE)) B1 ( CLK,CEB ,RSTB,result,result_REG);
ff #(.width(18),.DREG(A1REG),.RSTTYPE(RSTTYPE)) A1( CLK,CEA ,RSTA,A_REG,A_REG2);
ff #(.width(36),.DREG(MREG),.RSTTYPE(RSTTYPE)) M_ff( CLK,CEM
,RSTM,multiply,multiply_REG);
ff #(.width(1),.DREG(CARRYINREG),.RSTTYPE(RSTTYPE)) CARRYIN_ff( CLK,CECARRYIN
,RSTCARRYIN,CARRY_IN_MUX,CARRYIN_REG);
ff #(.width(48),.DREG(PREG),.RSTTYPE(RSTTYPE)) P_ff( CLK,CEP ,RSTP,add_sub_2,P);
ff #(.width(1),.DREG(CARRYOUTREG),.RSTTYPE(RSTTYPE)) CARRYOUT_ff( CLK,CECARRYIN
,RSTCARRYIN,cout,CARRYOUT);
assign CARRYOUTF=CARRYOUT;
assign PCOUT= P;
assign BCOUT= result_REG;
assign M=multiply_REG;
always@(*)
begin

if(!OPMODE_REG[6])
add_sub= D_REG+B_REG;
else
add_sub=D_REG-B_REG;

if(OPMODE_REG[4])
result= add_sub;
else
result= B_REG;

end

always@(*)
begin
    multiply=A_REG2*result_REG;
end

always@ (*)
begin
case(OPMODE_REG[1:0])
2'b00:X=0;
2'b01:X=multiply_REG;
2'b10:X=P;
2'b11:X={D_REG,A_REG2,result_REG};
endcase

```

```
end
always@(*)
begin
    case(OPMODE_REG[3:2])
    2'b00:Z=0;
    2'b01:Z=PCIN;
    2'b10:Z=P;
    2'b11:Z=C_REG;

endcase
end
always@(*)
begin
    if(!OPMODE_REG[7])

 {cout,add_sub_2}= X+Z+CARRYIN_REG;
 else
  {cout,add_sub_2}=Z-(X+CARRYIN_REG);
end


endmodule
```

- ***FF_Code:***

```
module ff( clk,en ,rst,D,Q);
parameter width=1;
parameter DREG=0;
parameter RSTTYPE="SYNC";
input clk,rst,en;
input [width-1:0]D;
output [width-1:0]Q;
reg [width-1:0] tmp;
generate
    if(RSTTYPE=="SYNC")
    begin
 always@(posedge clk)
begin

   if(rst)

    tmp<=0;
    else if(en)
    tmp<=D;
   end
end

else
begin
always@(posedge clk,posedge rst)
begin
```

```
    if(rst)

     tmp<=0;
     else if(en)
     tmp<=D;

    end
end
    endgenerate
    assign Q = (DREG)? tmp:D;

endmodule

```

- ***Tb_Code:***

```
module project_1_tb();
parameter A0REG=0;
parameter A1REG=0;
parameter B0REG=0;
parameter B1REG=0;
parameter CREG=0;
parameter MREG=0;
parameter DREG=0;
parameter PREG=0;
parameter CARRYINREG=0;
parameter CARRYOUTREG=0;
parameter OPMODEREG=0;
parameter CARRINYSEL="OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE ="ASYNC";

reg
CLK,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEP,CEC,CED,CEM,CARRYIN,
CECARRYIN,CEOPMODE;
reg [17:0]A,B,D,BCIN;
reg [7:0] OPMODE;
reg [47:0]C,PCIN;

wire [17:0] BCOUT;
wire  [47:0] PCOUT,P;
wire  CARRYOUT,CARRYOUTF;
wire  [35:0] M;
 project_1
#(A0REG,A1REG,B0REG,B1REG,CREG,MREG,DREG,PREG,CARRYINREG,CARRYOUTREG,OPMODEREG,CARRINYS
EL,B_INPUT,RSTTYPE) P1(A,B,D,C,CLK,CARRYIN,OPMODE,
    BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CEC
ARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
 initial begin
    CLK=0;
    forever begin
```

```
    #1 CLK=~CLK;
    end
    end

initial begin
//Reset all registers && initial values.
RSTA=1'b1;
RSTB=1'b1;
RSTM=1'b1;
RSTP=1'b1;
RSTC=1'b1;
RSTD=1'b1;
RSTCARRYIN=1'b1;
RSTOPMODE=1'b1;
//Enables
CEA=1'b0;
CEB=1'b0;
CEM=1'b0;
CEP=1'b0;
CEC=1'b0;
CED=1'b0;
CECARRYIN=1'b0;
CEOPMODE=1'b0;
//inputs
A=1'b0;
B=1'b0;
BCIN=1'b0;
C=1'b0;
D=1'b0;
PCIN=1'b0;
OPMODE=1'b0;
CARRYIN=1'b0;
#20;
RSTA=1'b0;
RSTB=1'b0;
RSTM=1'b0;
RSTP=1'b0;
RSTC=1'b0;
RSTD=1'b0;
RSTCARRYIN=1'b0;
RSTOPMODE=1'b0;
CEA=1'b1;
CEB=1'b1;
CEM=1'b1;
CEP=1'b1;
CEC=1'b1;
CED=1'b1;
CECARRYIN=1'b1;
CEOPMODE=1'b1;
#10;
```

```
RSTA=1'b0;
RSTB=1'b0;
RSTM=1'b0;
RSTP=1'b0;
RSTC=1'b0;
RSTD=1'b0;
RSTCARRYIN=1'b0;
RSTOPMODE=1'b0;
OPMODE=8'b10100111;
B=4;
PCIN=10;
A=1'b0;
BCIN=0;
C=0;
D=0;
CARRYIN=1'b0;
#20;
//test that the value of pre_adder will pass to post_adder and the value of C&Carry_in will be passed.
OPMODE=8'b00011101;
B=4'd10;
D=4'd9;
A=4'd3;
C=4'd3;
CARRYIN=1'b1;
#20;
//test that the value of pre_subtractor will pass to post_subtractor and the value of PCin&Carry_in will be passed.
OPMODE=8'b11010101;
B=4'd10;
D=5'd20;
A=4'd6;
PCIN=10'd600;
CARRYIN=1'b0;
#20;
//test Zero condition.
OPMODE=8'b11010000;
#10;
//Passing B to multiplier passing P to post_adder
OPMODE=8'b11001010;
B=4'd14;
A=4'd10;
#20;
//
OPMODE=8'b00111111;
B=5;
A=0;
D=0;
C=3;
CARRYIN=0;
```

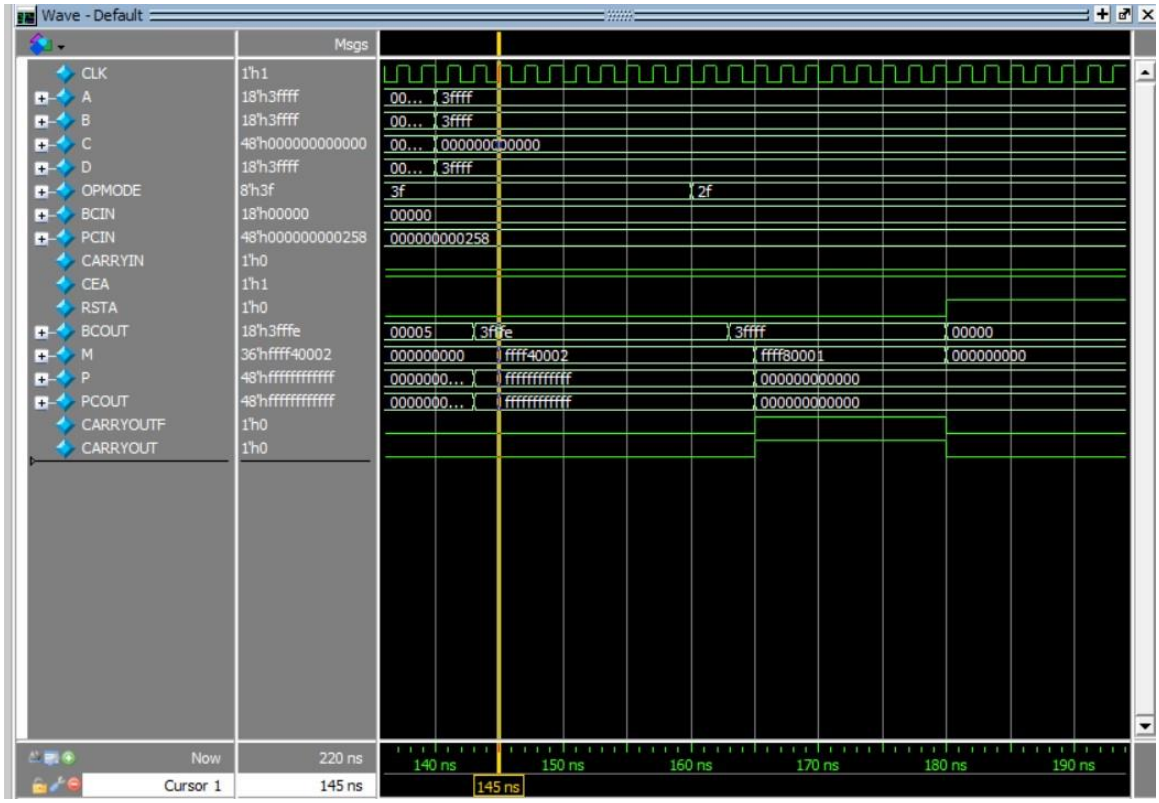
```
  #20;

  OPMODE=8'b00111111;
  B=18'b1111_1111_1111_1111_11;
  A=18'b1111_1111_1111_1111_11;
  D=18'b1111_1111_1111_1111_11;
  C=0;
  #20;
  OPMODE=8'b00101111;
  B=18'b1111_1111_1111_1111_11;
  A=18'b1111_1111_1111_1111_11;
  D=18'b1111_1111_1111_1111_11;
  C=0;
  #20;
  RSTA=1'b1;
  RSTB=1'b1;
  RSTM=1'b1;
  RSTP=1'b1;
  RSTC=1'b1;
  RSTD=1'b1;
  RSTCARRYIN=1'b1;
  RSTOPMODE=1'b1;
  #20;
  RSTA=1'b0;
  RSTB=1'b0;
  RSTM=1'b0;
  RSTP=1'b0;
  RSTC=1'b0;
  RSTD=1'b0;
  RSTCARRYIN=1'b0;
  RSTOPMODE=1'b0;
  OPMODE=8'b10100111;
  B=4;
  PCIN=10;
  A=1'b0;
  BCIN=0;
  C=0;
  D=0;
  CARRYIN=1'b0;
  #20;

   $stop;

  end
  initial begin
  $monitor("CLK=%b,rst=%b,enable=%b,OPMODE=%b,A=%d,B=%d,C=%d,D=%d,CARRYIN=%b,BCIN=%b,PCIN
  =%b,BCOUT=%d,M=%d,P=%d,PCOUT=%d,CARRYOUT=%b,CARRYOUTF=%b",CLK,RSTA,CEA,OPMODE,A,B,C,D,C
  ARRYIN,BCIN,PCIN,BCOUT,M,P,PCOUT,CARRYOUT,CARRYOUTF);
  end
  endmodule
```

- ***DO_FILE:***

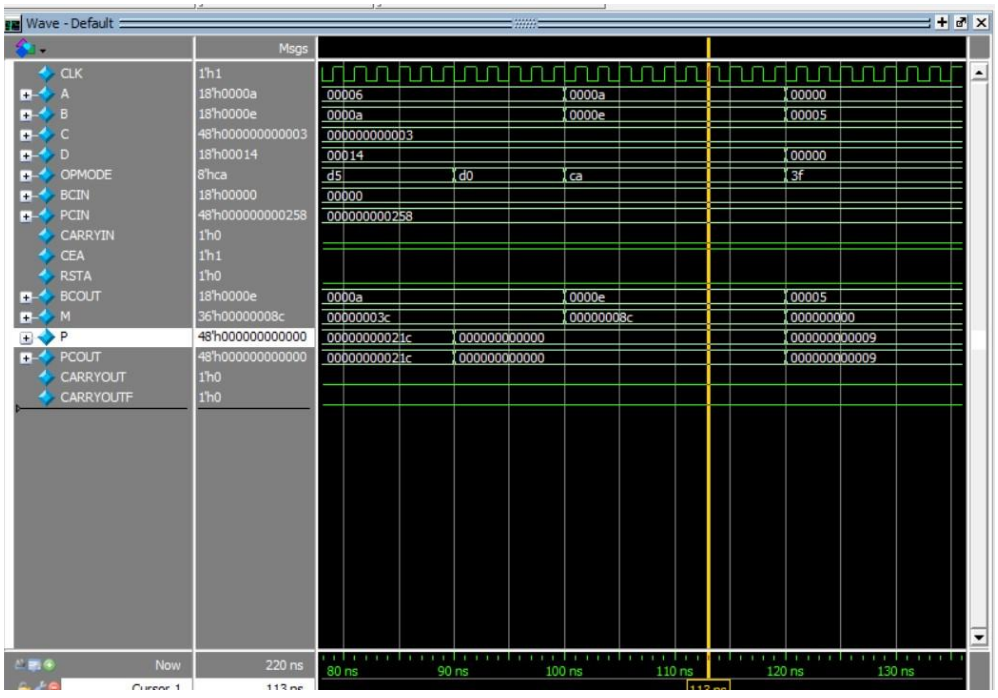
```
vlib work
vlog D_FF.v project1_code.v project1_tb.v
vsim -voptargs=+acc work.project_1_tb
add wave *
run -all
```

- **Snnipets_of_waveform:**

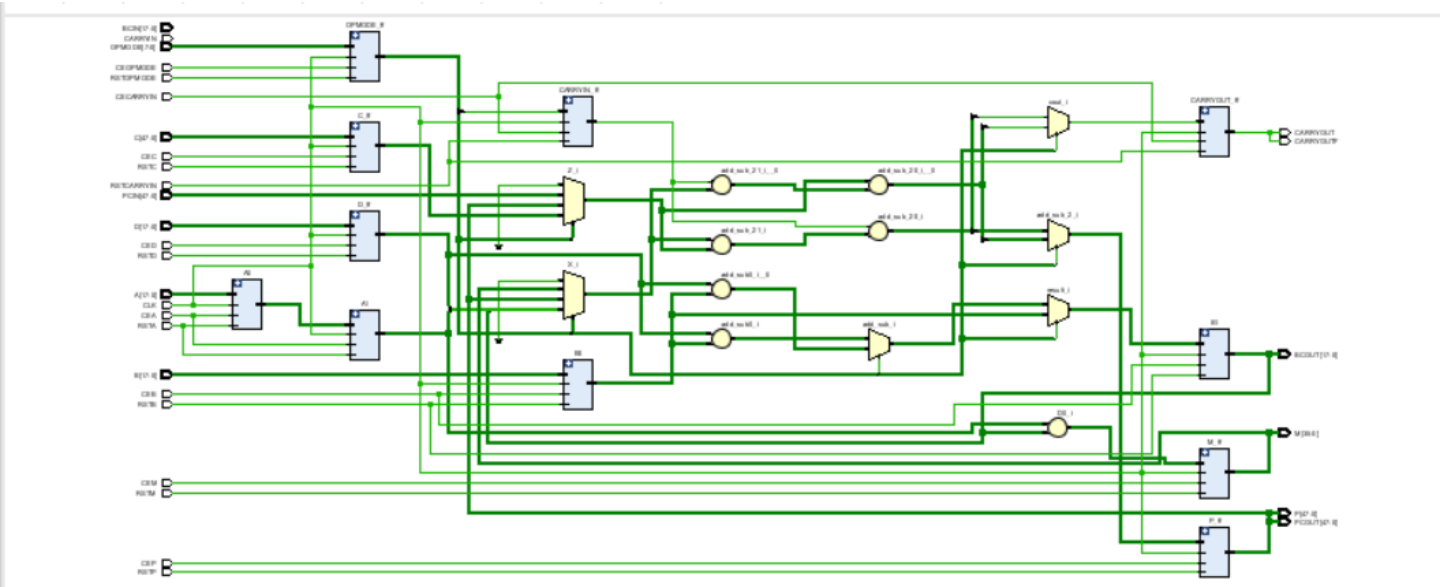
I. FOR PIPELINE:



II. For NO_PIPELINE:



- ***Vivado:***
  - ***Elaboration_with_no_errors***

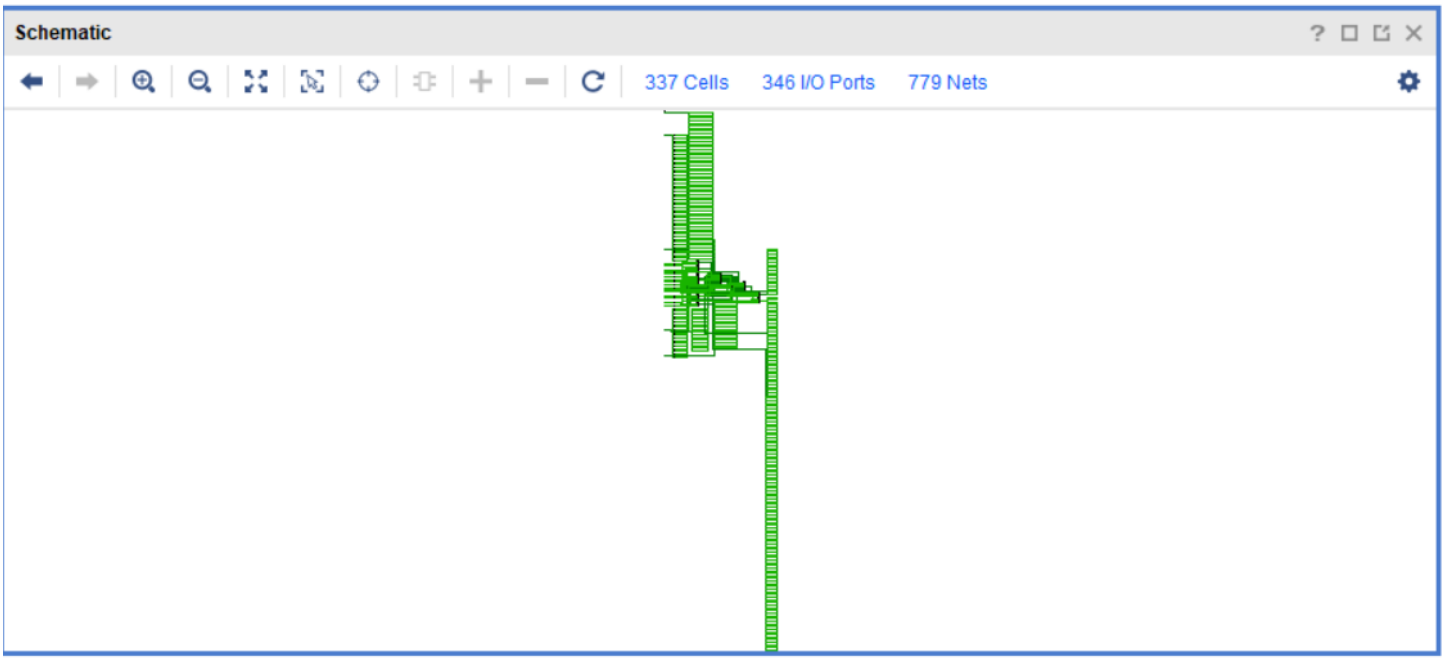


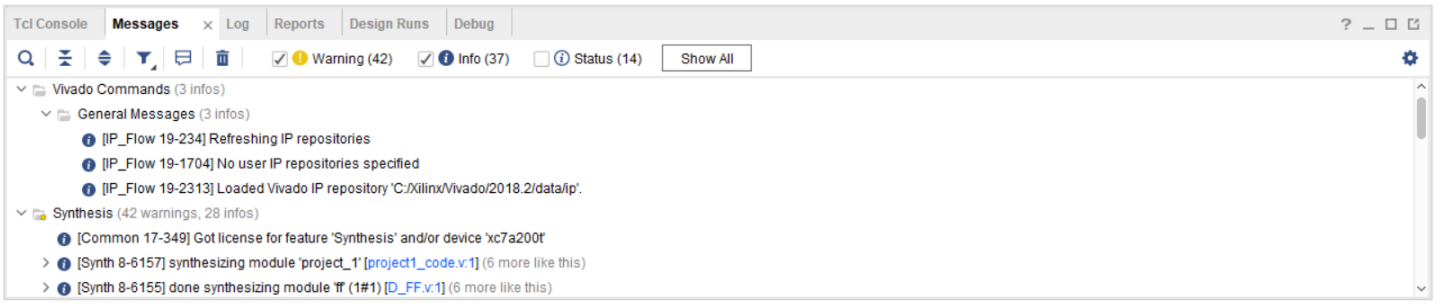
Tcl Console | **Messages** | Log | Reports | Design Runs

Warning (76) | Info (199) | Status (373) | Show All

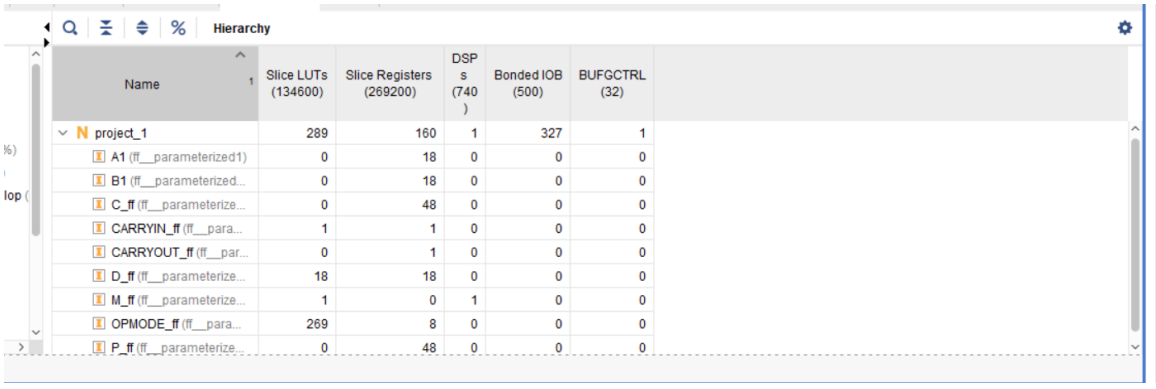
- Vivado Commands (3 infos)
  - General Messages (3 infos)
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- Elaborated Design (22 warnings, 18 infos)
  - General Messages (22 warnings, 18 infos)
    - [Synth 8-6157] synthesizing module 'project_1' [project1_code.v:1] (6 more like this)
    - [Synth 8-6155] done synthesizing module 'ff' (1#1) [D_FF.v:1] (6 more like this)

- **Synthesis_schematic_with_no_errors**



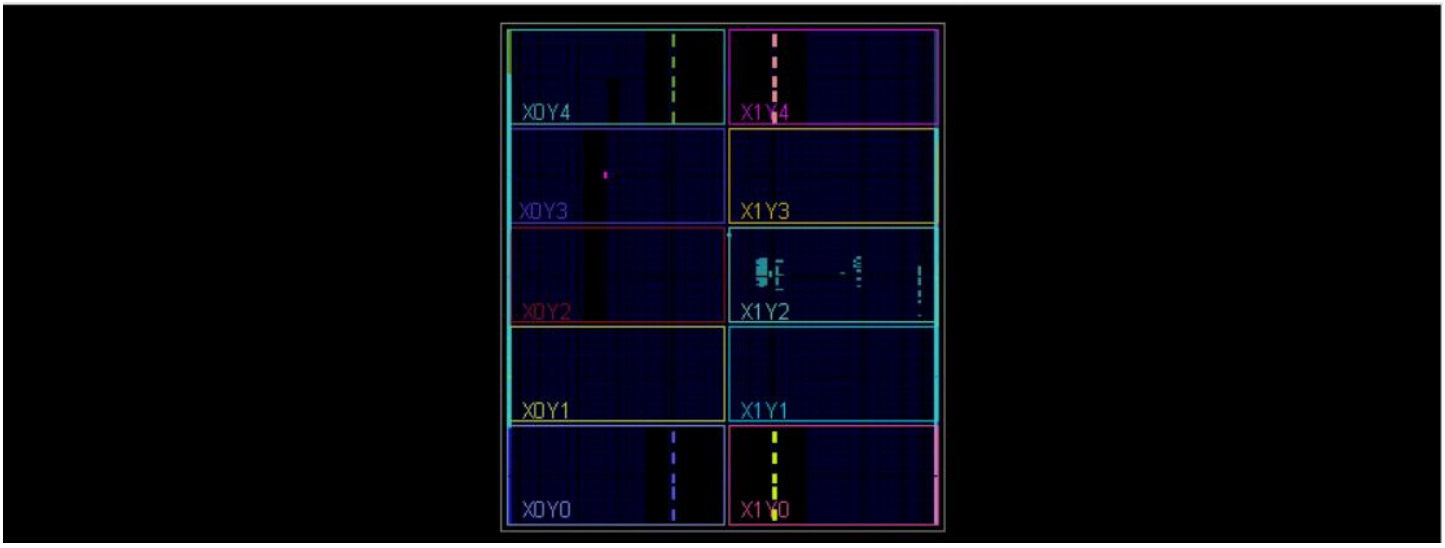


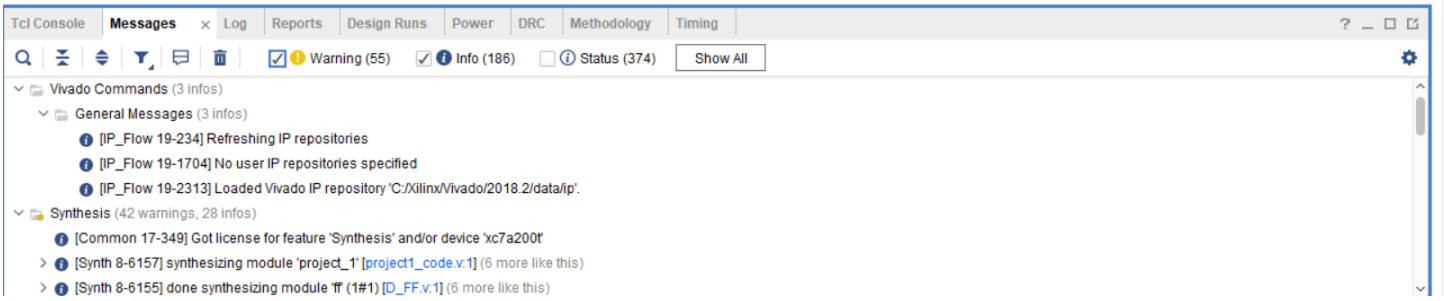
- **Report_utilization_after_synthesis**



Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
project_1	289	160	1	327	1
A1 (ff__parameterized1)	0	18	0	0	0
B1 (ff__parameterized...	0	18	0	0	0
C_ff (ff__parameterize...	0	48	0	0	0
CARRYIN_ff (ff__para...	1	1	0	0	0
CARRYOUT_ff (ff__par...	0	1	0	0	0
D_ff (ff__parameterize...	18	18	0	0	0
M_ff (ff__parameterize...	1	0	1	0	0
OPMODE_ff (ff__para...	269	8	0	0	0
P_ff (ff__parameterize...	0	48	0	0	0

- **Device_implementation_with_no_errors**





- **Report_utilization_after_implementation**