SONY

2SK152

Silicon N-Channel Junction FET

Description

The 2SK152 is the first device to reach such a high "Figure of merit" level. Because it uses the latest Epitaxy and Pattern technology.

Head amplifiers Video Cameras VTRs etc. perform very efficiently.

Features

- High figure of merit

$V_{DS}=5V$, $I_D=10mA$	$\|Y_{fs}\|/C_{iss}$	3.5	(Typ.)

- High $\|Y_{fs}\|$

$V_{DS}=5V$, $V_{GS}=0V$	$\|Y_{fs}\|$	30mS	(Typ.)

- Low input capacitance

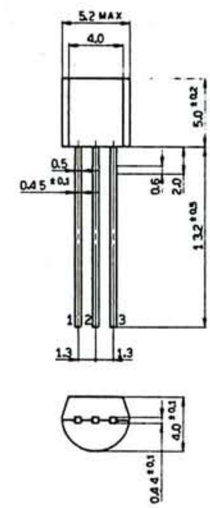
	C_{iss}	8pF	(Typ.)

Structure

Silicon N-Channel junction FET.

Package Outline

Unit: mm



1:Drain
2:Source
3:Gate

M-230

Absolute Maximum Ratings (Ta = 25°C)

• Drain to gate voltage	V_{DGO}	15	V
• Source to gate voltage	V_{SGO}	15	V
• Drain current	I_D	50	mA
• Gate current	I_G	5	mA
• Junction temperature	T_j	100	°C
• Storage temperature	T_{stg}	−50 to +120	°C
• Allowable power dissipation	P_D	300	mW

Electrical Characteristics

Ta = 25°C

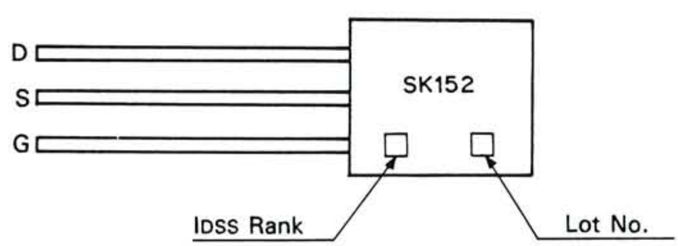
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain to gate voltage	V_{DGO}	$I_G = 10\mu A$	15			V
Source to gate voltage	V_{SGO}	$I_G = 10\mu A$	15			V
Gate cutoff current	I_{GSS}	$V_{GS} = -7V$, $V_{DS} = 0V$			−2	nA
Drain current	I_{DSS}	$V_{DS} = 5V$, $V_{GS} = 0V$	9.5		42	mA*
Gate to source cutoff voltage	$V_{GS(OFF)}$	$V_{DS} = 5V$, $I_D = 100\mu A$	−0.55		−2.0	V
Forward transfer admittance	$\|Y_{fs}\|$	$V_{DS} = 5V$, $V_{GS} = 0V$, f = 1kHz	21	30		mS
Input capacitance	C_{iss}	$V_{DS} = 5V$, $V_{GS} = 0V$, f = 1MHz		8	9	pF

*Note) Drain current detail specification as follows.

Classification

Rank	I_{DSS}(mA) $V_{DS} = 5V$ $V_{GS} = 0V$
1	9.5 to 14.8
2	13.4 to 21.0
3	19.0 to 30.2
4	27.4 to 42.0

Mark

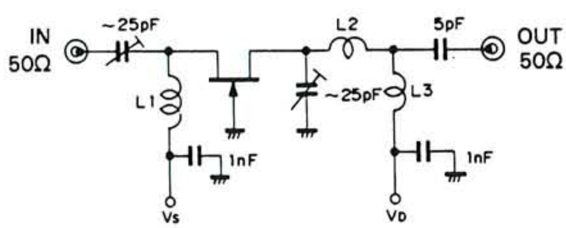


Standard Circuit Design Data

Ta = 25°C

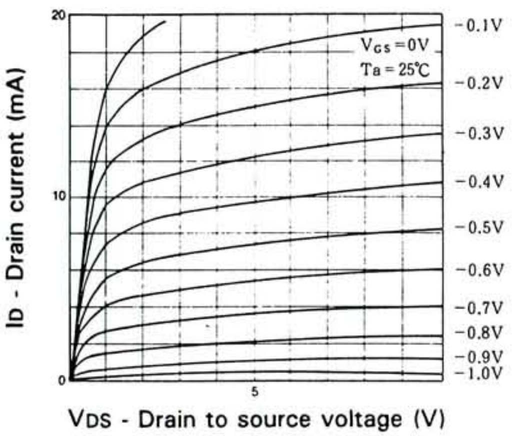
Item	Symbol	Condition	Typ.	Unit
Forward transfer admittance	$\lvert Y_{fs} \rvert$	$V_{DS}=5V$, $I_D=10mA$, $f=1kHz$	25	mS
Input capacitance	C_{iss}	$V_{DS}=5V$, $I_D=10mA$, $f=1MHz$	7.2	pF
Gate cutoff current	I_G	$V_{DG}=5V$, $I_D=10mA$	40	pA
Input resistance	r_{is}	$V_{DS}=5V$, $I_D=10mA$, $f=100MHz$	3.5	kΩ
Input capacitance	C_{is}		7.2	pF
Output resistance	r_{os}		3	kΩ
Output capacitance	C_{os}		2.5	pF
Power gain	PG	$V_{DS}=5V$, $I_D=10mA$, $f=100MHz$	15	dB
Noise figure	NF		1.8	dB
Equivalent input noise voltage	$\bar{e}_n$	$V_{DS}=5V$, $I_D=10mA$ $f=1kHz$, $R_g=0\Omega$	1.2	$nV/\sqrt{Hz}$
Reverse transfer capacitance	C_{rss}	$V_{DS}=5V$, $V_{GS}=0V$, $f=1MHz$	2.0	pF

100 MHz PG, NF Test Circuit

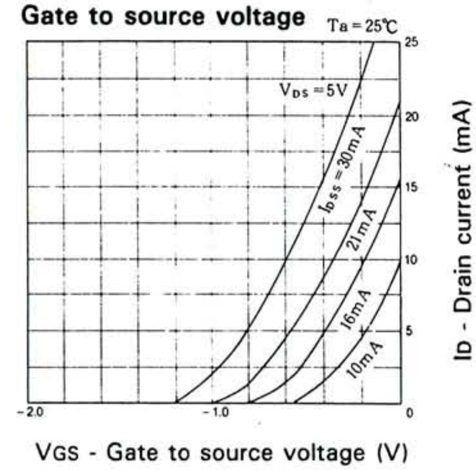


L1 ϕ0.45mm Polyurethane Wireϕ3mm 10.5t
L2, L3 ϕ0.45mm Polyurethane Wireϕ3mm 5.5t

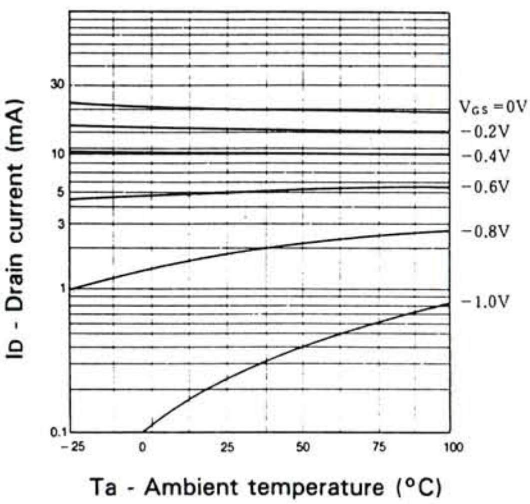
Drain current vs. Drain to source voltage



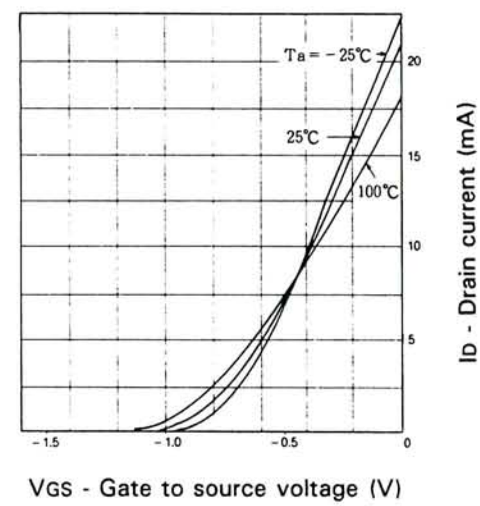
Drain current vs. Gate to source voltage



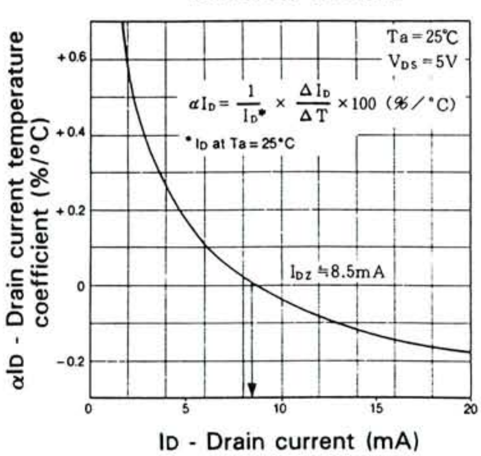
Drain current vs. Ambient temperature



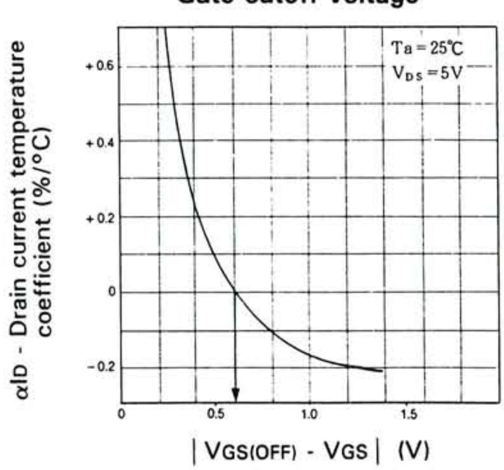
Transfer characteristics vs. Ambient temperature



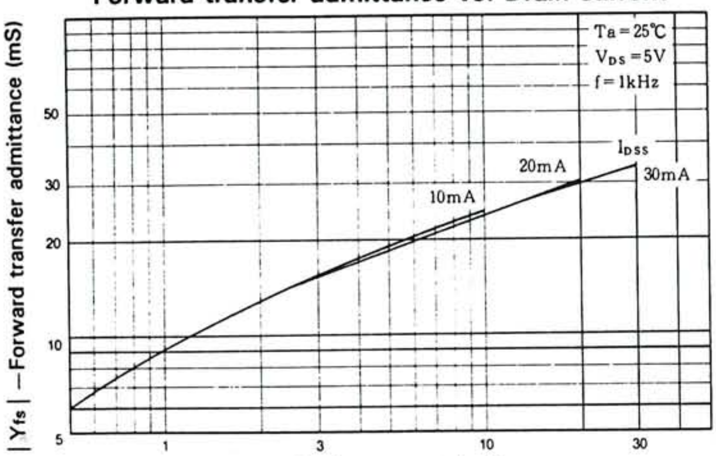
Drain current temperature coefficient vs. Drain current



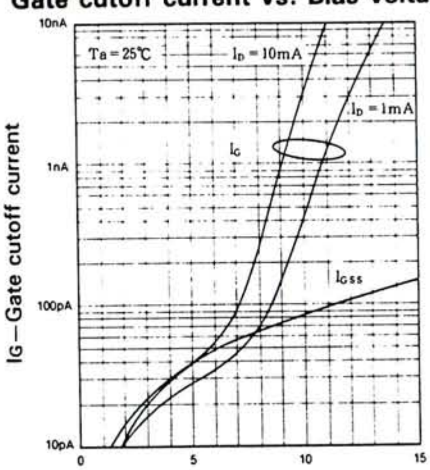
Drain current temperature coefficient vs. Gate cutoff voltage



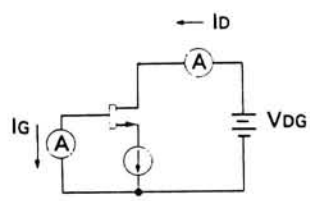
Forward transfer admittance vs. Drain current



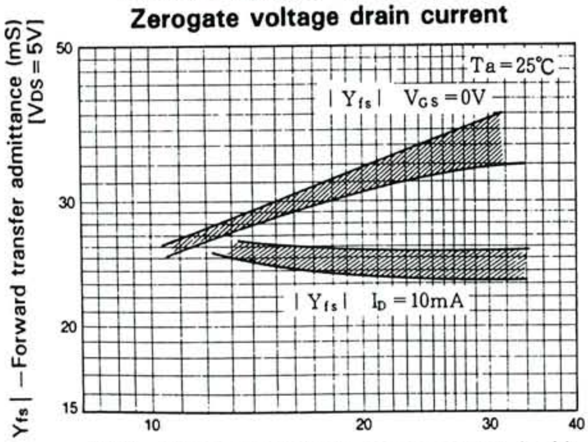
Gate cutoff current vs. Bias voltage



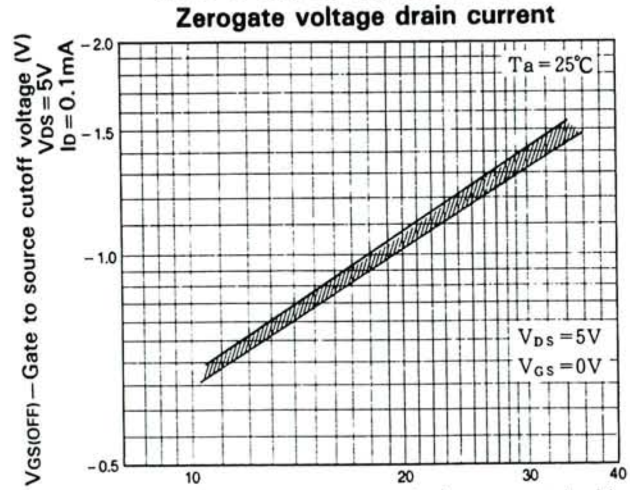
IG Test Circuit



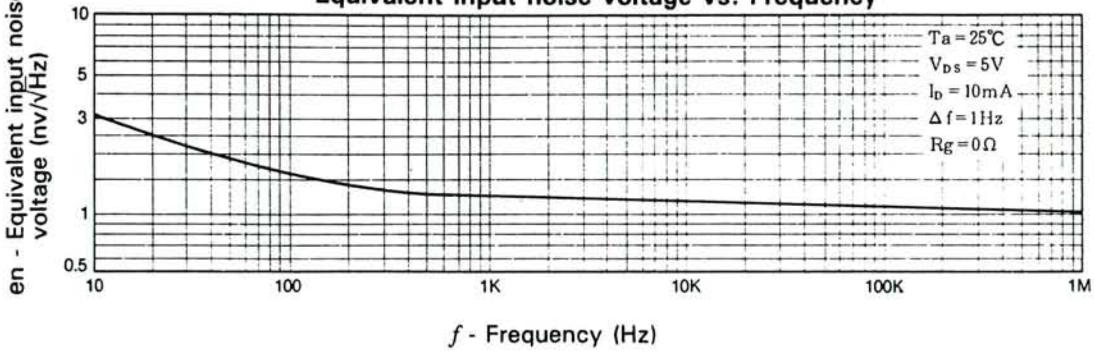
Forward transfer admittance vs. Zerogate voltage drain current



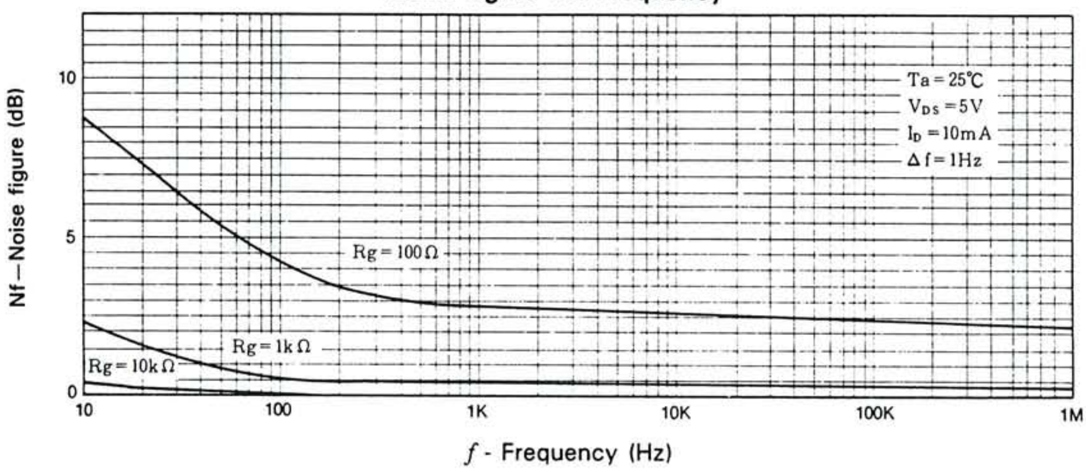
Gate to source cutoff voltage vs. Zerogate voltage drain current



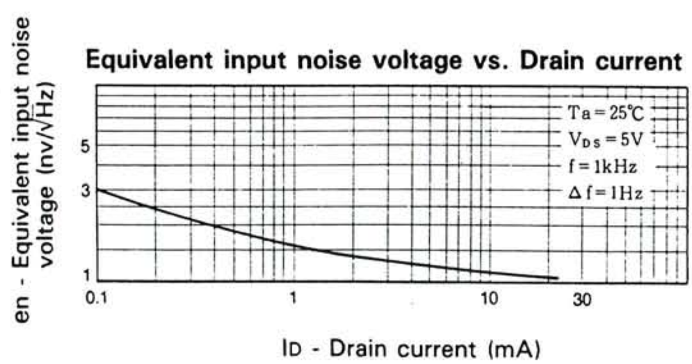
Equivalent input noise voltage vs. Frequency



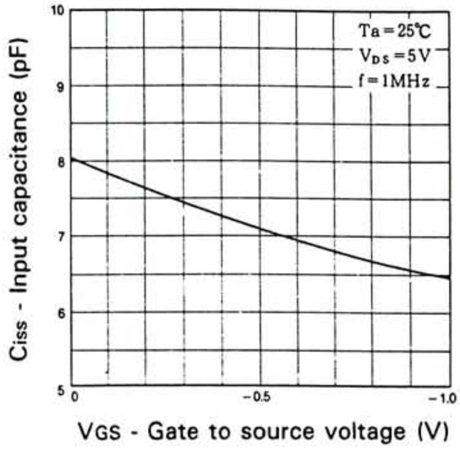
Noise figure vs. Frequency



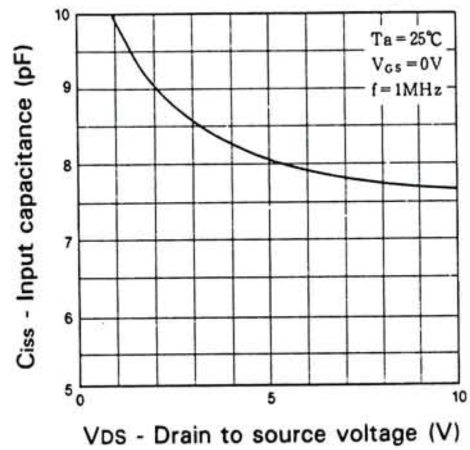
Equivalent input noise voltage vs. Drain current



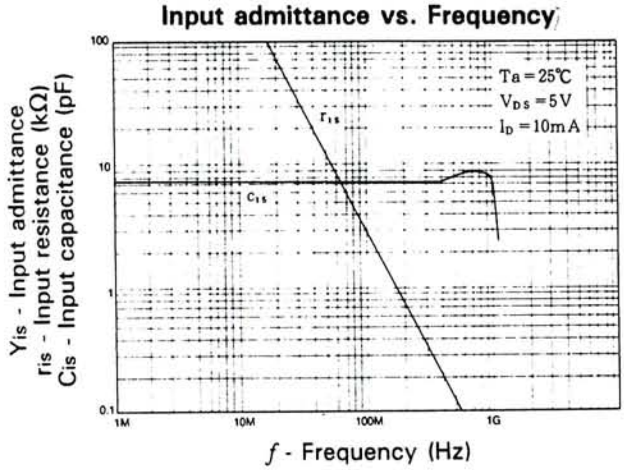
Input capacitance vs. Gate to source voltage



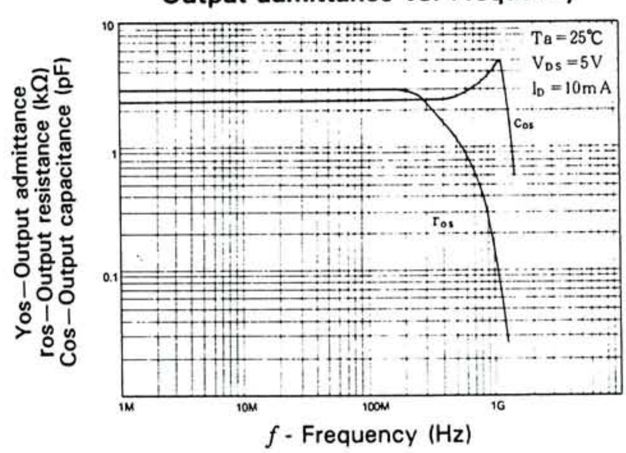
Input capacitance vs. Drain to source voltage



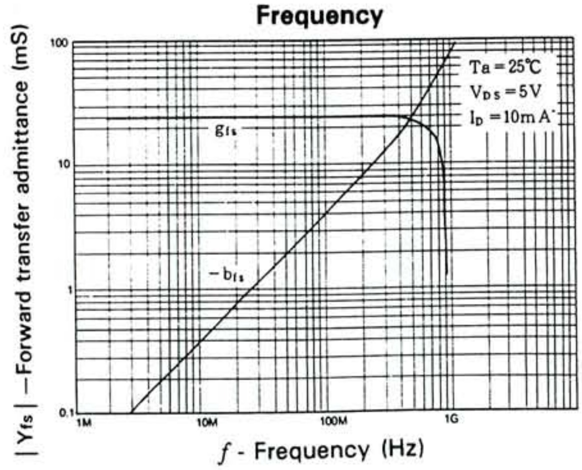
Input admittance vs. Frequency



Output admittance vs. Frequency



Forward transfer admittance vs. Frequency



Reverse transfer admittance vs. Frequency