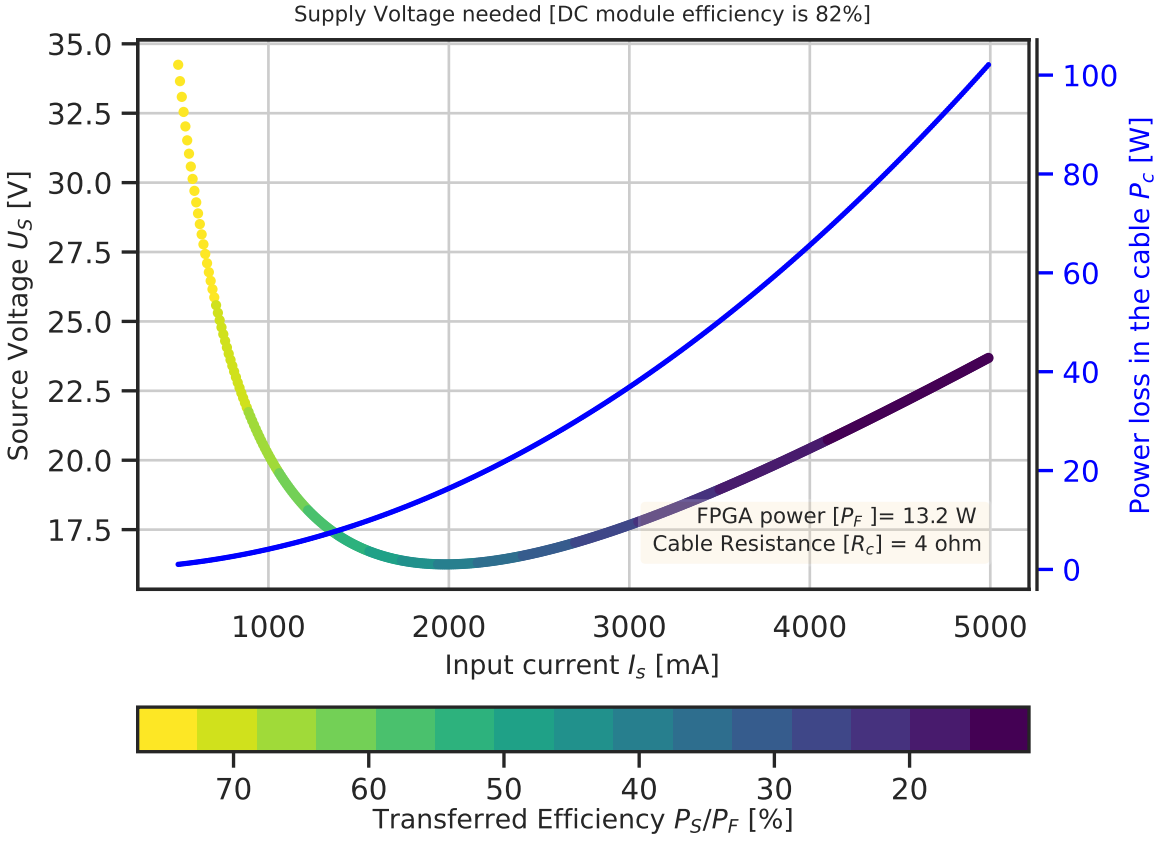
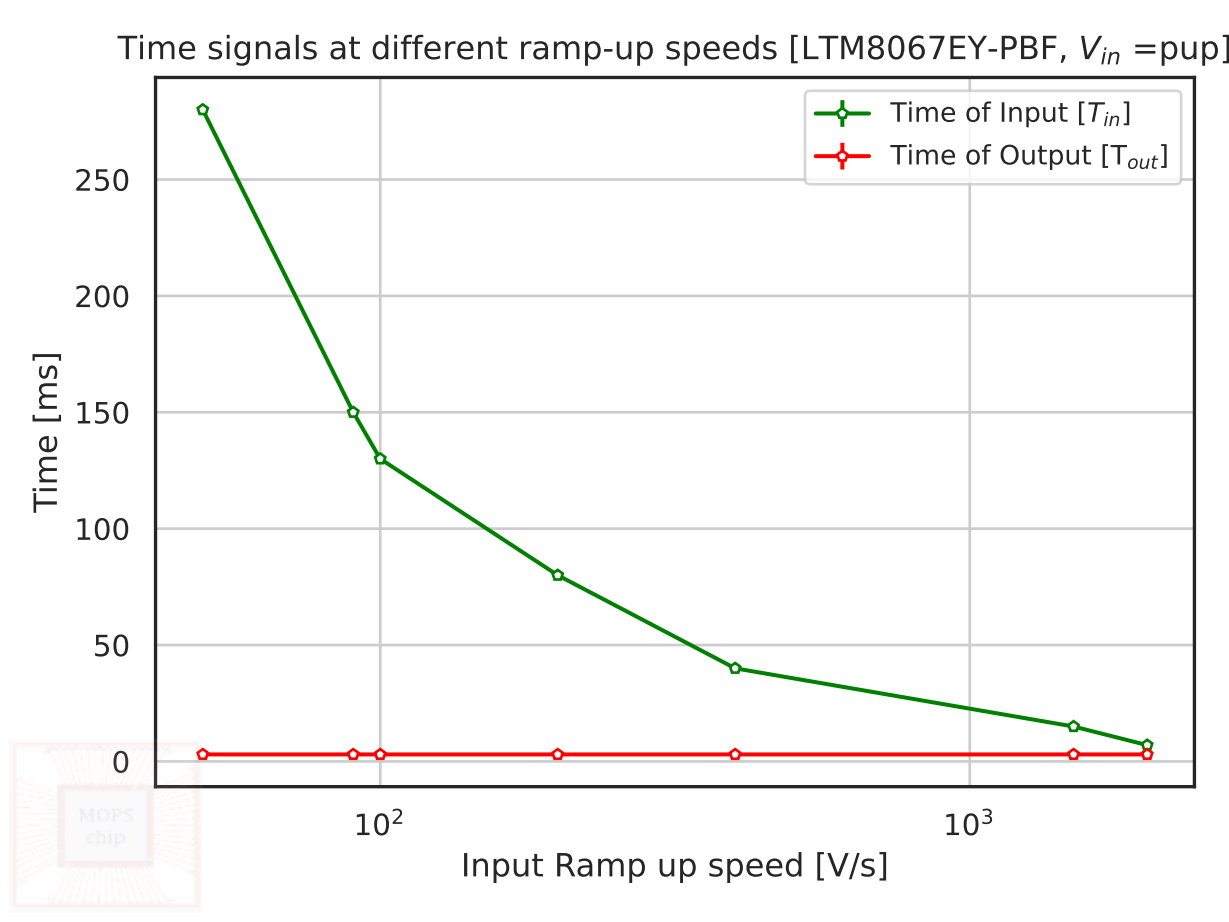
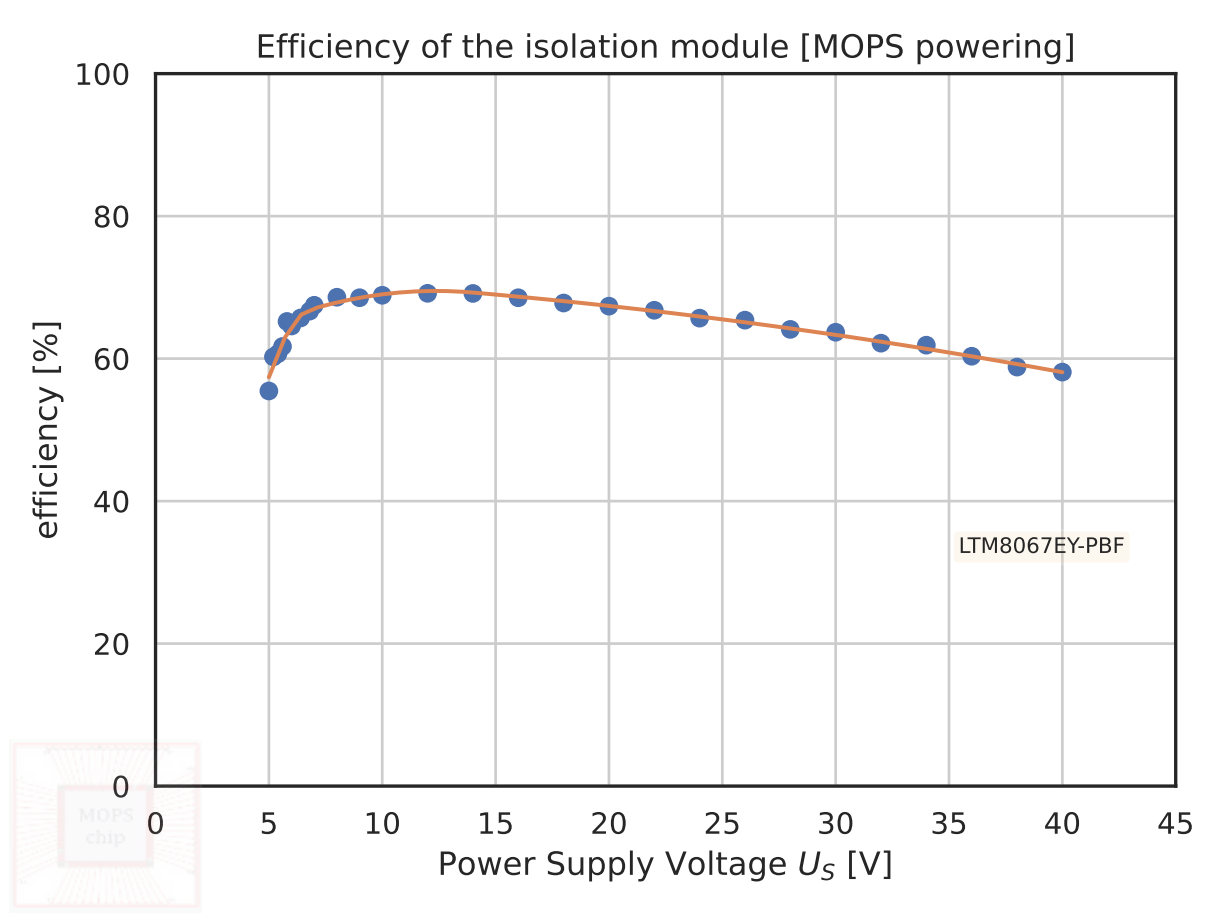
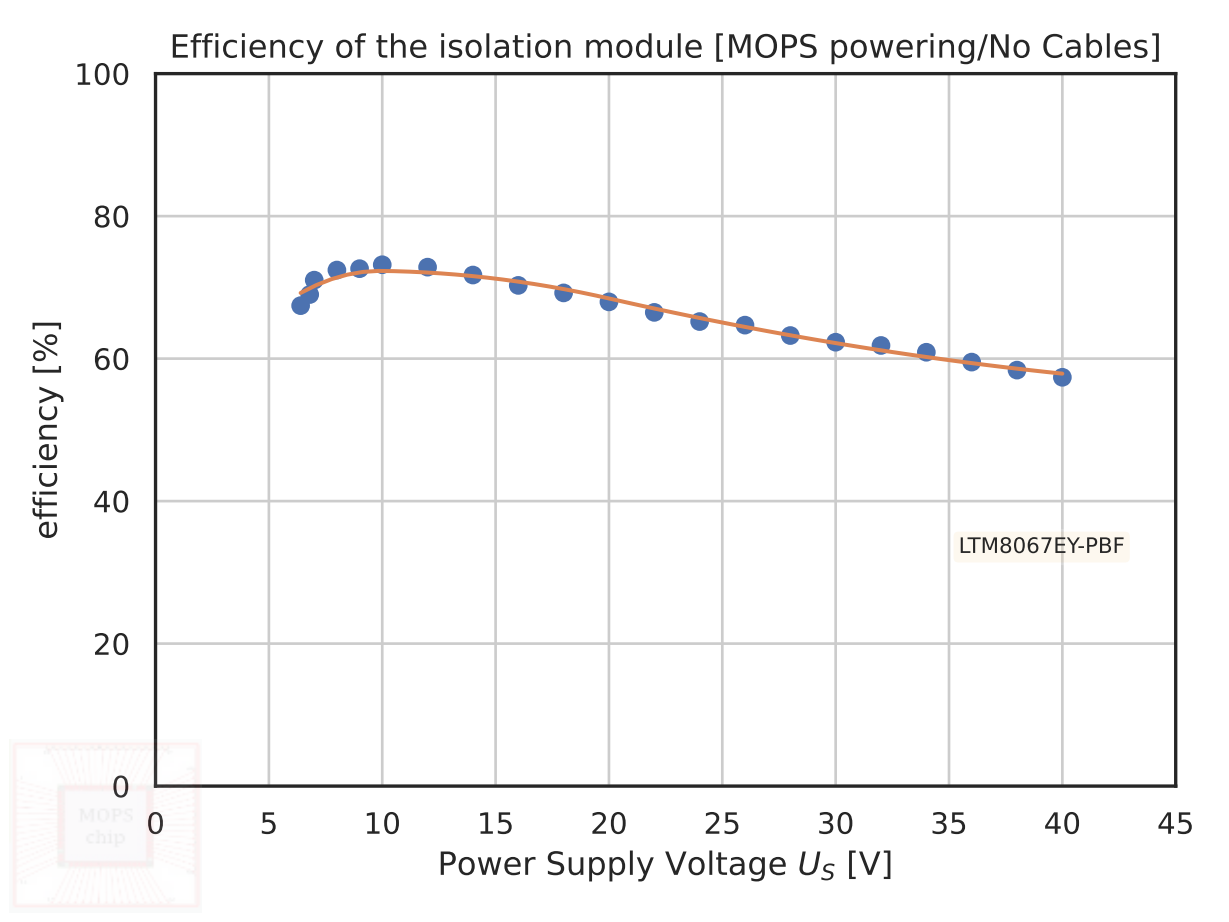
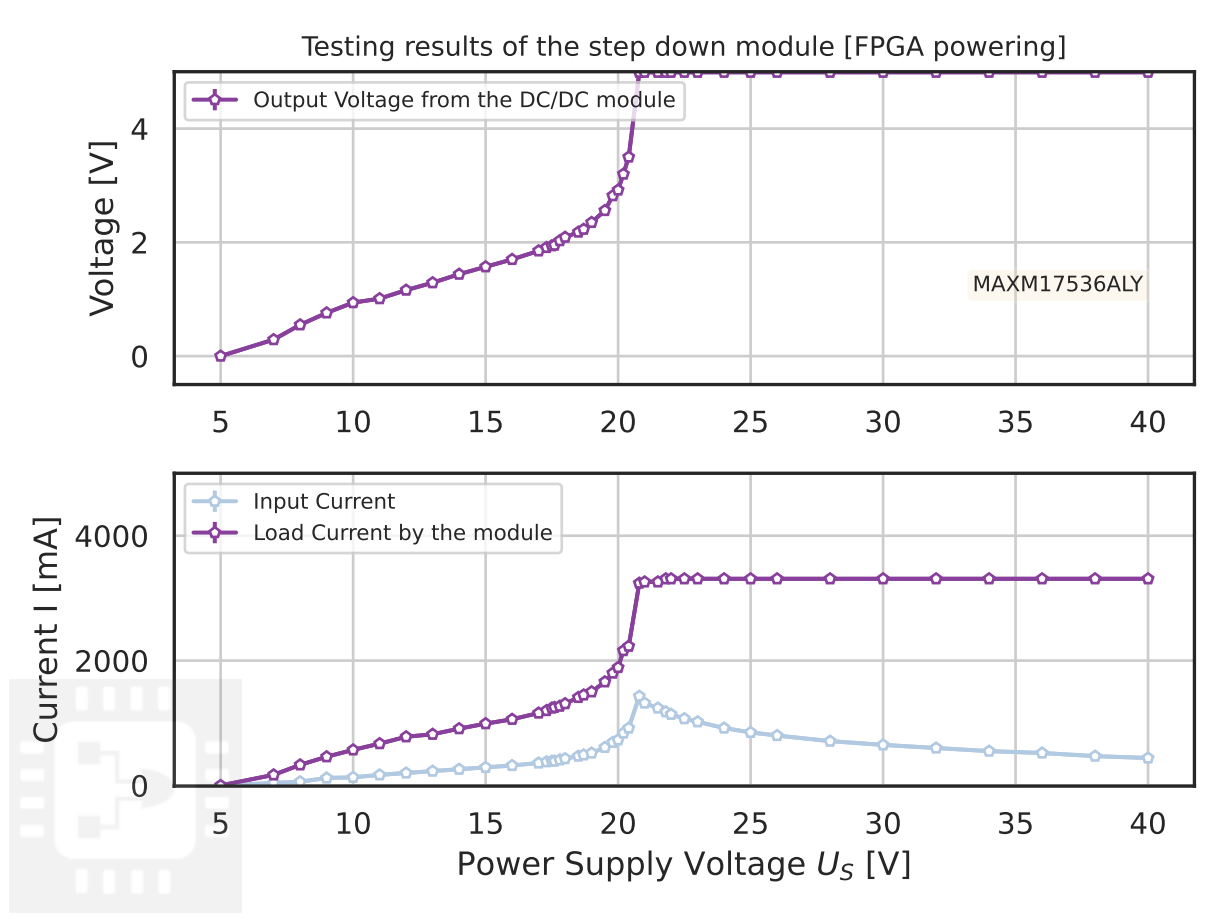
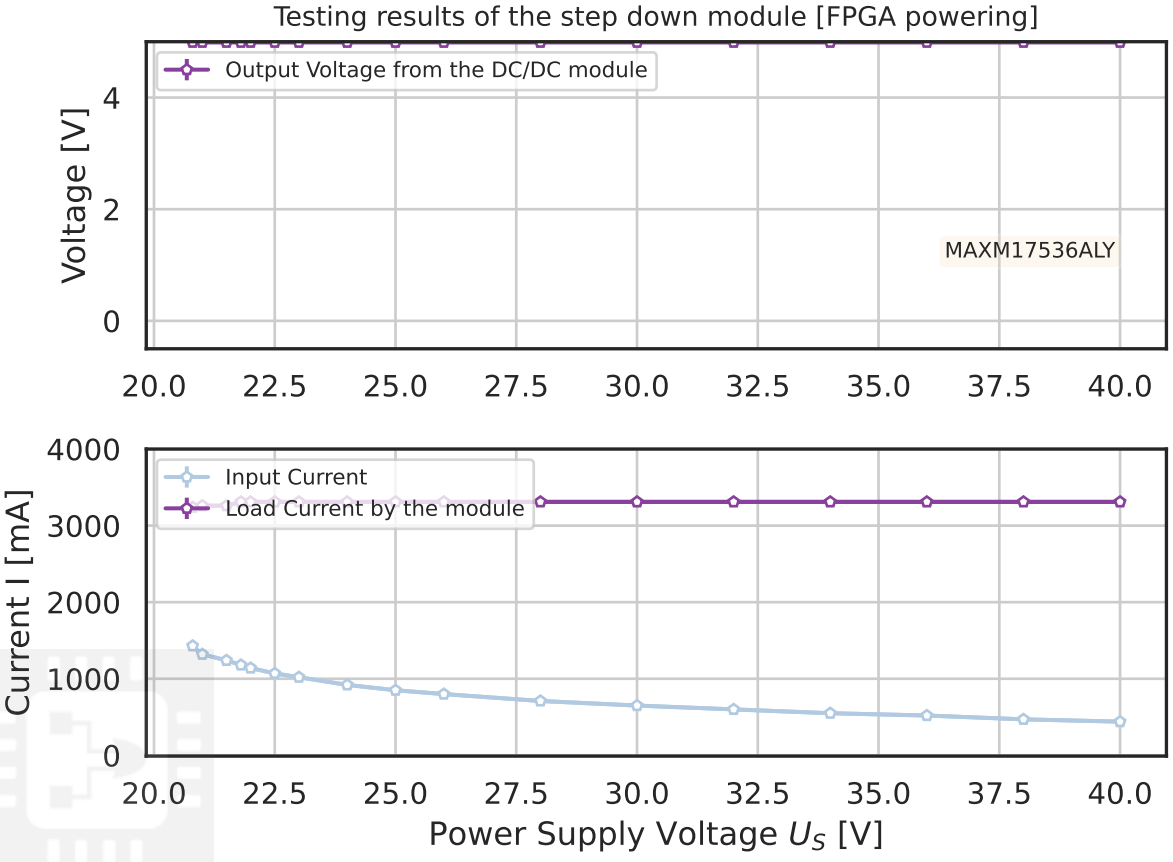

Supply Voltage needed [DC module efficiency is 82%]
Source Voltage U_S [V]
35.0
32.5
30.0
27.5
25.0
22.5
20.0
17.5
Power loss in the cable P_c [W]
100
80
60
40
20
0
FPGA power [P_F]= 13.2 W
Cable Resistance [R_c] = 4 ohm
1000
2000
3000
4000
5000
Input current I_s [mA]
70
60
50
40
30
20
Transferred Efficiency P_S/P_F [%]

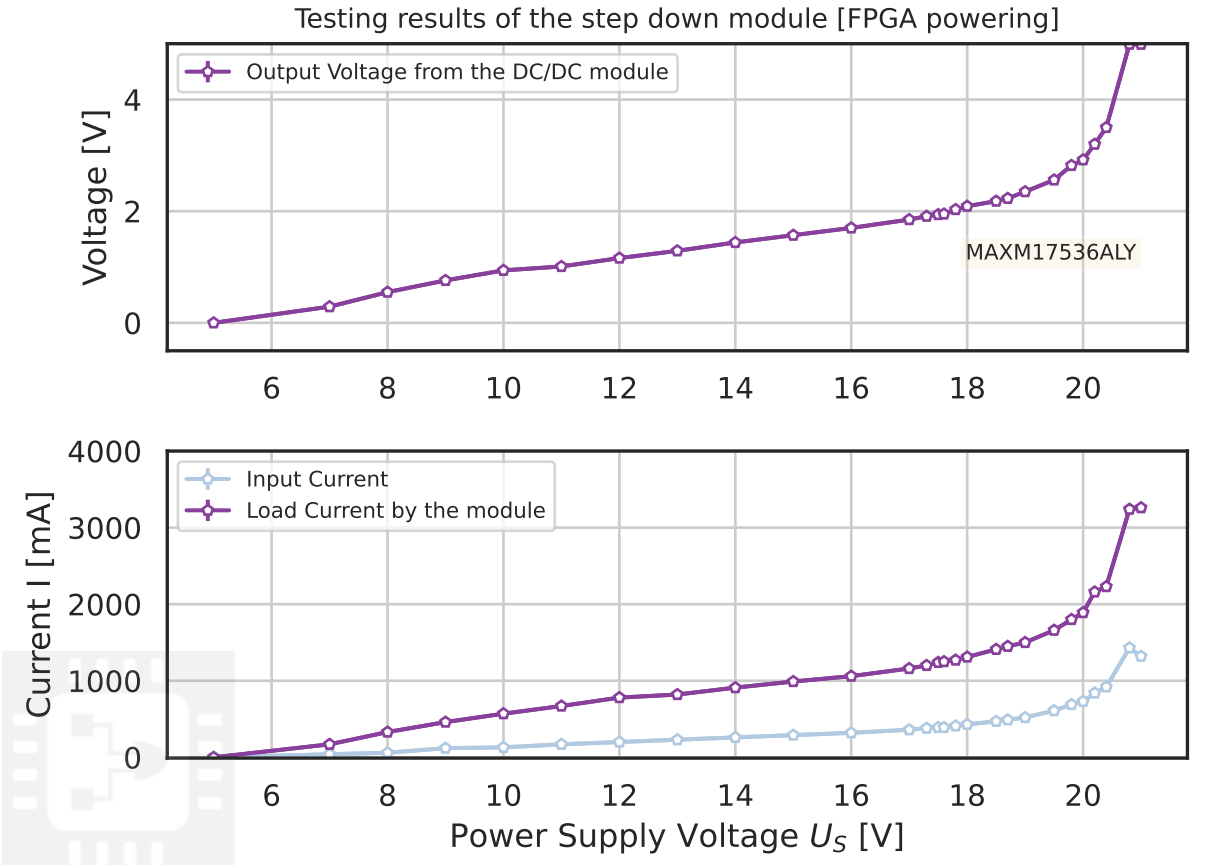

Time signals at different ramp-up speeds [LTM8067EY-PBF, V_{in} =pup]
Time of Input [T_{in}]
Time of Output [T_{out}]
Time [ms]
250
200
150
100
50
0
10^2
10^3
Input Ramp up speed [V/s]

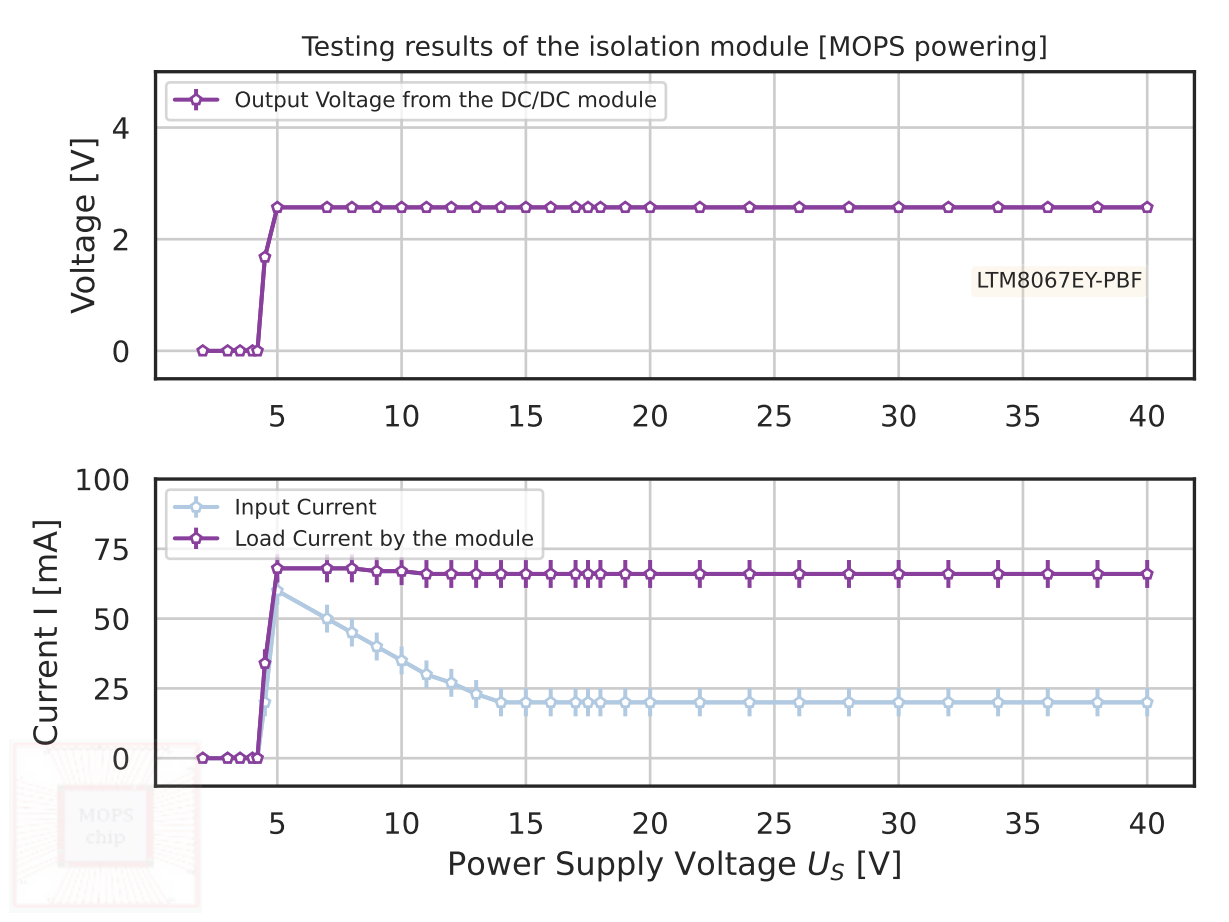

Efficiency of the isolation module [MOPS powering]
efficiency [%]
100
80
60
40
20
0
0
5
10
15
20
25
30
35
40
45
Power Supply Voltage U_S [V]
LTM8067EY-PBF

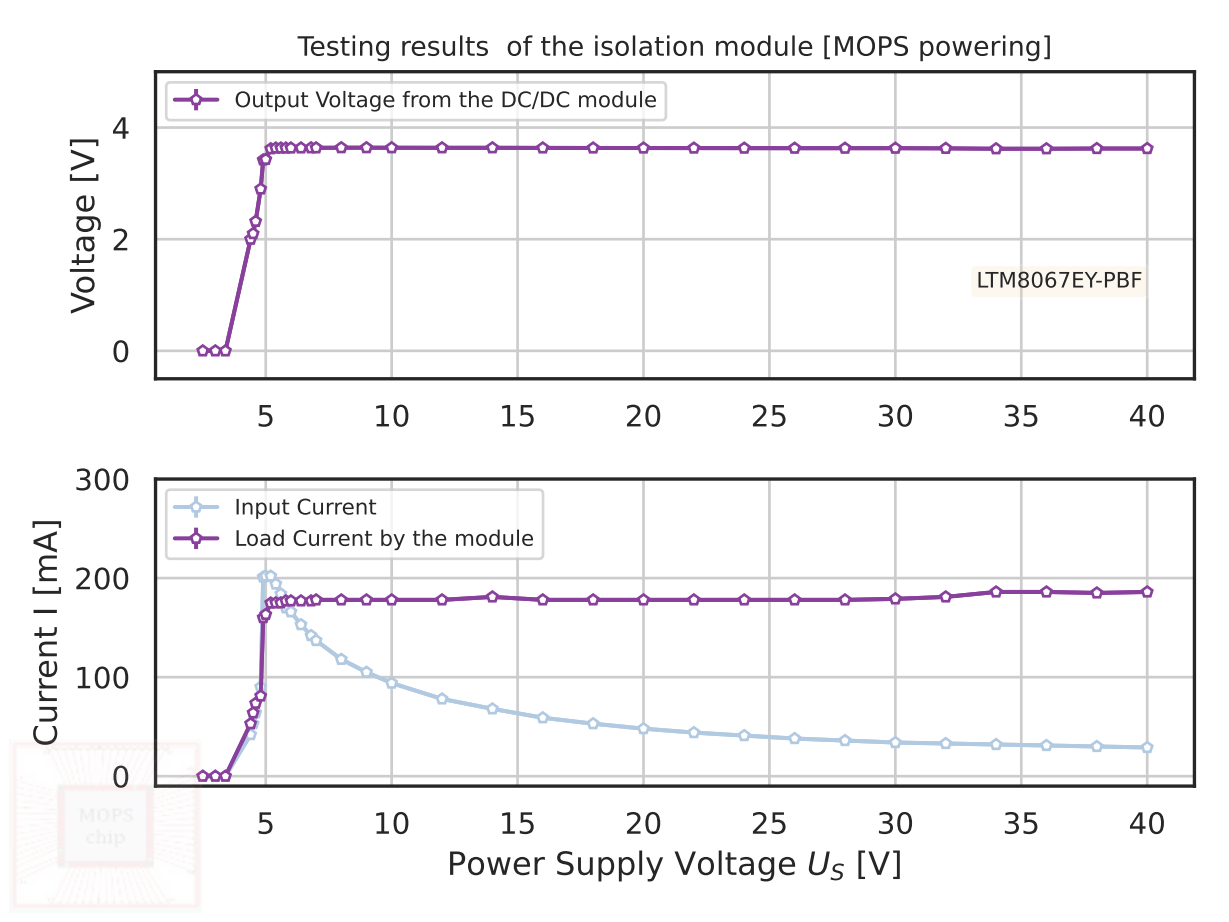

Efficiency of the isolation module [MOPS powering/No Cables]
efficiency [%]
100
80
60
40
20
0
0
5
10
15
20
25
30
35
40
45
Power Supply Voltage U_S [V]
LTM8067EY-PBF

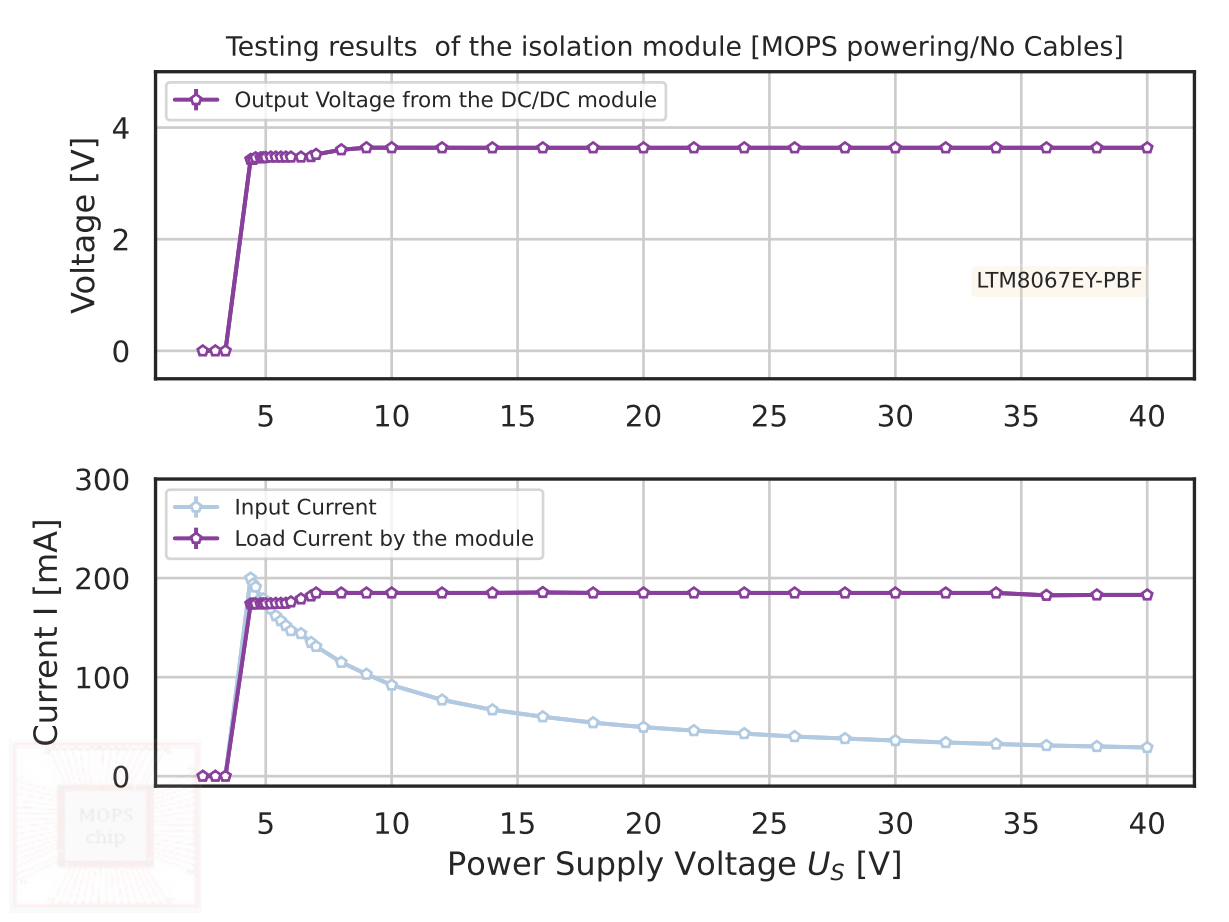

Testing results of the step down module [FPGA powering]
Output Voltage from the DC/DC module
Voltage [V]
0
2
4
MAXM17536ALY
5
10
15
20
25
30
35
40
Input Current
Load Current by the module
Current I [mA]
0
2000
4000
Power Supply Voltage U_S [V]

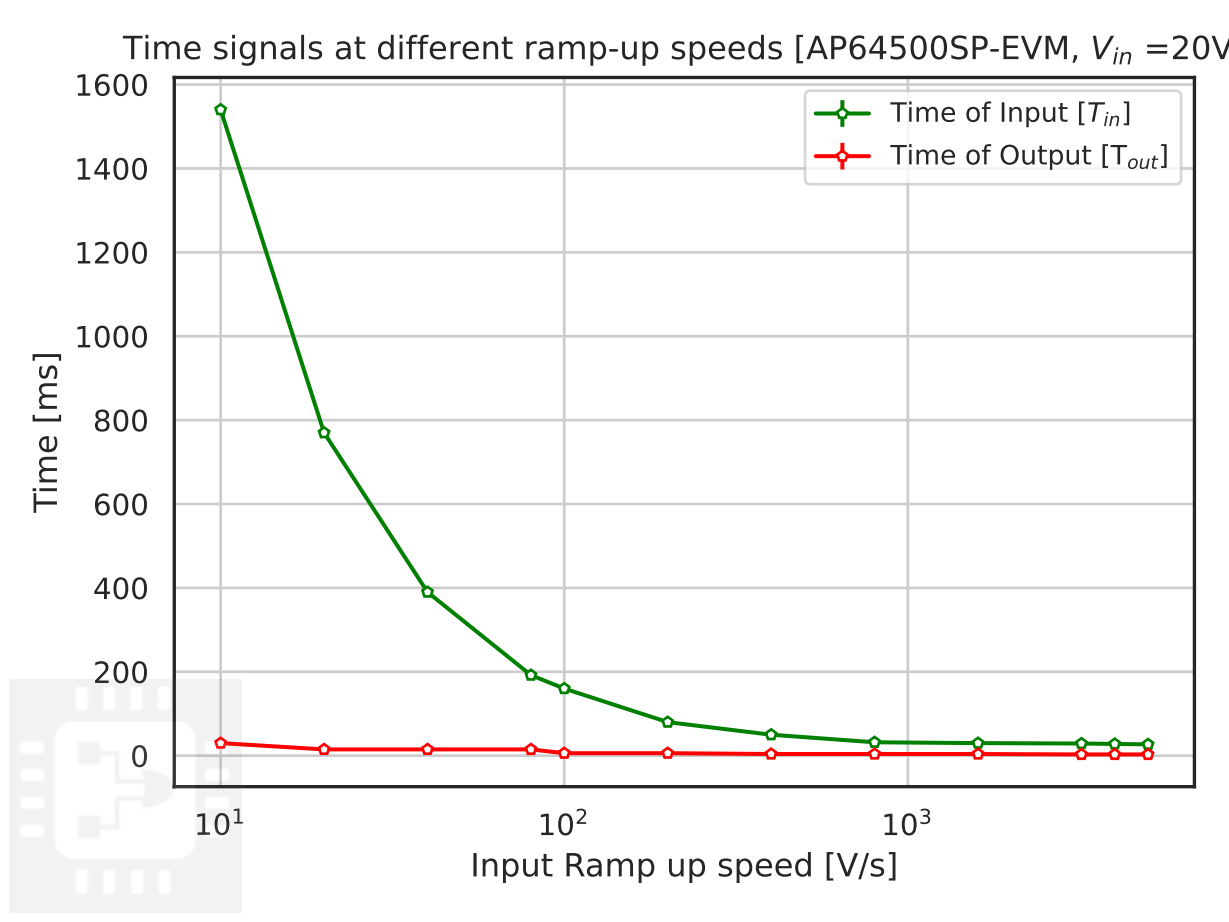

Testing results of the step down module [FPGA powering]
Output Voltage from the DC/DC module
MAXM17536ALY
Voltage [V]
0
2
4
20.0
22.5
25.0
27.5
30.0
32.5
35.0
37.5
40.0
Input Current
Load Current by the module
Current I [mA]
0
1000
2000
3000
4000
Power Supply Voltage U_S [V]

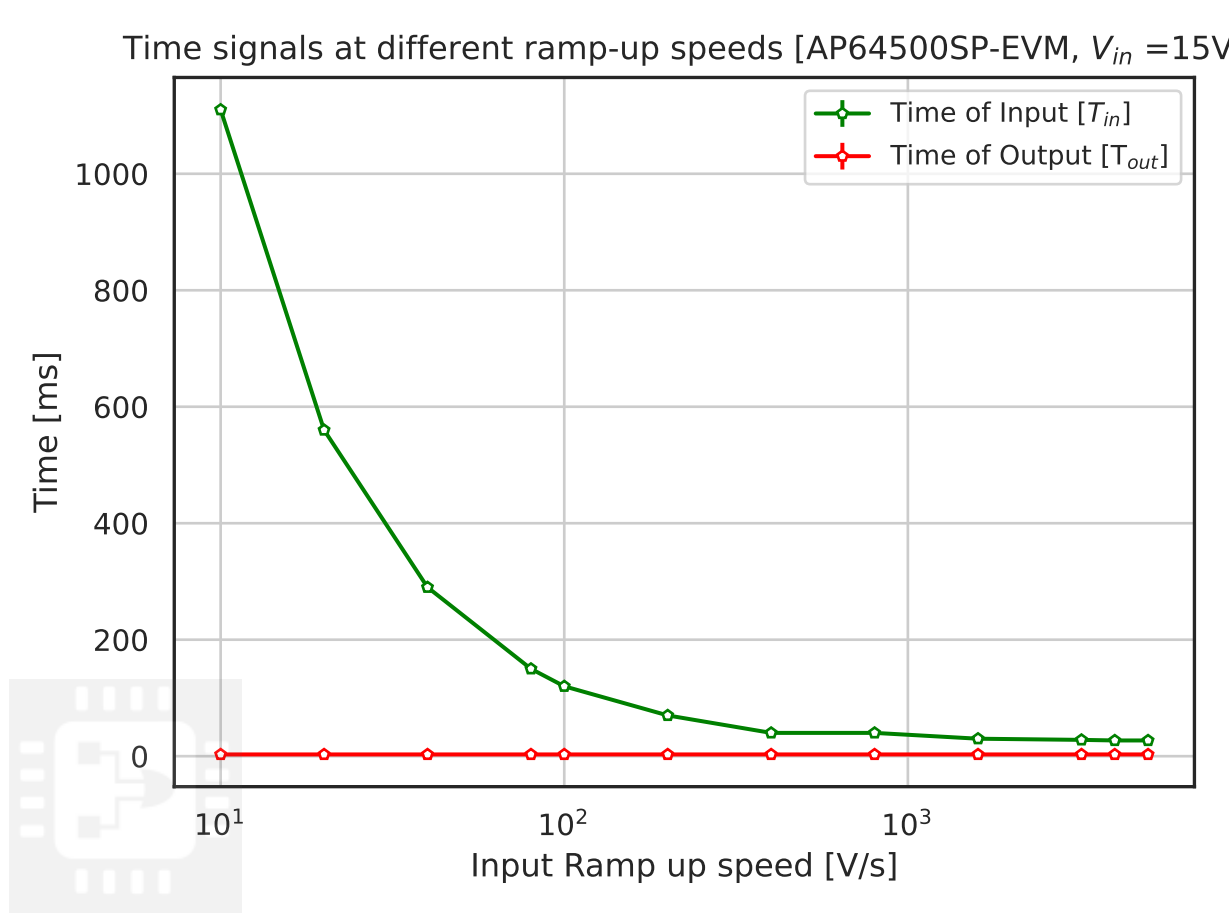

Testing results of the step down module [FPGA powering]
Output Voltage from the DC/DC module
MAXM17536ALY
Voltage [V]
0
2
4
6
8
10
12
14
16
18
20
Input Current
Load Current by the module
Current I [mA]
0
1000
2000
3000
4000
Power Supply Voltage U_S [V]

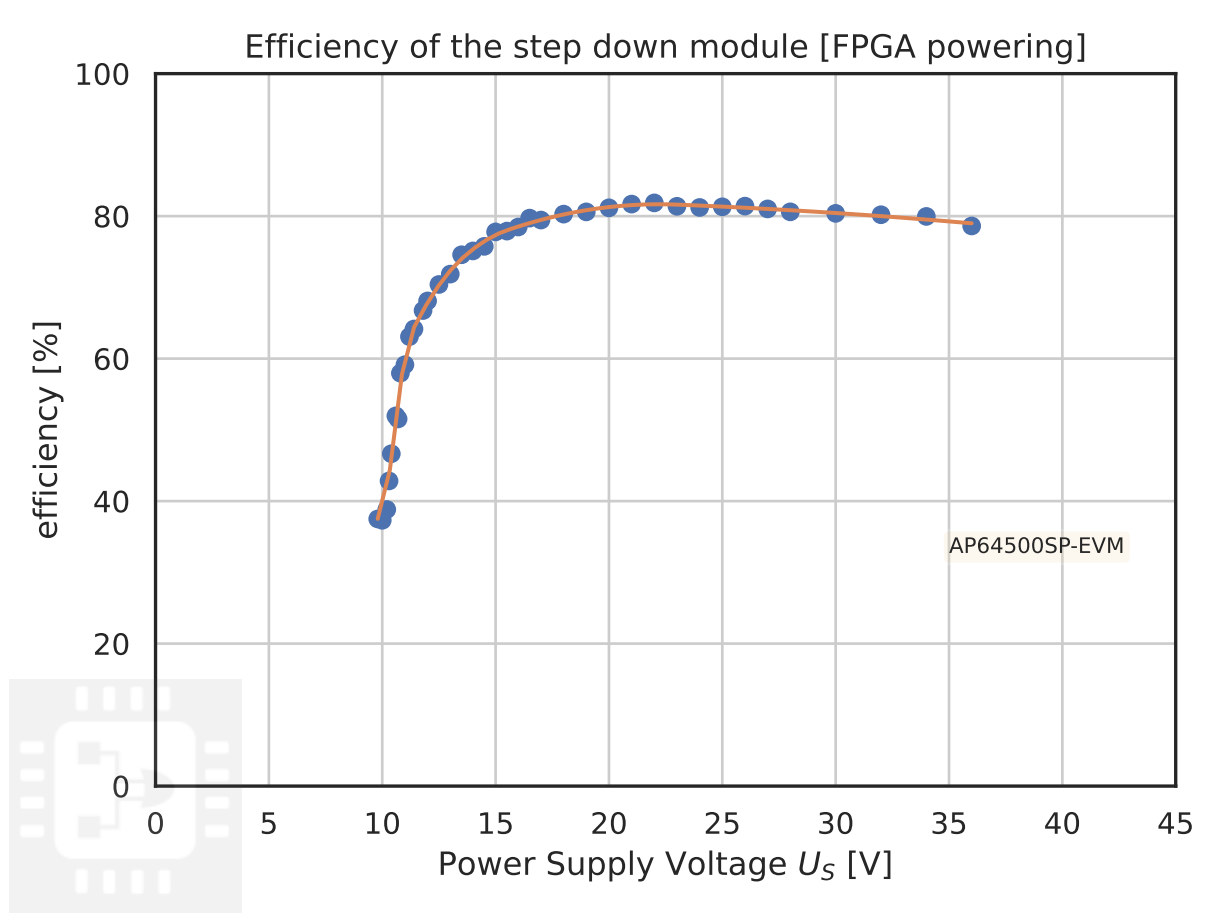

Testing results of the isolation module [MOPS powering]
Output Voltage from the DC/DC module
Voltage [V]
LTM8067EY-PBF
Input Current
Load Current by the module
Current I [mA]
Power Supply Voltage U_S [V]

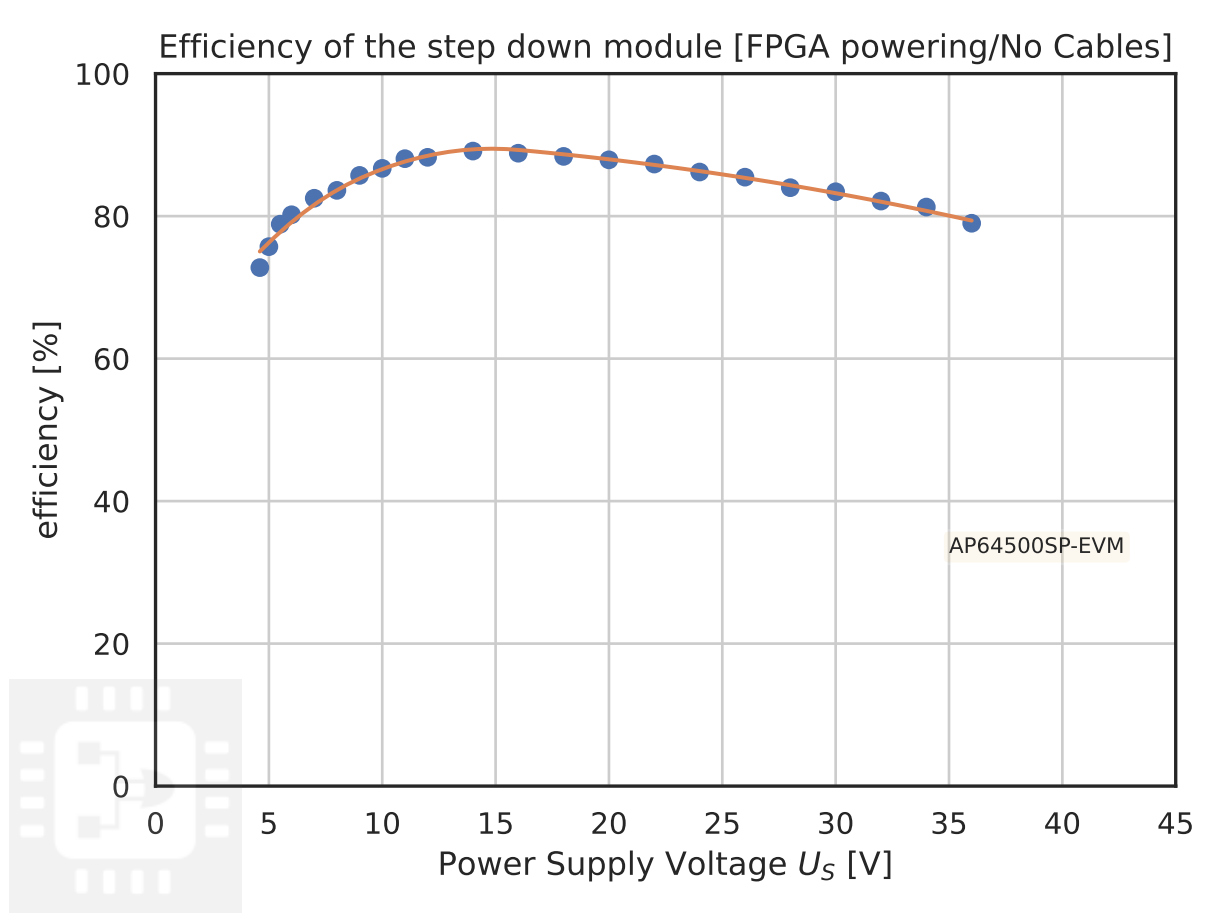

Testing results of the isolation module [MOPS powering]
Output Voltage from the DC/DC module
Voltage [V]
LTM8067EY-PBF
Input Current
Load Current by the module
Current I [mA]
Power Supply Voltage U_S [V]

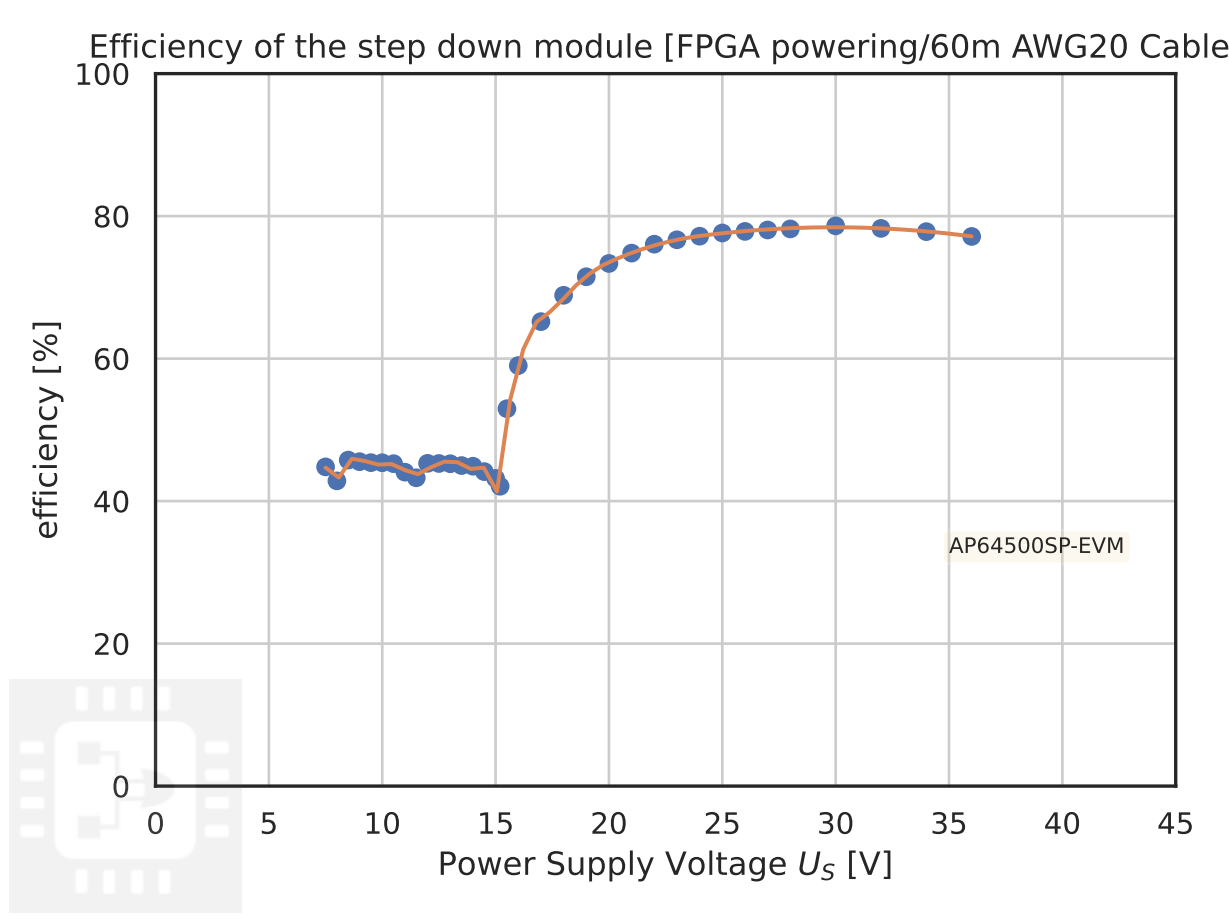

Testing results of the isolation module [MOPS powering/No Cables]
Output Voltage from the DC/DC module
Voltage [V]
0
2
4
LTM8067EY-PBF
5
10
15
20
25
30
35
40
Input Current
Load Current by the module
Current I [mA]
0
100
200
300
Power Supply Voltage U_S [V]

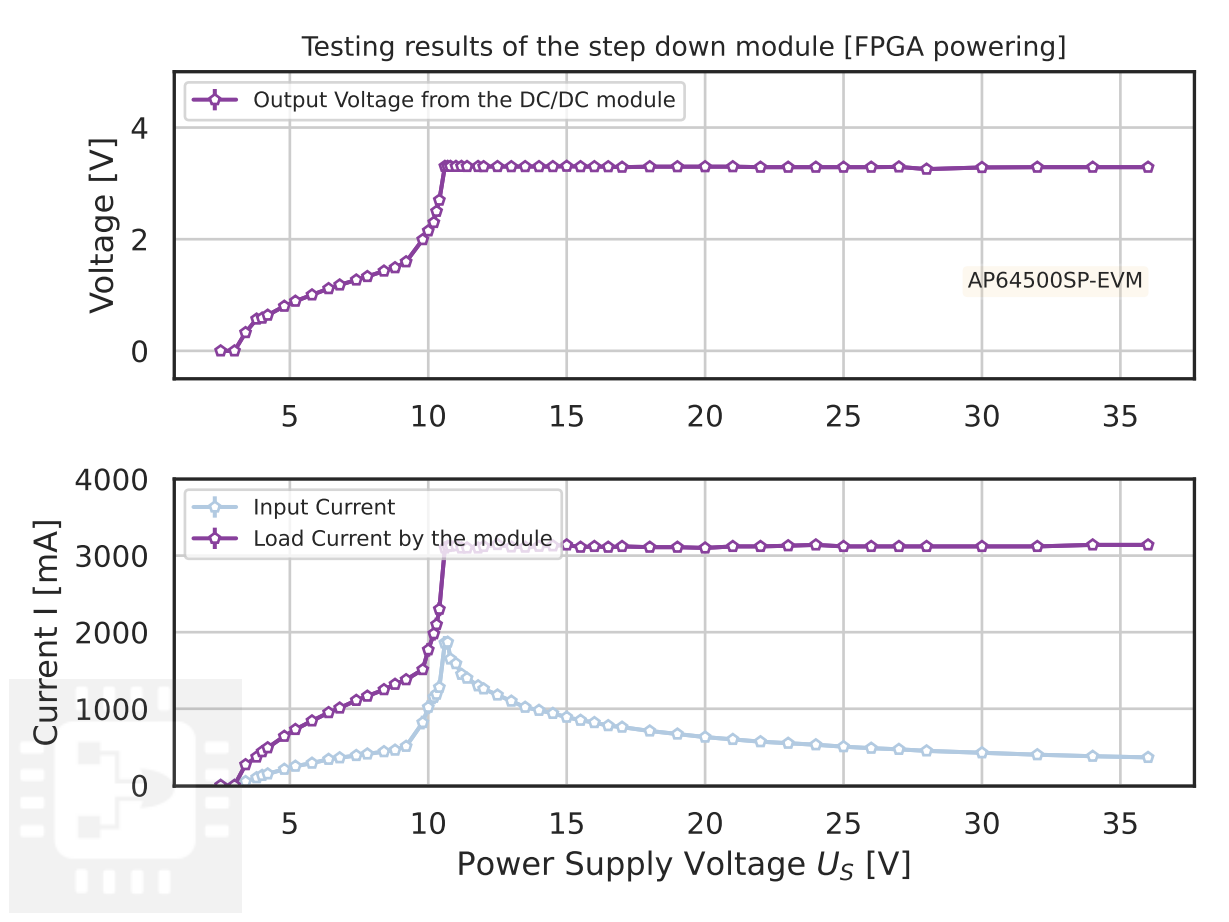

Time signals at different ramp-up speeds [AP64500SP-EVM, V_{in} =20V
Time of Input [T_{in}]
Time of Output [T_{out}]
Time [ms]
1600
1400
1200
1000
800
600
400
200
0
10^1
10^2
10^3
Input Ramp up speed [V/s]


Time signals at different ramp-up speeds [AP64500SP-EVM, V_{in} =15V
Time of Input [T_{in}]
Time of Output [T_{out}]
1000
800
600
400
200
0
Time [ms]
10^1
10^2
10^3
Input Ramp up speed [V/s]


Efficiency of the step down module [FPGA powering]
efficiency [%]
100
80
60
40
20
0
0
5
10
15
20
25
30
35
40
45
Power Supply Voltage U_S [V]
AP64500SP-EVM


Efficiency of the step down module [FPGA powering/No Cables]
efficiency [%]
100
80
60
40
20
0
0
5
10
15
20
25
30
35
40
45
Power Supply Voltage U_S [V]
AP64500SP-EVM


Efficiency of the step down module [FPGA powering/60m AWG20 Cable
efficiency [%]
100
80
60
40
20
0
0
5
10
15
20
25
30
35
40
45
Power Supply Voltage U_S [V]
AP64500SP-EVM


Testing results of the step down module [FPGA powering]
Output Voltage from the DC/DC module
Voltage [V]
AP64500SP-EVM
Input Current
Load Current by the module
Current I [mA]
Power Supply Voltage U_S [V]